RS485/RS422 Transceivers Operate from 3V to 5.5V Supplies and Withstand ±60V Faults

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The LTC2862–LTC2865 are robust RS485/RS422 transceivers that feature ±60V overvoltage and ±15kV ESD tolerance to reduce failures caused by electrical overstress. These transceivers introduce several new capabilities for high voltage tolerant RS485 transceivers: operation from 3V to 5.5V supply voltages, up to 20Mbps data rate, ±25V common mode voltage range, selectable slew rate, interface to low voltage logic, and availability in 3mm × 3mm DFN packages.

The venerable RS485 serial bus forms the backbone of many commercial and industrial data communications systems. RS485-based networks are used in a wide variety of applications, including industrial control systems, supervisory control and data acquisition systems, building automation and security, theatre and performance venue lighting control, commercial aircraft and ground vehicle busses, and other custom networked systems. Robustness to electrical overstress is an important attribute for RS485 transceivers used in these applications, with risk of wiring faults, ground voltage faults and lightning induced surge voltages.

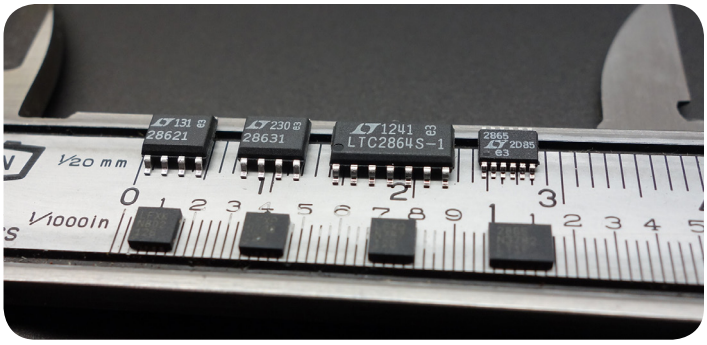

Figure 1. This family of robust high voltage tolerant transceivers includes features typically only found only in less robust ICs

However, most high voltage tolerant RS485 transceivers lack the performance and features of the latest non high voltage tolerant RS485 transceivers. The LTC2862–LTC2865 transceivers fill this gap by combining fault tolerance with the expanded capabilities demanded in the specifications for contemporary network applications.

3V TO 5.5V OPERATION

High voltage tolerant RS485 transceivers typically operate from 5V supplies, but the 5V supply is fast becoming an anachronism, rarely used in modern digital circuits. In some cases, a fault-tolerant RS485 transceiver is the only 5V component in the system, incurring the cost of a dedicated supply.

In contrast to some high voltage tolerant transceivers, the LTC2862–LTC2865 maintain full compliance to RS485 and RS422 standards when operating from a 3.3V supply. Competing parts sometimes drive a reduced VOD when powered by 3.3V. The LTC2862–LTC2865 transceivers are fully interoperable with 5V-powered transceivers on the same bus when operating from either a 3.3V or 5V supply.

LOW VOLTAGE LOGIC INTERFACE

Many microcontroller systems operate at voltages lower than 3.3V. The LTC2865 provides the means to interface to logic operating as low as 1.65V. A V_L supply pin and built in level shifters translate the I/O signals from the lower voltage V_L logic supply to the higher voltage V_{CC} supply used to power the RS485 receiver and transmitter. This eliminates the need for external level shifters in mixed-voltage RS485 systems. The two supplies may be powered up and powered down independently of each other.

20Mbps OR 250kbps DATA RATE

Modern RS485 systems can operate at data rates that exceed the capabilities of most high voltage tolerant transceivers. For example, the highly popular LT1785/LT1791 transceivers operate at a maximum of 250kbps. The LTC2862–LTC2865 offer similar high voltage tolerance, but can communicate 160 times faster at up to 20Mbps.

Not all systems require a high data rate. In applications where 250kbps suffices, the system designer may prefer an RS485 driver with low EMI slew-controlled

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transitions. The LTC2862–LTC2865 satisfy this need. These parts come in two versions: the high speed 20Mbps LTC2862-1, LTC2863-1, LTC2864-1; and the slew-limited 250kbps LTC2862-2, LTC2863-2, LTC2864-2. The LTC2865 supports both the high speed and the slew-limited transmit modes and provides an additional input pin to select between the two modes.

±25V COMMON MODE VOLTAGE RANGE

Standard RS485 transceivers operate over a limited common mode voltage range that extends from –7V to 12V. In a commercial or industrial environment, ground faults, noise, and other electrical interference can induce common mode voltages that exceed these limits. An ideal RS485 transceiver would not only survive large common mode voltages but would continue to send and receive data without disruption.

The receivers in the LTC2862–LTC2865 operate over an expanded ±25V common mode voltage range. The receivers use low offset bipolar differential inputs, combined with high precision resistor dividers to maintain precise receiver thresholds over the wide common mode voltage range. The transmitters operate up to the absolute maximum voltages of ±60V, and will sink or source current up to the limits imposed by their current limit circuitry.

PART NUMBER	DUPLEX	ENABLES	V_L PIN	SLEW LIMIT PIN	PACKAGES
LTC2862-1, -2	HALF	YES	NO	NO	S8: 8-LEAD SO DD: 8-LEAD DFN
LTC2863-1, -2	FULL	NO	NO	NO	S8: 8-LEAD SO DD: 8-LEAD DFN
LTC2864-1, -2	FULL	YES	NO	NO	S: 14-LEAD SO DD: 10-LEAD DFN
LTC2865	FULL	YES	YES	YES	MSE: 12-LEAD MSOP DE: 12-LEAD DFN

Table 1. LTC2862–LTC2865 pinouts and packages

The LTC2862–LTC2865 excel in rejecting large amplitude, high frequency and high slew rate common mode perturbations. Figure 2 shows the LTC2865 receiving 10Mbps data with a ±200mV differential signal superimposed on a 50VP-P 1MHz common mode signal, while Figure 3 shows the LTC2865 receiving 20Mbps data with a ±200mV differential signal superimposed on a –12V step in the common mode voltage with a 36ns 10%–90% fall time. In a noisy electrical environment this exceptional common mode rejection can greatly improve the reliability of data communications.

Both the high speed 20Mbps and the slew-limited 250kbps version of the LTC2862–LTC2865 contain receivers with the full 20Mbps bandwidth. A fast common mode transient such as the one illustrated in Figure 3 can produce a differential voltage as it propagates along the cable if the capacitive loads on the two lines are not well matched. If the resulting differential voltage exceeds the receiver

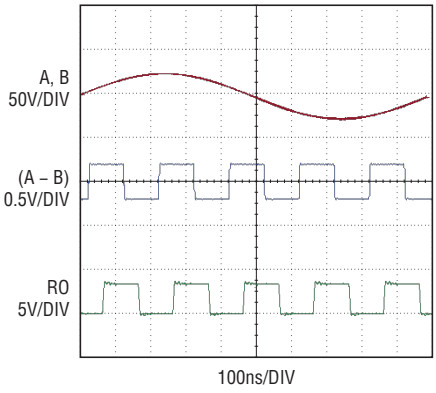

Figure 2. LTC2865 receiving 10Mbps ±200mV differential signal with 1MHz 50VP-P common mode sweep

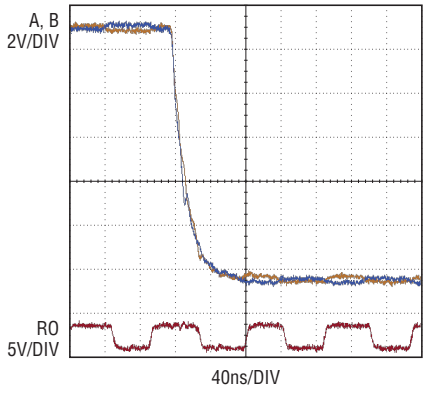

Figure 3. LTC2865 receiving 20Mbps ±200mV differential signal with –12V 36ns fall time common mode step

These devices have a failsafe feature that guarantees the receiver output is in a logic 1 state (the idle state) when the inputs are shorted, left open, or terminated but not driven, for more than about 3µs. The delay allows normal data signals to transition through the threshold region without being interpreted as a failsafe condition. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of –25V to 25V.

threshold it may trigger a state change in the receiver. In systems where the data rate is ≤ 250kbps, the noise immunity of the receivers may be increased by adding a 100pF–1nF capacitor across the receiver pins to filter the high frequency differential noise generated by common mode noise acting on mismatched capacitive loads.

FULL FAILSAFE OPERATION WITH SYMMETRICAL RECEIVER THRESHOLDS

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The LTC2862–LTC2865 implement the failsafe function with a window comparator (Figure 4). The comparator has fully symmetric positive and negative signal threshold voltages (typically ±75mV). The voltage difference between the two signal threshold voltages constitutes the signal hysteresis (typically 150mV). In addition the failsafe threshold voltage lies between the negative signal threshold voltage and 0V with a typical value of –50mV. The difference between the negative signal threshold voltage and the failsafe threshold voltage is the failsafe hysteresis, typically 25mV.

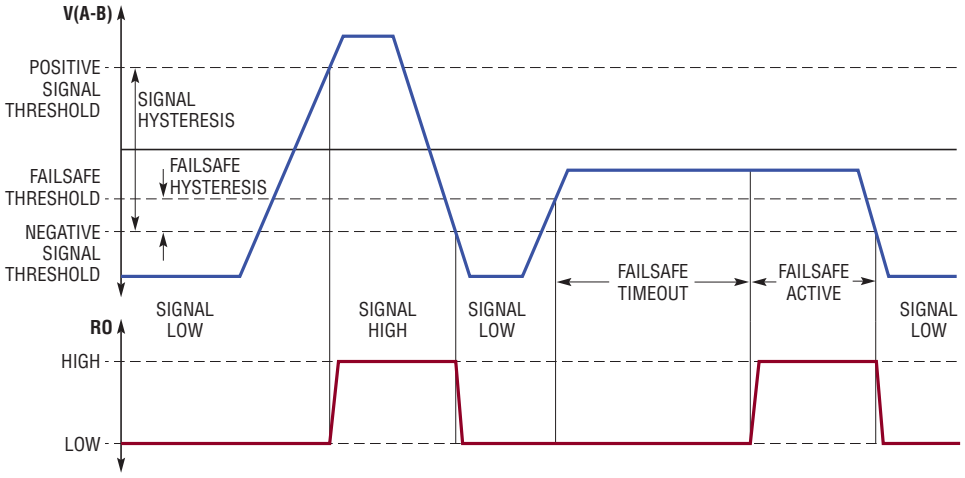


Figure 4. Failsafe window comparator operation

A normal data signal produces a high on the receiver output RO when the differential input voltage goes above the positive signal threshold voltage and a low on RO when the differential input voltage goes below the negative signal threshold voltage. The failsafe function is triggered when the differential input voltage goes above the failsafe threshold voltage but stays below the positive signal threshold for longer than the failsafe timeout time. When the failsafe timer times out, the failsafe is active and RO is forced high. It stays high until the differential input voltage goes below the negative signal threshold voltage.

Many RS485 transceivers have asymmetrical receiver thresholds that employ only the negative signal threshold and the failsafe threshold voltages. This provides effective failsafe detection but causes

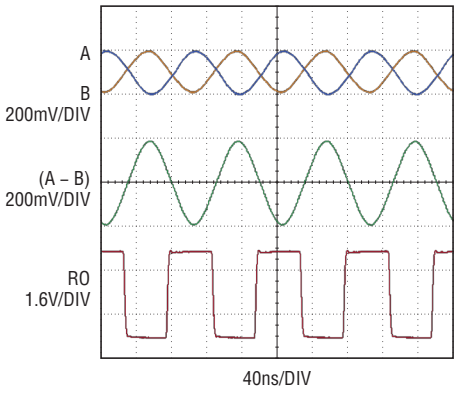


Figure 5. Duty cycle of LTC2865 symmetrical receiver with ±200mV 20Mbps input signal

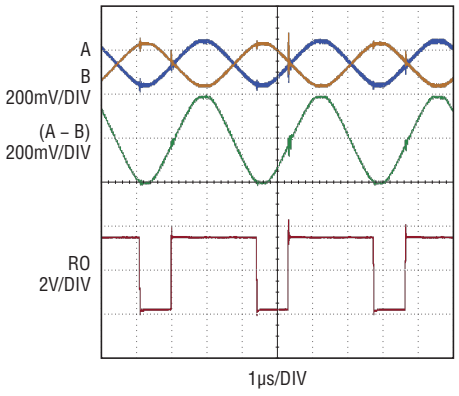


Figure 6. Duty cycle of competitor asymmetrical receiver with ±200mV 600kbps input signal

The LTC2862–LTC2865 feature glitch-free power-up and power-down protection to meet hot plugging (Hot Swap) requirements. These transceivers do not produce a differential disturbance on the bus when they are connected to the bus while unpowered, or while powered but disabled. Similarly, these transceivers do not produce a differential disturbance on the bus when they are powered up in the disabled state while already connected to the bus.

distortions in the duty cycle of the receiver output RO in the case of attenuated signals with slow edges. The symmetrical thresholds used in the LTC2862–LTC2865 maintain the proper duty cycle in the RO output even with highly attenuated signals (Figure 5), while a transceiver with asymmetric thresholds introduces substantial duty cycle distortion (Figure 6).

In addition, the 150mV (typical) signal hysteresis of the LTC2862–LTC2865 receivers provides superior noise immunity compared to receivers with asymmetrical receiver thresholds. Noise transients that momentarily go above the failsafe threshold but return below the negative signal threshold will trigger an erroneous high RO output in an asymmetric receiver (Figure 8) but are filtered out by the failsafe timer in the symmetric LTC2862–LTC2865 receivers (Figure 7).

HOT PLUGGING, HOT SWAPPING, AND GLITCH-FREE POWER-UP AND POWER-DOWN

The LTC2862–LTC2865 feature glitch-free power-up and power-down protection to meet hot plugging (Hot Swap) requirements. These transceivers do not produce a differential disturbance on the bus when they are connected to the bus while unpowered, or while powered but disabled. Similarly, these transceivers do not produce a differential disturbance on the bus when they are powered up in the disabled state while already connected to the bus. In these cases the receiver output RO remains off with a high impedance output.

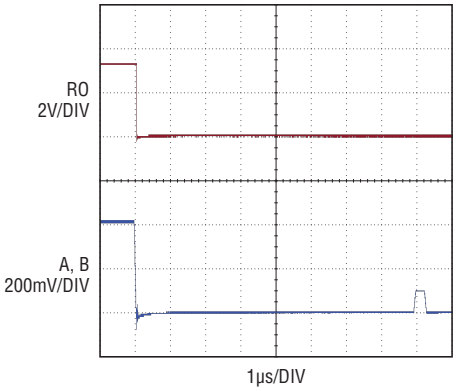


Figure 7. LTC2862 symmetrical receiver rejecting +100mV noise pulse on –200mV differential input

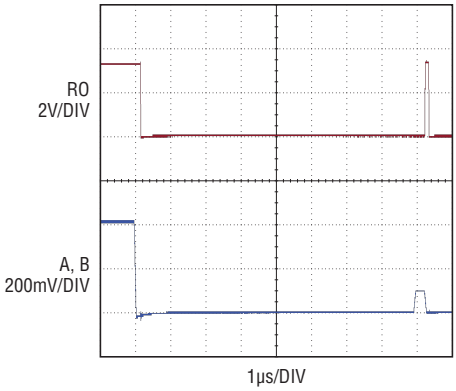


Figure 8. Competitor asymmetrical receiver responding to +100mV noise pulse on –200mV differential input

If the driver or receiver inputs are in an enabled state during power-up or power-down, the outputs make a glitch-free transition to the proper state as the supply passes through the transceiver's internal supply undervoltage detector threshold. The LTC2863 has no means to disable the receiver or driver, so it always powers up with a glitch-free transition to the fully enabled state.

PACKAGES AND PINOUTS

The LTC2862–LTC2865 offer four pin configurations to meet a wide range of application requirements, with each pinout offered in leaded and leadless packages.

LTC2862: The half-duplex LTC2862 with shared receive and transmit pins is the most commonly used version. It comes in an 8-pin leaded SO package and a small 3mm × 3mm 8-pin leadless DFN package. The LTC2862 in the SO package is socket compatible with its predecessor, the LT1785.

LTC2863: The LTC2863 is a full-duplex transceiver with separate receive and transmit pins that omits the receiver and driver enable pins in order to fit in an 8-pin package. As a consequence, both the driver and receiver are always enabled and the part has no shutdown mode. Like the LTC2862, it is available in an 8-pin leaded SO package and a small 3mm × 3mm 8-pin leadless DFN package.

LTC2864: The LTC2864 is a full-duplex transceiver with enable pins. It is available in a 14-pin leaded SO package for socket compatibility with the LT1791 as well as a 10-lead 3mm × 3mm DFN package.

LTC2865: The LTC2865 includes the superset of the functionality available in the rest of the family. Like the LTC2864, it offers a full-duplex pinout and adds two additional pins: a VL pin for a logic interface supply voltage and an SLO input pin to select the high speed or slew-limited transmitter mode.

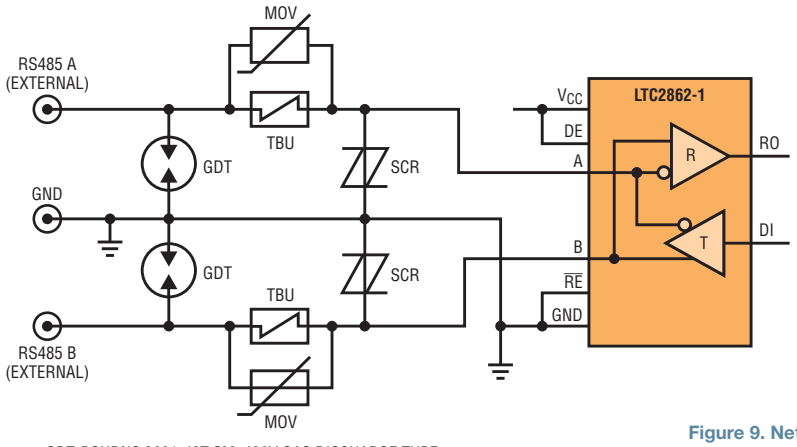
The handling of exposed wires and screw terminals by service personnel introduces the risk of ESD damage, while the possibility of wiring the cables to the wrong screw terminals introduces the risk of overvoltage damage. The high fault voltage and ESD tolerance make the LTC2862–LTC2865 exceptionally resistant to damage from these hazards.

±60V FAULT AND ±15kV ESD TOLERANCE

RS485 wiring connections are often made by connecting the bare twisted wire to screw terminal blocks. The apparatus containing the RS485 interface may house circuits powered by 24V AC/DC or other voltages that are also connected with screw terminals. The handling of exposed wires and screw terminals by service personnel introduces the risk of ESD damage, while the possibility of wiring the cables to the wrong screw terminals introduces the risk of overvoltage damage. The high fault voltage and ESD tolerance make the LTC2862–LTC2865 exceptionally resistant to damage from these hazards.

The ±60V fault protection of the LTC2862–LTC2865 is achieved by using a high voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered-off and high impedance conditions. The driver outputs use a progressive foldback current limit design to protect against overvoltage faults while allowing high current output drive. The LTC2862–LTC2865 are protected from ±60V faults even with GND open, or VCC open or grounded.

The LTC2862–LTC2865 are protected from electrostatic discharge from personnel or equipment up to ±15kV (HBM) to the A, B, Y and Z pins with respect to GND. On-chip protection devices start to conduct at voltages greater than approximately ±78V and conduct the discharge current safely to the GND pin. Furthermore, these devices withstand up to ±15kV discharges even when the part is powered up and operating without latching up. All the other pins are protected to ±8kV (HBM).



GDT: BOURNS 2031-42T-SM; 420V GAS DISCHARGE TUBE
TBU: BOURNS TBU-CA085-300-WH; 850V TRANSIENT BLOCKING UNIT
MOV: BOURNS MOV-7D391K; 390V 25J METAL OXIDE VARISTOR
SCR: BOURNS TISP4P035L1NR-S; 35V BIDIRECTIONAL THYRISTOR

Figure 9. Network for IEC Level 4 protection against surge, EFT and ESD plus ±360V overvoltage protection

EXTENDED PROTECTION AGAINST IEC SURGE, EFT, ESD AND OVERVOLTAGE FAULTS

An RS485 transceiver used in an industrial environment can be exposed to extremely high levels of electrical overstress due to lightning surge, electrical fast transients (EFT) from switching high current inductive loads, and electrostatic discharge (ESD) from electrically charged personnel or equipment. (Test methods for ESD, EFT, and surge are defined in the IEC standards 61000-4-2, 61000-4-4, and 61000-4-5, respectively.)

The transients produced by the surge tests in particular contain much more energy than can be absorbed by the on-chip ESD protection devices of the LTC2862–LTC2865. Therefore, a properly designed external protection network is necessary to achieve a high level of surge protection. An external network can also extend the ESD, EFT and overvoltage performance of the LTC2862–LTC2865 to extremely high levels.

The protection network shown in Figure 9 demonstrates how the high breakdown voltage of the LTC2862–LTC2865 is used to advantage in a protection circuit that meets the highest defined IEC protection levels (Level 4) for surge, EFT and ESD, while extending the overvoltage fault tolerance to ±360V. This protection circuit maintains the ±25V common mode voltage range and adds only ~8pF of capacitance per line (line to GND), thereby providing an extremely high level of protection without impacting the performance of the LTC2862–LTC2865 transceivers.

The gas discharge tubes (GDTs) provide the primary protection against electrical surges. These devices provide a very low impedance and high current

System designers are no longer required to choose between robust fault tolerance or high performance in a RS485 and RS422 transceivers—the LTC2862–LTC2865 transceivers offer both.

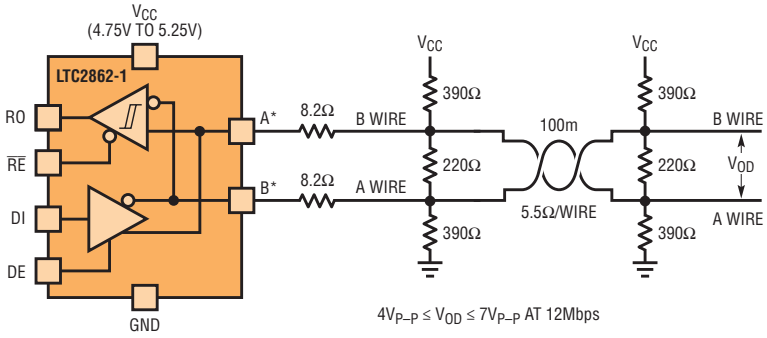


Figure 10. LTC2862-1 PROFIBUS compatible line interface

* THE POLARITY OF A AND B IN THIS DATA SHEET IS OPPOSITE THE POLARITY DEFINED BY PROFIBUS.

carrying capability when they fire, safely discharging the surge current to GND.

The transient blocking units (TBUs) are solid-state devices that switch from a low impedance pass-through state to a high impedance current limiting state when a specified current level is reached. These devices limit the current and power that can pass through to the secondary protection.

The secondary protection consists of a bidirectional thyristor that triggers above 35V to protect the bus pins of the LTC2862–LTC2865 transceiver. The high trigger voltage of the secondary protection maintains the full ±25V common mode voltage range of the receivers.

The final component of the network is the metal oxide varistor (MOV) that clamps the voltage across the TBUs to protect them against fast ESD and EFT transients that exceed the turn-on time of the GDT. The high performance of this network is attributable to the low capacitance of the GDT and thyristor primary and secondary protection devices. The 130pF MOV capacitance floats on the line and is shunted by the TBU, so it contributes no appreciable capacitive load on the signal.

The high breakdown voltage and robustness of the LTC2862–LTC2865 is an essential element of this protection circuit. The ±35V SCR devices used to maintain the common mode voltage range would not protect transceivers with breakdown voltages below ±35V. Furthermore, connecting the MOVs in parallel with the TBUs prevents the MOV capacitance from loading the RS485 bus, but it has the disadvantage of shunting ESD and EFT current through the SCR devices. The resulting voltage drop across the SCR is placed on the bus pins of the transceiver. This unique low capacitance topology can only be used with a robust high voltage transceiver.

USING THE LTC2862 IN PROFIBUS APPLICATIONS

PROFIBUS is an RS485-based field bus with additional requirements for cables, interconnects, line termination, and signal levels. Figure 10 shows the LTC2862-1 in a PROFIBUS network. The following considerations must be followed for full PROFIBUS compliance:

1. Each end of the PROFIBUS line must be terminated with a 220Ω resistor between B and A, a 390Ω pullup resistor between B and V_{CC}, and a 390Ω pulldown resistor between A and GND.
2. 8.2Ω resistors in series with the LTC2862-1 A and B pins are necessary to reduce the peak to peak differential voltage V_{OD} received at the end of a 100m terminated cable to less than 7V per the PROFIBUS standard.
3. The polarity of the PROFIBUS signal is opposite to the polarity convention used in most RS485 transceiver data sheets. Connect pin A to the PROFIBUS B wire (through an 8.2Ω series resistor) and connect pin B to the PROFIBUS A wire (through an 8.2Ω series resistor).
4. Power the LTC2862-1 transceiver with a 5% tolerance 5V supply (4.75V to 5.25V) to ensure that the PROFIBUS VOD tolerances are met.

CONCLUSION

System designers are no longer required to choose between robust fault tolerance or high performance in a RS485 and RS422 transceivers—the LTC2862–LTC2865 transceivers offer both. These transceivers feature ±60V overvoltage and ±15kV ESD tolerance, but also include: operation over 3V to 5.5V supply voltages, up to 20Mbps data rate, ±25V common mode voltage range; selectable slew rate, interface to low voltage logic; and availability in 3mm × 3mm DFN packages. ■