Addressable Bus Buffer Provides Capacitance Buffering, Live Insertion and Nested Addressing in 2-WireBus Systems

by John Ziegler

Introduction

The reliability of data processing, data storage and communications systems depends in part on how well the system is monitored. To this end, input/output (I/O) cards contain circuitry to monitor parameters such as temperature, fan speed and system voltages. These circuits often communicate through 2-wire serial buses, such as SMBus or I^2C.

Several practical problems can occur in these systems, especially as they become large. First, data bus rise time specifications become difficult to meet, as the SDA (serial data) and SCL (serial clock) capacitances of each I/O card add directly to those of the backplane, while the pull-up impedance remains constant. Second, cycling power whenever a new I/O card is installed is not an option in many uninterruptible systems. Third, a device's address is often dictated by the function that it performs. If an existing system already contains a temperature sensor, for example, then inserting a new I/O card with a temperature sensor into the system could result in multiple devices having the same address. Finally, the likelihood of a device becoming confused and holding the bus lines low increases as the number of devices on the bus increases.

The new LTC4302 addressable 2-wire bus buffer addresses all of these problems. The LTC4302 provides a bridge between any two physically separate 2-wire buses. SDAIN and SCLIN connect to one 2-wire bus, e.g., a backplane; and SDAOUT and SCLOUT connect to a second 2-wire bus, e.g. an I/O card. Masters on the buses can command the LTC4302 to connect and disconnect the backplane and card buses through software. By using multiple LTC4302s in a system and connecting and disconnecting them appropriately, users can assign the same address to multiple devices in the system. If a large bus becomes stuck low, the CONN pin of the LTC4302 can be used to isolate portions of the bus, helping the master locate the source of the problem quickly.

When it connects the backplane and card buses, the LTC4302 provides bidirectional buffering, keeping the backplane and card capacitances isolated from each other. Therefore, users can design several LTC4302s into a large system to break its large capacitance into several smaller pieces, while still passing the SDA and SCL signal to all devices at the same time. Finally, because the LTC4302's SDA and SCL pins default to a high impedance state even when no V_{CC} voltage is applied, an LTC4302 can be inserted onto a live 2-wire bus without corrupting it. Two general purpose input-outputs (GPIOs) are available on the LTC4302-1. The LTC4302-2 replaces one GPIO with a second supply voltage V_{CC2}, providing level shifting between systems with different supply voltages.

Circuit Operation

Startup

A block diagram for the LTC4302-1 is shown in Figure 1. During power-up, the LTC4302 starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until the V_{CC} voltage rises above 2.5V (typical). This ensures that the LTC4302 does not try to function until it has sufficient bias voltage. During this time, the 1V pre-charge circuitry is active and forces 1V through 100kΩ nominal resistors to the SDA and SCL pins. The 1V pre-charge minimizes the disturbance caused by the LTC4302's SDA and SCL pins in hot-swapping applications. When the LTC4302 is being inserted into a live backplane, the backplane SDA and SCL bus voltages may be anywhere from 0V to the bus pull-up supply voltage. Pre-charging the SDA and SCL pins to 1V minimizes the worst-case backplane-to-pin voltage differential at the moment of connection, thus minimizing the amount of disturbance on the backplane.

Once the LTC4302 comes out of undervoltage lockout, the pre-charge circuitry is shut off, and the 2-Wire Digital Interface circuitry (shown in Figure 1) is activated. The master on SDAIN and SCLIN can then address the LTC4302 and utilize its various features, which include the Backplane-to-Card Connection circuitry (also referred to below as "Connection Circuitry"), Rise Time Accelerators, and GPIO circuits. These features default to a high-impedance state: the Connection Circuitry and Rise Time Accelerators are inactive, and the GPIOs are in open-drain output mode with their pull-down devices turned off. The LTC4302 is in the default state whenever it is in UVLO or when the CONN voltage is low.

Connection Circuitry

When the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pins being low. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT turn their pull-downs off. The same is true for SCLIN and SCLOUT.

This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of how the devices in the system are connected to the LTC4302.

Another key feature of the connection circuitry is that, while it joins the two buses together, it still maintains electrical isolation between them, thus providing capacitance buffering for both sides. This means that devices on the backplane must drive only the backplane capacitance plus the low capacitance of the LTC4302 (around 10pF). The LTC4302 drives the capacitance of the rest of the I/O card. Likewise, devices on the card must only drive the capacitance of the card plus the low capacitance of the LTC4302. The LTC4302 drives the capacitance on the backplane. The LTC4302 is capable of driving capacitive loads ranging from 0pF to 1000pF on all of its data and clock pins.

Rise Time Accelerators

Masters on the bus may activate rise time accelerators on the backplane side (SDAIN and SCLIN), the card side (SDAOUT and SCLOUT), neither or both. When activated, the accelerators switch in 2mA of pull-up current at V_{CC} = 2.7V and 9mA at V_{CC} = 5.5V during bus rising edges to quickly slew the SDA and SCL lines once their DC voltages exceed 0.6V and the initial rise rate on the pin exceeds 0.8V/µs. Figure 2 shows the rise time reduc-

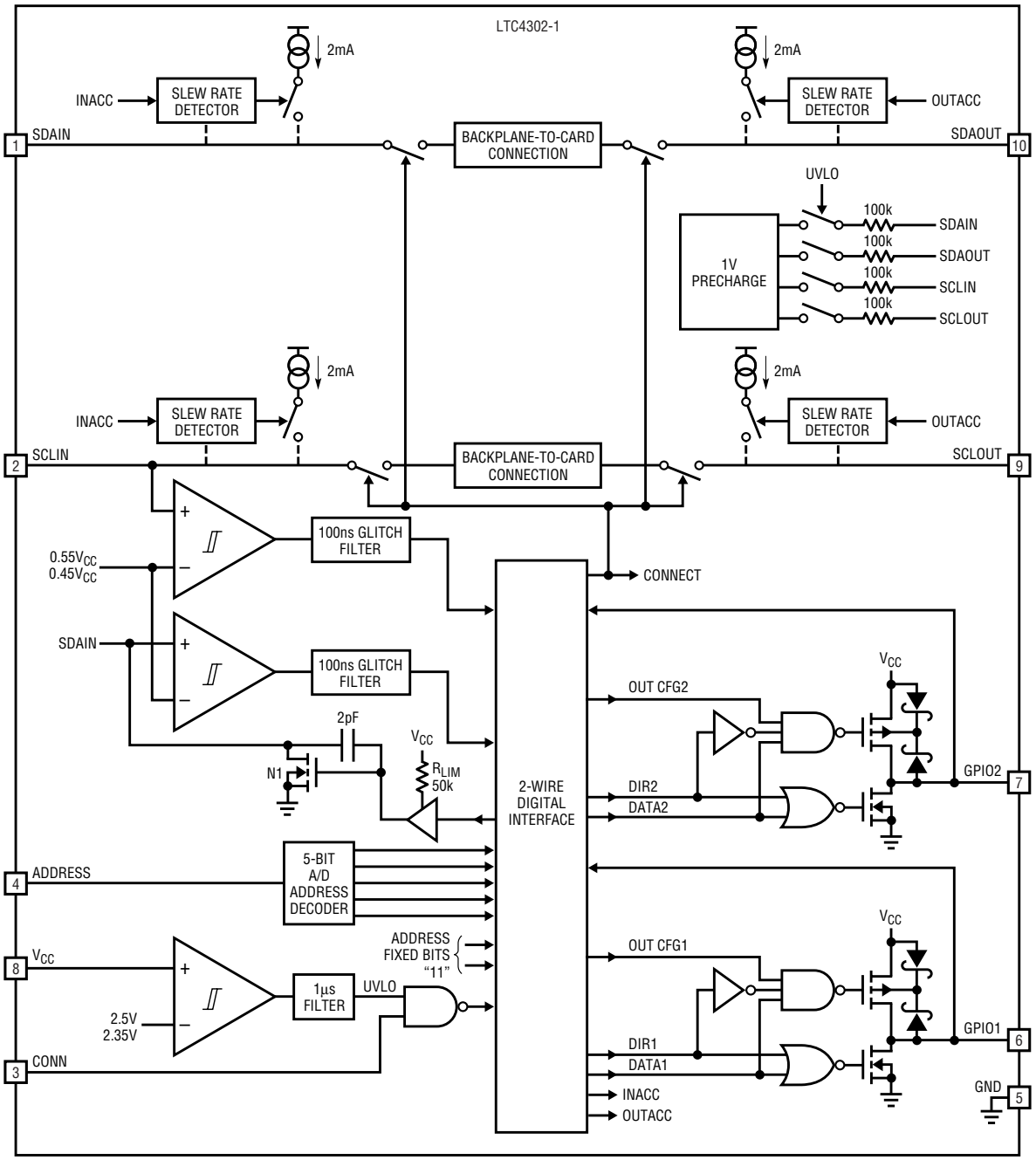
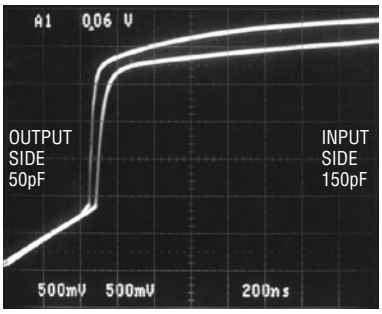


Figure 1. Addressable 2-wire bus buffer block diagram



200ns/DIV

Figure 2. Rise time accelerators reduce rise time for C_{BUS} = 50pF, C_{BUS} = 150pF.

tion achieved for V_{CC} = 3.3V and bus equivalent capacitances of 50pF and 150pF.

General Purpose Input/Outputs (GPIOs)

The LTC4302 -1 provides two GPIOs that can be configured as input, open-drain outputs, or push-pull outputs. In push-pull mode, at V_{CC} = 2.7V, the typical pull-up impedance is 670Ω and the typical pull-down impedance is 35Ω, making the GPIO pull-downs capable of driving LEDs. In open-drain output mode, the logic high is provided by connecting a pull-up resistor from the GPIO pin to an external supply voltage. This supply voltage can range from 2.2V to 5.5V, independent of the V_{CC} voltage. The LTC4302-2 replaces one GPIO with a second supply voltage pin V_{CC2} and therefore provides a single GPIO.

Single ADDRESS Pin Provides 32 Addresses

The LTC4302 saves valuable board space by providing 32 unique addresses from a single ADDRESS pin. A resistive divider between V_{CC} and ground sets an analog voltage on the ADDRESS pin. An internal A/D converter translates the ADDRESS voltage into a 5-bit digital word, which sets the five LSBs of the address. The two MSBs are hard-wired to "11."

CONN Reset Pin

Grounding the CONN pin resets the LTC4302 to its high-impedance default state: the output side is disconnected from the input side, the rise time accelerators on both sides are disabled, and the GPIOs are set in open-drain output mode with the NMOS open-drain pulldown turned off. Grounding the CONN pin also disables the 2-Wire Digital Interface circuitry, preventing masters on the bus from communicating with the LTC4302. When the CONN voltage is brought back high, the LTC4302 remains in its default state.

When an SDA or SCL line is stuck low, masters can use the CONN pins of the LTC4302s in the system to find the source of the problem. A master drives one CONN pin low at a time while monitoring the stuck bus. When the line returns high, the master then knows that the stuck device is on the other side of the last LTC4302 whose CONN pin was driven low.

Live Insertion and Removal, and Capacitance Buffering Application

The application shown in Figure 3 highlights the live insertion and removal, and the capacitance buffering features of the LTC4302. Assuming that a staggered connector is available, make ground and V_{CC} the longest pins to guarantee that SDAIN and SCLIN receive the 1V pre-charge voltage before they connect. Make SDAIN and SCLIN medium length pins to ensure that they are firmly connected while CONN is low. Make CONN the shortest pin and connect a weak resistor from CONN to ground on the I/O card. This ensures that the LTC4302 remains in a high impedance state while SDAIN and SCLIN are making connection during live insertion. During live removal, having CONN disconnect first ensures that the LTC4302 enters a high impedance state in a controlled manner before SDAIN and SCLIN disconnect.

Note that if the I/O card were plugged directly into the backplane, the card capacitance would add directly to the backplane capacitance, making rise and fall time requirements difficult to meet. Inserting a LTC4302 on the edge of the card, however, isolates the card capacitance from the backplane. The LTC4302 drives the capacitance of everything on the card, and the backplane must drive only the capacitance of the LTC4302, which is less than 10pF. As more I/O cards are added and the system grows, placing a LTC4302 on the edge of each

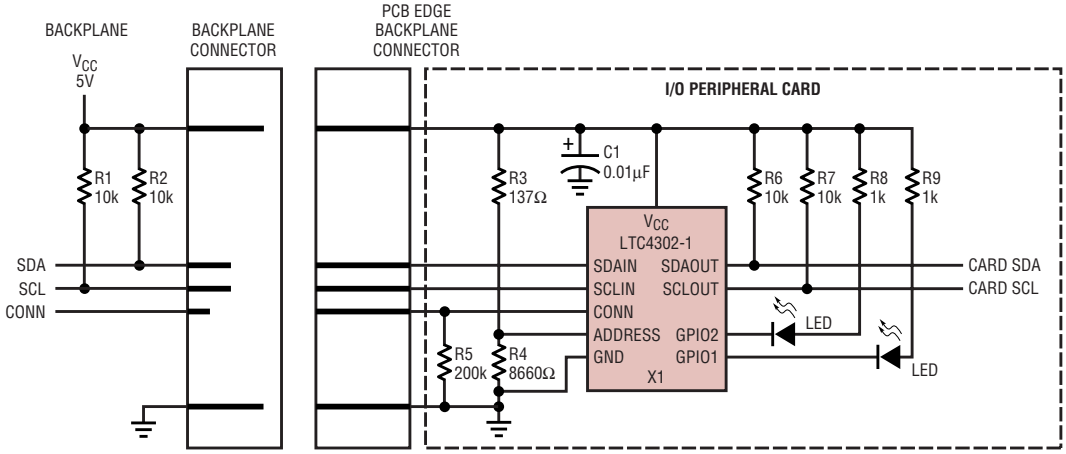


Figure 3. LTC4302-1 in a live insertion and capacitance buffering application

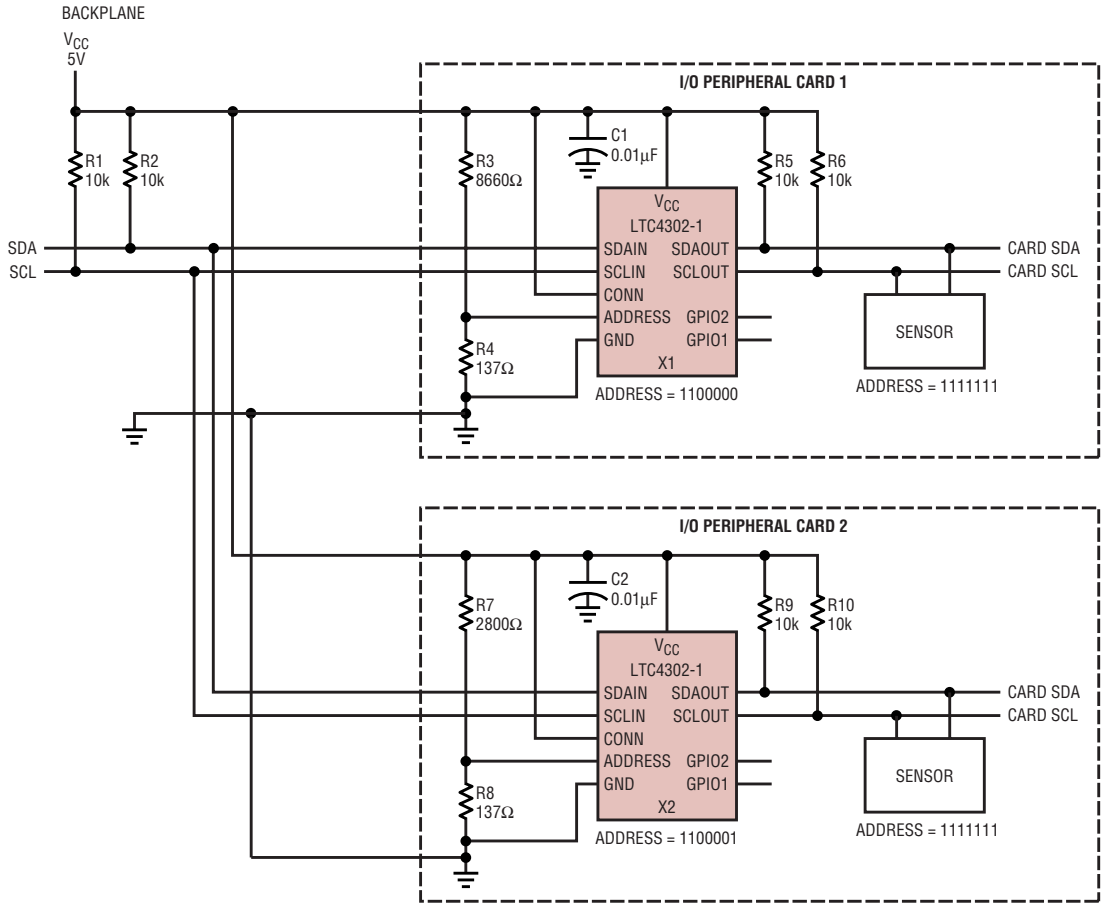


Figure 4. LTC4302-1 in a nested addressing application

card breaks what would be one large, unmanageable bus into several manageable segments, while still allowing all segments to be active at the same time. Moreover, the LTC4302's rise time accelerators provide strong pull-up currents during bus rising edges, so that even heavily loaded bus lines meet system rise time requirements with ease.

Address Expansion with Nested Addressing

Figure 4 illustrates how the LTC4302 can be used to expand the number of devices in a system by using nested addressing. Note that each I/O card contains a sensor device having address 1111111. If the two cards were plugged directly into the backplane, the two sensors would require two different addresses. However, each LTC4302 isolates the devices on its card from the rest of the system until it is commanded to connect. If masters use the LTC4302s to connect only one I/O card at a time, then each I/O card can have a device with address 1111111 and no problems occur.

5.5V to 3V Level Translator and Power Supply Redundancy (LTC4302-2)

Systems requiring different supply voltages for the backplane side and the card side can use the LTC4302-2 as shown in Figure 5. The pull-up resistors on the card side connect from SDAOUT and SCLOUT to V_{CC2}, and those on the backplane side connect from SDAIN and SCLIN to V_{CC}. The LTC4302-2 functions for voltages ranging from 2.7V to 5.5V on both V_{CC} and V_{CC2}. There is no constraint on the voltage magnitudes of V_{CC} and V_{CC2} with respect to each other.

This application also provides power supply redundancy. If either the V_{CC} or V_{CC2} supply voltage falls below its UVLO threshold, the LTC4302-2 disconnects the backplane from the card, so that the side that is still powered can continue to function.

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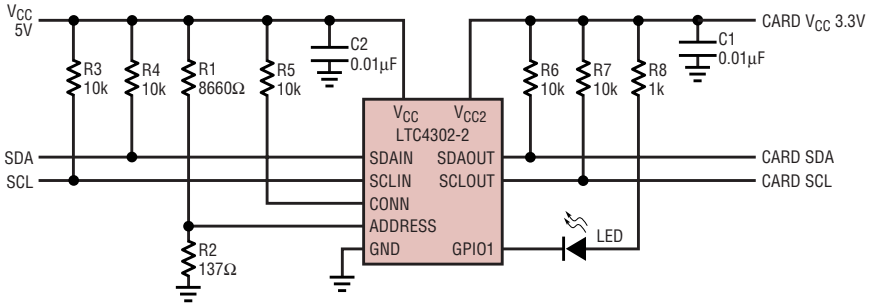

Figure 5. 5V to 3.3V level translator application

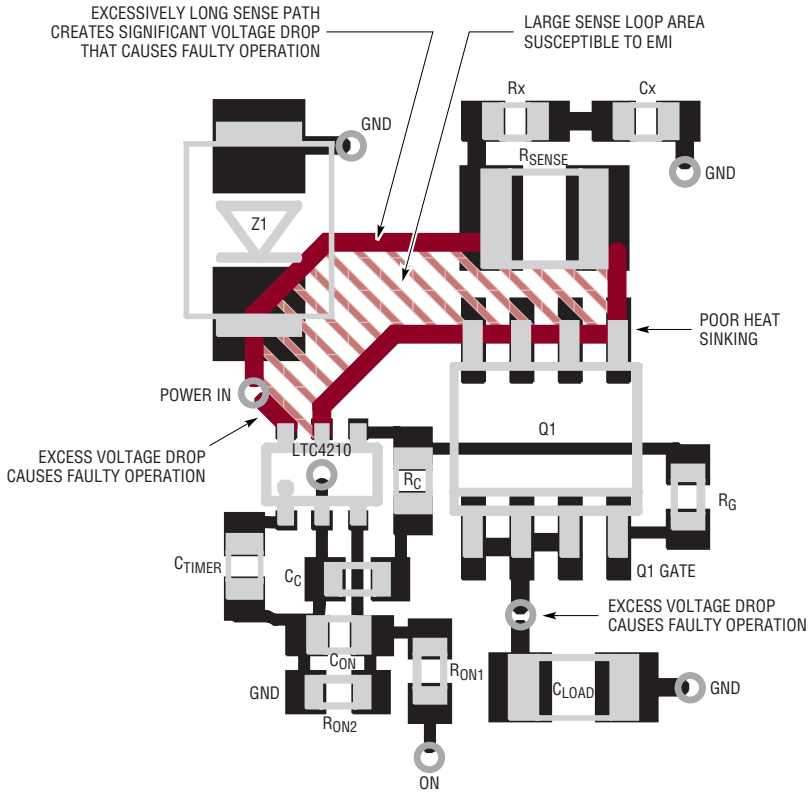

Figure 3. Example of layout that can reduce the accuracy of Kelvin sensing. The problems shown here include: excess length of thin high resistance track in series with sense resistor, inadequate heat sinking on Q1, and an insufficient number of vias for input power and output load connections.

resistors. The use of a 4-terminal resistor forces the auto router to make a correct Kelvin connection to the current sense resistor. But this alone is not enough. High speed switch mode power supplies have a high dI/dt path that can inductively couple with the sense loop and also cause malfunction. To minimize inductive coupling, the Kelvin sense circuit must exhibit minimal loop area.

Setting the Proper Constraints in an Auto-Router

Set the auto-router constraints to route the Kelvin sense connections as a differential pair to keep the connections side by side and close together. Use maximum length constraints to prevent the connections from wandering too far from the direct path. Constrain the connection to the component layer on a multi-layer PC board to prevent unwanted vias in this critical connection path. Although the proper choice of sense resistor and layout constraints can mitigate many of the PCB layout pitfalls, in the end it's up to the designer to carefully check the layout.

Notes

[1] Some sources of 4-terminal Kelvin sensed resistors include:
- www.Caddock.com
- www.IMS-Resistors.com
- www.IRCtt.com
- www.Vishay.com

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that power is delivered when diagonal switches are on. It differs in that during the free-wheeling portion of the switching cycle, either the top or bottom switches of the bridge remain on. This provides for recovery of parasitic energy and zero-voltage turn-on transitions for the primary switches. The LTC3722-1 can be configured to provide adaptive (with programmable time-out) or fixed delay control for zero voltage switching operation. In adaptive DirectSense™ mode, the turn-on timing adjusts automatically by sensing the transition voltages on the bridge legs, eliminating external trims. This provides accurate zero voltage transition timing with changes in input voltage, output load and circuit parasitics. Fixed (or manual) delay control is also available, which allows for fixed transition delays or even custom dynamic timing schemes. The LTC3722-1 also features adjustable synchronous rectifier timing.

Conclusion

The new LTC3722-1 current-mode controller provides a wealth of features targeted at high power isolated full bridge applications, including flexible timing control, synchronous rectifier outputs, under-voltage lockout, programmable slope compensation and current mode leading edge blanking.

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Summary

The LTC4302-1/LTC4302-2 addressable 2-wire bus buffers ease the practical issues associated with complex 2-wire bus systems. They allow I/O cards to be hot-plugged into live systems and break one large capacitive bus into several smaller ones, while still passing the SDA and SCL signals to every device in the system. They can also connect and disconnect different bus segments at different times, providing nested addressing capability and easing the debugging process during stuck low situations.