−48V Hot Swap Controller Offers Comprehensive Protection for Telecom Systems

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Introduction

High performance, high reliability telecom systems employ distributed power modules to generate low voltage, high current supplies from a −48V bus. These systems require that the individual power modules are hot swappable—they can be inserted and removed at any time without affecting the operation of the main system. Another requirement is that failed elements self-isolate without affecting neighboring elements. The system controller takes notice of any failures and reconfigures the system so

that there is no interruption of service. The system controller also signals for service, providing failed board identification and diagnostic details. In order to perform these tasks effectively, the

Figure 1. Basic LTC4251 Family Hot Swap Topology

system controller requires a solid first line of defense, specifically a Hot Swap™ controller on the front end of each and every card.

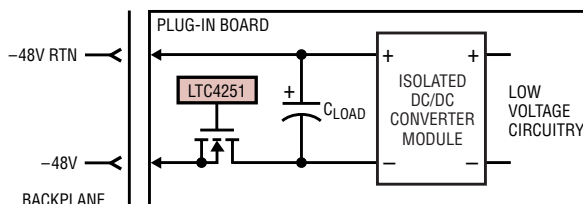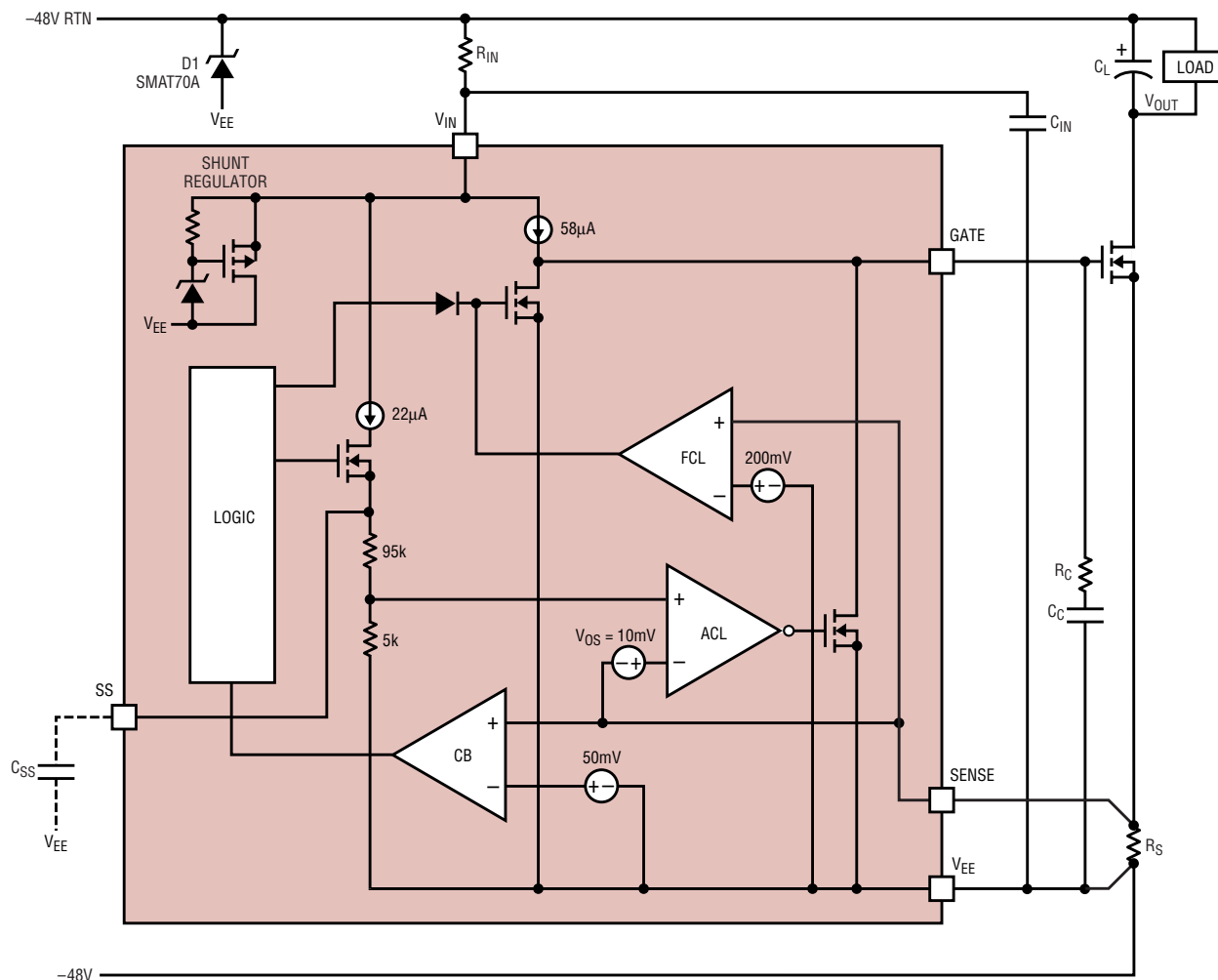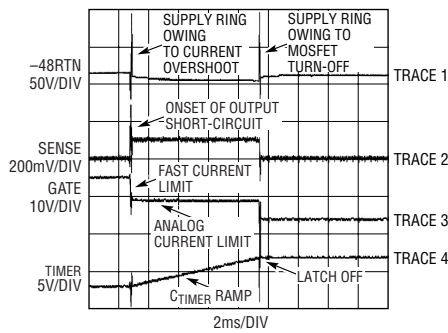Figure 2. Low-side MOSFET Hot Swap scheme

Figure 3. Output short-circuit behavior

The new LTC4251, LTC4252 and LTC4253 Hot Swap controllers offer comprehensive circuit protection for –48V applications (and higher) through three stages of current control. They protect the system bus from hot swapped power modules and they protect the power modules from glitches on the system bus. These devices are available in a variety of configurations to fill almost any application need.

Figure 1 shows the major elements of a hot swappable power module. During insertion or commutation of a short circuit fault, the power supply bus can ring to more than twice its nominal supply voltage, easily exceeding the absolute maximum supply rating of most devices. The LTC4251 family uses a floating supply topology with a low side MOSFET drive and a shunt regulator to solve this problem. Thus, operation is limited only by MOSFET voltage and current ratings.

The MOSFETs in Hot Swap circuits are fully enhanced to achieve the lowest on resistance in normal operation. A low resistance MOSFET is chosen
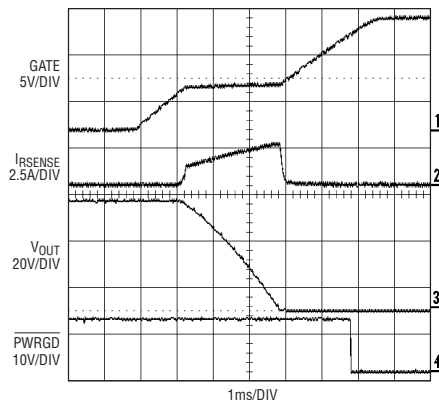

Figure 5. LTC4252 start-up behavior

because of its low insertion loss and the fact that it does not require a heat-sink. The problem is that with a low impedance load fault, huge currents are drawn from the bus, which in turn collapses the bus voltage. Neighboring boards see the loss of bus supply and may reset or fail if the voltage dip lasts too long.

3 Stages of Current Control

The LTC4251 family employs three stages of current limiting to protect the MOSFET and minimize bus disturbances:
❏ A timed circuit breaker
❏ Active current limiting
❏ Fast feedforward path that limits peak current under worst-case catastrophic fault conditions

The LTC4251 family isolates major faults with the fast current limit comparator, FCL as shown in Figure 2. When the SENSE voltage across the current sensing resistor, R_{SENSE} exceeds four times the circuit breaker limit of 50mV, the gate of the external MOSFET is immediately discharged. When the fast comparator no longer detects the excessive sense current, it releases the GATE. Charge
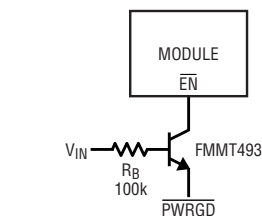

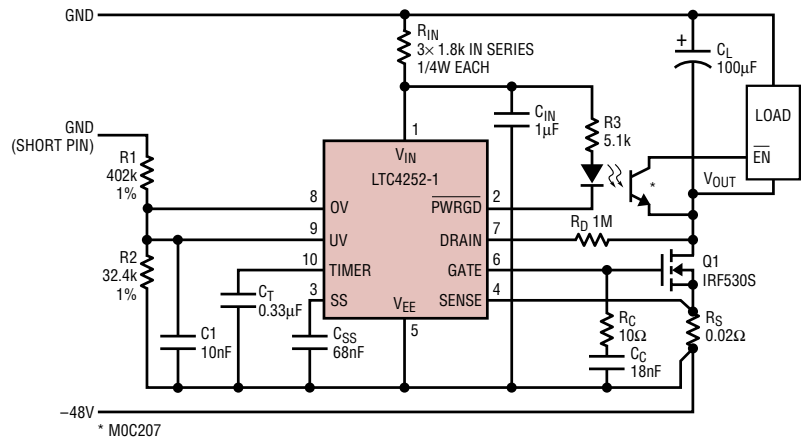**Figure 6. NPN interface between $\overline{PWRGD}$ and module**

Figure 4. –48V/2.5A LTC4252-1 Hot Swap controller

stored in the compensation capacitor recharges the GATE while the analog current limit amplifier (ACL) swings in to regulate the sense current to approximately twice the circuit breaker current limit.

With such a fault, the bus voltage collapses at first but quickly recovers when the MOSFET limits the current and isolates the fault. Stray bus lead inductance glitches are clamped by the transient suppressor diode, D1 before reaching MOSFET breakdown voltage. Without D1, the glitch avalanches the MOSFET, interfering with the analog current limit loop.

Figure 3 shows the waveform for a short circuit failure in the power module. The –48VRTN sags a little due to the bus supply load regulation. The SENSE pin voltage briefly peaks to more than four times the circuit breaker voltage at the onset of the fault, but quickly drops to twice the circuit breaker voltage during analog current limiting. The GATE pin is ripped downwards by the fast comparator with a slight voltage undershoot. The undershoot is corrected by the charge from the compensation capacitor C_C. During this fault interval, the circuit breaker comparator (CB) sets the TIMER pin to charge up. When the circuit breaker timer trips, the GATE pin is pulled down, shutting down the MOSFET before it exceeds its safe operating area. The benefit of fast current limiting is obvious from the very short disturbance on the bus supply not causing a circuit breaker trip.
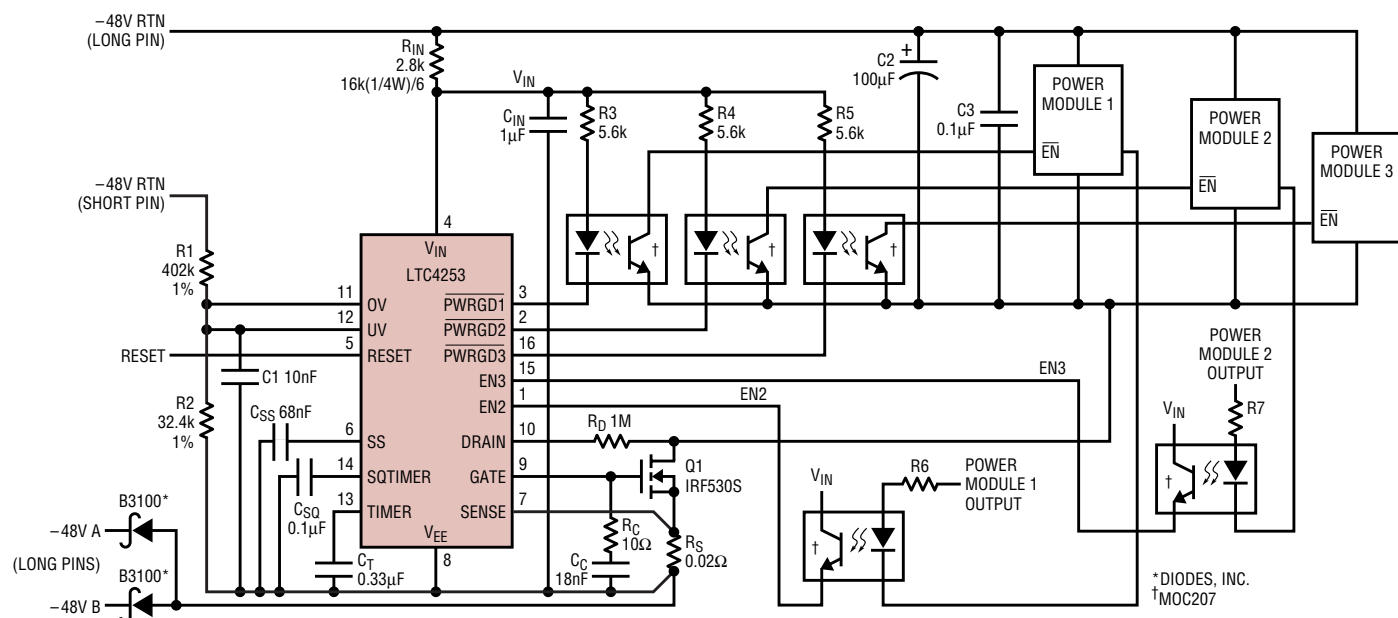
Figure 7. –48V/2.5A Hot Swap sequence controller

Latchoff vs Auto-Retry

When a timed circuit breaker fault occurs, the devices in the LTC4251 family (except the LTC4252-2) latch off and wait for service. The fault latch can be reset by an external pull down device at the TIMER or UV pin. In the LTC4252-2, the TIMER pin starts a retry sequence after allowing a programmable time for the MOSFET to cool.

Floating Shunt Regulator

LTC4251 family uses a simple, fast-responding shunt regulator that floats at the negative bus terminal. This allows the Hot Swap controller, in theory, to adapt to any power supply bus of –24V or more. Wide range supplies, such as those encountered in the telecom world

are easily handled by the LTC4251 family's 15:1 shunt current range. Even more dynamic range is available on a transient basis—a guaranteed 50:1 over the operating current—so that the device can operate without interruption in a noisy, spike-ridden environment.

Start-Up Behavior

The current limiting feature of the LTC4251, LTC4252 and LTC4253 makes soft-start (output load voltage ramping) less essential than it would be in a non-current-limiting circuit. Nevertheless, the LTC4252 and LTC4253 offer a current soft-start pin that acts as the reference for the analog current limit amplifier. By attaching a capacitor, the sense

current can be modulated at start-up. Figure 5 shows the start-up behavior of the circuit shown in Figure 4.

Undervoltage and Overvoltage Detectors

Programmable undervoltage (UV) and overvoltage (OV) detectors disconnect the load whenever the input supply exceeds the desired operating range. The UV detector enables the device to function above a preset threshold while the OV detector disables the chip above a preset threshold. The LTC4251 (except the LTC4251-2) and LTC4252 MS8 have a single pin with both UV and OV detect function. The external resistor divider (R1 and R2) sets the standard telecom operating range. The LTC4252 MS10 and LTC4253 have separate pins for UV and OV so they can be independently programmed. Separate UV and OV pins allow other user programmable settings. LTC4251-2 has its OV function internally disabled.

Timer with Drain Voltage Accelerated Response

A multifunction timer delays the initial start-up from undervoltage input or internal undervoltage lockout, controls the circuit breaker response time, and controls shutdown cooling timing for LTC4252-2 in auto-retry mode. The
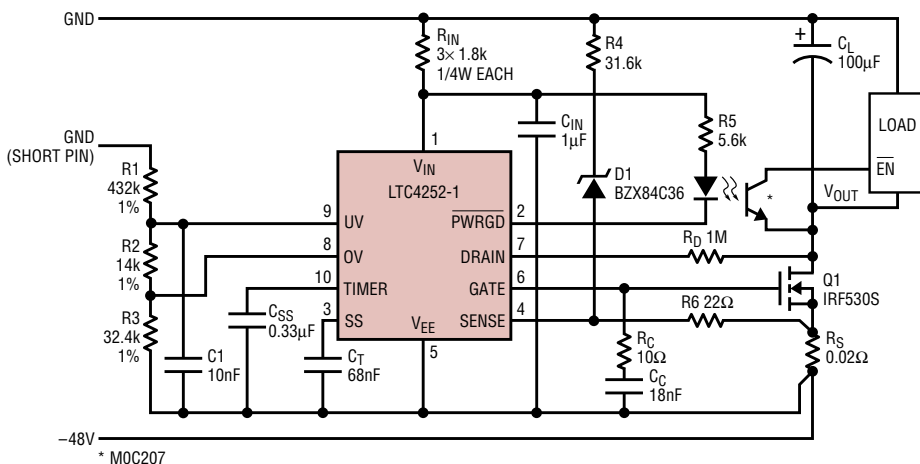
Figure 8. Power limit circuit breaking application

initial start-up delay allows time for the board supply voltage to stabilize at plug-in, before activating the MOSFET. The circuit breaker response is set within the safe operating area (SOA) of the MOSFET at worst-case operating voltage and analog limit current. The shutdown cooling period is approximately 5.25 times the initial timing duration.

For the LTC4252-2 in continuous auto-retry, the MOSFET operating temperature will rise above ambient temperature, and the time to SOA limit must be adjusted accordingly. For both the LTC4252 and LTC4253, a resistor, R_D, can be connected between DRAIN pin and the drain of the MOSFET to reduce the current limit period when a high V_{DS} condition is present. The current flowing into the DRAIN pin effectively senses the MOSFET drain source voltage. This DRAIN pin current is amplified eight times and added to the circuit breaker timer pull-up current, accelerating the response. If the worst case is used to determine SOA limit with drain-accelerated current, the timer response at mild overload without drain-accelerated current is now longer and less sensitive. For the LTC4251, there is no DRAIN input pin, the worst case operating voltage is used to set the circuit breaker response.

Power Good and Sequencer

LTC4252 has an open-collector Power Good status pin that can drive an optocoupler or an NPN to enable the power module. This pin is pulled low after the MOSFET is driven to full enhancement, indicating a successful power-up. The opto-coupler interface takes care of the common-mode voltage difference between the Hot Swap controller and the power module. Figure 6 shows an NPN configuration for $\overline{PWRGD}$ interface.

The LTC4253 has three sequenced $\overline{PWRGD}$ outputs and two enable (EN) inputs allowing three modules be sequenced as shown in Figure 7. The LTC4253 allows up to three power modules be turn on sequentially, minimizing the power demand on the –48V bus. When the first module turns on, it signals via the EN input to enable the second module. The minimum sequence interval between each module is set by a capacitor at SQTIMER pin.

Power Limited Circuit Breaker

In applications where timed power limit is preferred over current limit, Figure 8 shows how to create a power limited circuit breaker by tying the current limit to the supply voltage via Zener diode D1, and resistors R4 and R6. Limiting by power permits the control of equipment heat dissipation or power allocation.

Conclusion

This new family of devices offers comprehensive solutions to –48V Hot Swap applications. Higher voltage applications are also supported to the limits of the MOSFET. These devices are rugged and capable of handling large transients from catastrophic failures as well as neighboring board failures that cause large return currents. The LTC4251 is available in SOT-23 with two different UV and OV threshold combinations and one version without an OV threshold. The LTC4252 is available in 8-pin and 10-pin MS packages with latch-off mode and auto-retry. The LTC4253 is available in a 16-pin SSOP package, and also features a latchoff version. ⌁