High Performance 3-Phase Power Supplies Yields High Efficiency over the Entire CPU Load Range

by Wei Chen and Steve Hobrecht

Introduction

Thermal stress is a major concern for enterprise CPUs that frequently draw up to 100A of load current. PolyPhase® switching DC/DC converters reduce thermal stress by providing high efficiency at heavy loads, and thus have become the standard power supply solution for high powered CPUs. PolyPhase switchers are also finding their way into mobile applications where CPUs are drawing currents greater than 30A, and will draw 65A in the near future. Mobile CPUs pose an additional problem, though. They spend much of the time in sleep or standby modes, meaning that *light load* efficiency is important to maximize battery run-time. Traditional PolyPhase converters, despite their exceptional performance at heavy load, are not as efficient at light load.

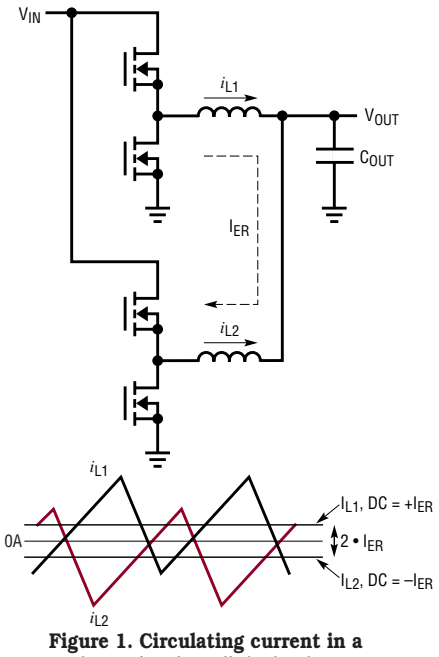


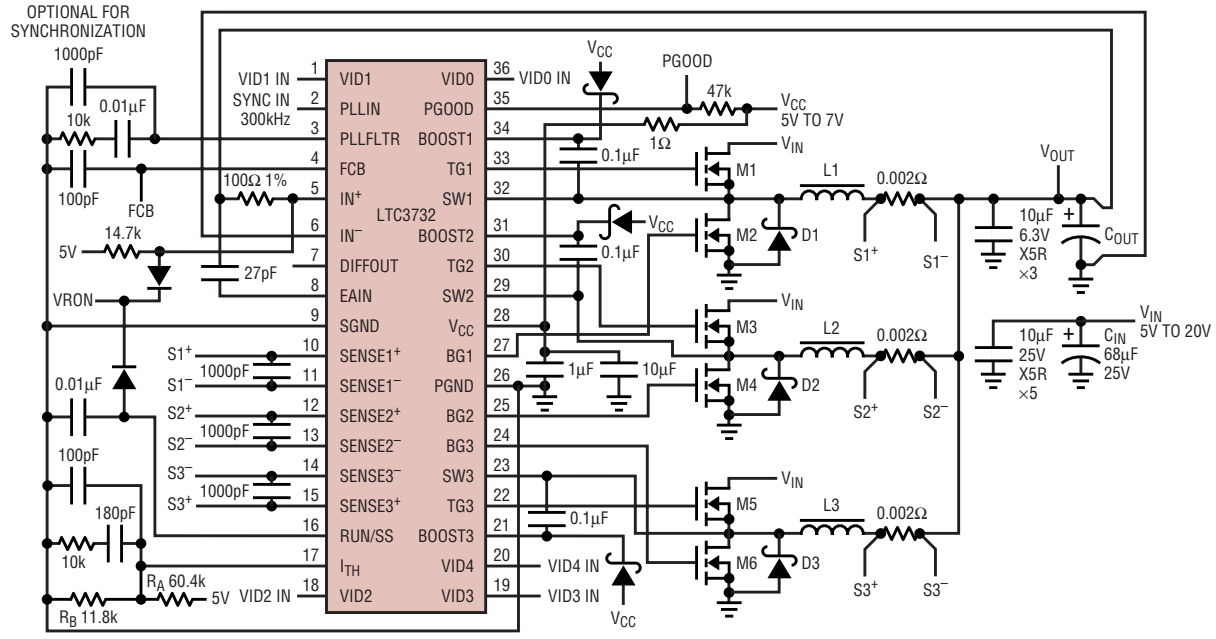
Figure 1. Circulating current in a 2-phase circuit at light load

The LTC3730, LTC3731 and LTC3732 family of PolyPhase controllers are efficient at both heavy and light CPU loads, making these new controllers a good match for high performance notebook computer applications.

This high efficiency at light loads is a result of a new Stage Shedding™ feature, which significantly reduces conduction switching losses.

These new controllers have other important features that make them a good choice for mobile CPU applications:

- ❑ True remote sensing on both the positive and negative output rails to ensure tight output regulation at high output currents;
- ❑ Kelvin sensing (positive and negative) on the pads of each current sense resistor to achieve accurate



VIN: 3.3V TO 20V
VOUT: 1.1V TO 1.85V, 60A
fSW: 300kHz
CIN: SANYO OS-CON 25SP68M (619) 661-6835
COUT: 330µF/2.5V ×10 SANYO POSCAP 2RSTPE330MC
D1 TO D3: B340A

L1 TO L3: 0.8µH SUMIDA CEP125-0R8 (847) 956-0667
M1, M3, M5: IR IRF7811W (310) 322-3331
OR FAIRCHILD FDS6688 (408) 822-2126
OR SILICONIX Si7860DP (800) 554-5565
M2, M4, M6: IR IRF7822 ×2
OR SILICONIX Si7856DP ×2

Figure 2. Schematic diagram of a 3-phase 65A VRM9.x power supply

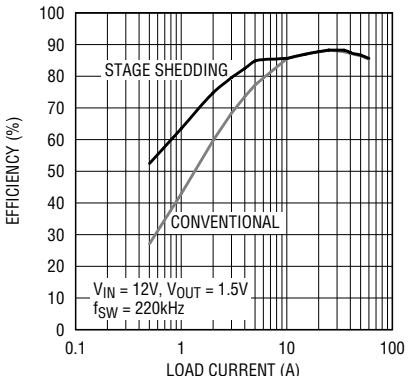


Figure 3. Measured efficiencies of Stage Shedding operation and conventional operation for the VRM9 design

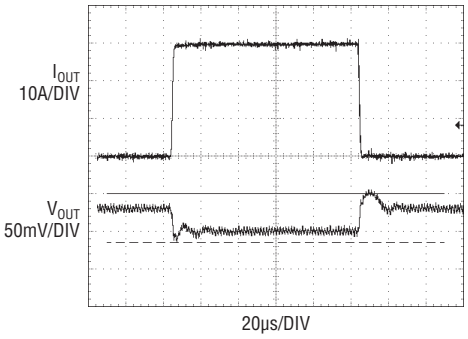


Figure 4. Load transient waveforms for the VRM9.1 design

current sharing, even if the layout of parallel power stages is not symmetrical;

- ❑ All controllers feature integrated high current MOSFET drivers for up to 600kHz switching frequency, thus minimizing the overall power supply size and component count.

LTC3731 is a versatile 3-phase controller that generates a 30 or 60 degree clock output based on the voltage level of the PHASMD pin. This feature allows several LTC3731s to be paralleled for up to 12-phase operation. The 0.6V to 6V output voltage is programmed by an external resistor divider. The LTC3730 is a dedicated 3-phase controller with 5-bit VID output programming that is compatible with IMVP2 and IMVP3 requirements. The internal op amp can be used to program voltage offsets for different CPU operation modes. This controller is suitable for powering Intel mobile Northwood CPUs. The LTC3732 is another 3-phase controller with a 5-bit VID output programming that is compatible with VRM9.x specs. This controller is suitable for powering Intel desktop Pentium 4 (P4) CPUs in a so called DeskNote PC or Transportable PC design. A DeskNote PC uses the desktop CPU in a notebook computer design to simultaneously achieve high performance and low cost. All three controllers are available in space saving SSOP36 packages, while the LTC3731 is also available in the much smaller, and thermally enhanced, 5mm × 5mm QFN package.

Stage Shedding Operation Improves Efficiency at Light Loads

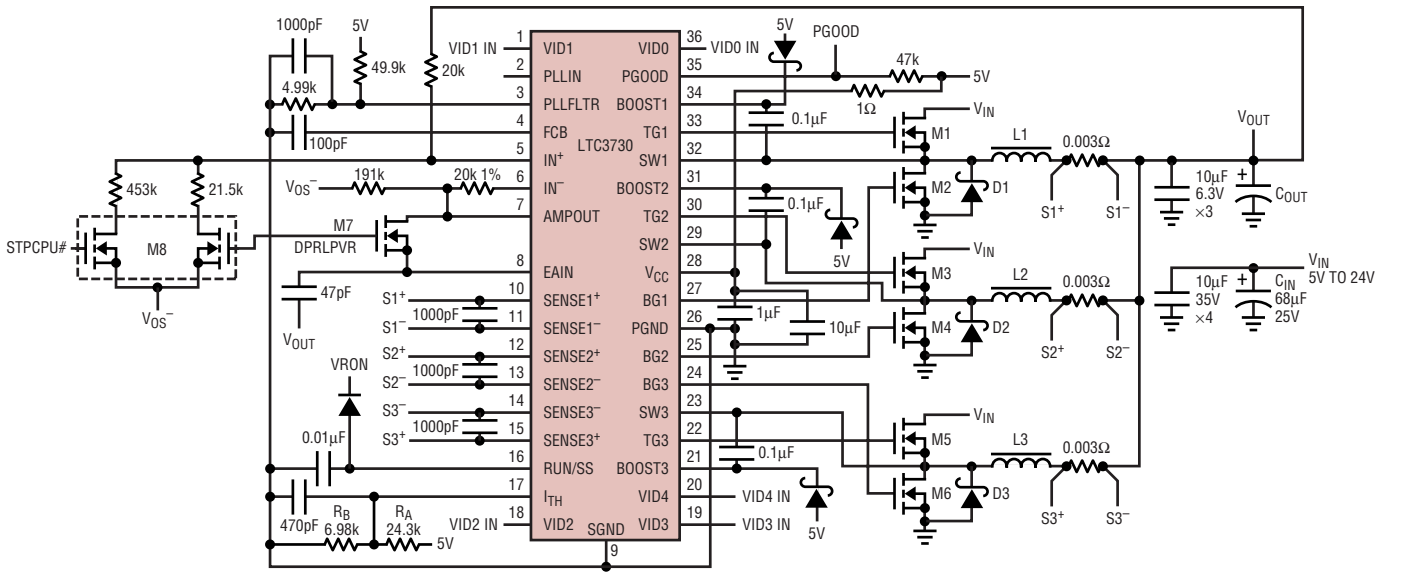
There are three main obstacles to obtaining high efficiency at light loads with a PolyPhase converter:

- ❑ Switching related losses
- ❑ Extra conduction losses induced by circulating currents
- ❑ IC bias losses

The first two obstacles, described below, are reduced by the Stage Shedding feature. The IC bias losses can be reduced by enabling Burst Mode® operation.

Light Load Efficiency Obstacle 1: Switching-Related Power Losses

In high current applications, low $R_{DS(ON)}$ MOSFETs are typically chosen to minimize conduction losses at full loads. At light loads, though, the high gate charge and parasitic capacitance of these MOSFETs often cause significant power losses associated with gate driving and switching. Also, the core loses of inductors dominate the overall inductor power losses at light loads. Since the switching losses, gate driving losses, and inductor core losses do not decrease with load currents, light load efficiency suffers.



VOUT: 0.6V TO 1.75V, 45A
SWITCHING FREQUENCY: 300kHz
CIN: SANYO OS-CON 25SP68M
COUT: 270µF/2V ×4 PANASONIC SP EEFSD0D271R

D1 TO D3: B140A DIODES INC
L1 TO L3: SUMIDA 1µH/20A CEP125 IROMC-H OR 1µH/19A PANASONIC PCC-D126H OR TOKO EH125C

M1, M3, M5: IR IRF7811W OR FAIRCHILD FDS6688 OR SILICONIX Si7860DP
M2, M4, M6: IR IRF7811X2 OR SILICONIX Si7856DP
M7: 1/2 SILICONIX Si1034X
M8: SILICONIX Si1034X

Figure 5. IMVP3 compatible, 45A, 3-phase power supply

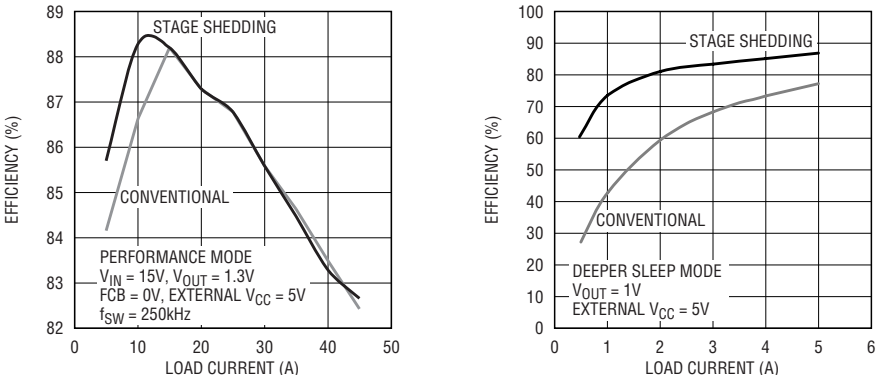


Figure 6. Measured efficiencies of Stage Shedding operation and conventional operation for the 3-phase IMVP3 power supply

Light Load Efficiency Obstacle 2: Circulating Currents

In a PolyPhase synchronous buck converter, the inductor current in each synchronous buck stage is allowed to reverse at light loads due to synchronous rectification. In a practical PolyPhase design, a current sharing error always exists because of tolerances in the sense resistors and slight mismatches between paralleled channels within the controllers. Any current sharing error among the paralleled stages introduces circulating currents that result in additional power losses. As shown in Figure 1, for example, if the current difference between two paralleled channels is 2A (I_{ER}=1A), one channel (Channel 1) will source 1A and the other channel (Channel 2) will sink 1A at no load conditions. Since this 1A current circulates between two channels instead of flowing toward the output, this current introduces unnecessary power losses. Therefore, the circulating current must be minimized to improve light load efficiency in a PolyPhase converter.

The Solution: Stage Shedding Operation

A simple solution is to turn off the bottom FET when the inductor current starts to reverse. This is called pulse skipping in most LTC controllers. This scheme significantly reduces the reverse current. However, an accurate detection of inductor current zero-cross and an immediate turn-off of the bottom FETs are difficult to achieve. A more effective scheme, as implemented in new 3-phase controllers, is the Stage Shedding technique. At light loads, the controllers automatically shut down all but one channel. This scheme completely eliminates the circulating currents and related power losses. Furthermore, Stage Shedding eliminates the gate drive losses, MOSFET switching losses, and inductor core losses of the unused channels. Thus the Stage Shedding technique decreases the conduction losses and switching losses significantly at light loads, resulting in a much higher efficiency at light loads. Since the controller maintains the original regulation loop, Stage Shedding has no effect on output regulation accuracy.

Burst Mode Operation Minimizes Obstacle 3: IC Bias Losses

To further minimize the IC bias losses and switching losses at no load conditions, Burst Mode operation can be enabled by applying a voltage between 0.6V and (V_{CC} – 1V) to the FCB pin.

3-Phase, High Efficiency 65A VRM9.x Power Supply for Pentium 4 CPU

Figure 2 shows a 3-phase VRM9.x power supply for a Pentium® 4 CPU. It uses the LTC3732 to drive nine small PowerPak SO-8 MOSFETs for 65A output current. To provide higher output currents, simply use lower $R_{DS(ON)}$ MOSFETs and higher current rated inductors. R_A and R_B implement a lossless active voltage positioning (AVP) technique to minimize the output capacitor size. For more detailed technical information about AVP see the LTC1736 data sheet or Design Solution 224. Figure 3 shows the measured efficiency under different load conditions. In this case the input is 12V, the output voltage is 1.5V and the switching frequency is 220kHz. The efficiencies are measured for both Stage Shedding operation and for conventional PolyPhase operation (with all channels ON). As the chart shows, Stage Shedding operation significantly improves efficiencies at light loads (≤10A). At 1% of full load (0.6A), Stage Shedding operation improves efficiency more than 25%. Figure 4 shows the load transient response waveform for the 30A load step. With ten POSCAPS (330µF/2.5V,

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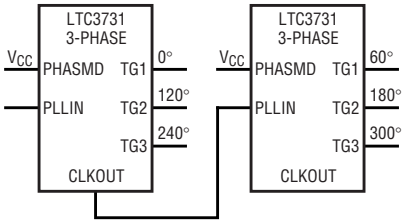


Figure 7a. 6-phase configuration

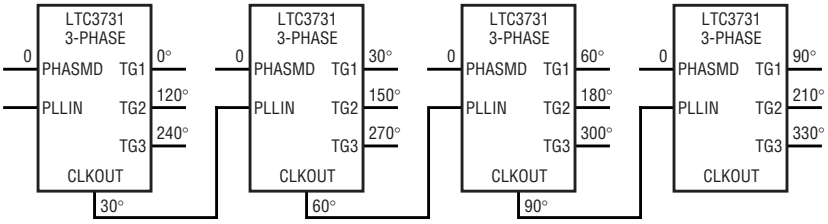
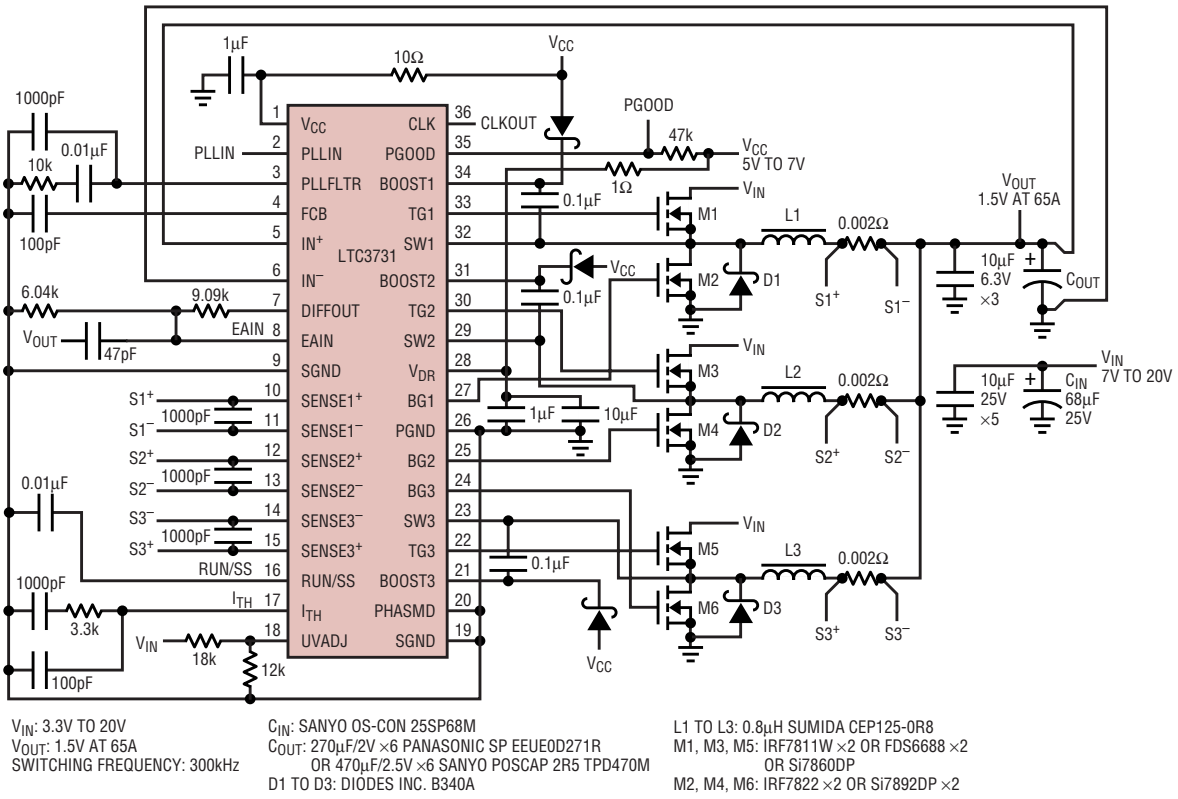


Figure 7b. 12-phase configuration



VIN: 3.3V TO 20V
VOUT: 1.5V AT 65A
SWITCHING FREQUENCY: 300kHz

CIN: SANYO OS-CON 25SP68M
COUT: 270µF/2V ×6 PANASONIC SP EEUE0D271R
OR 470µF/2.5V ×6 SANYO POSCAP 2R5 TPD470M
D1 TO D3: DIODES INC. B340A

L1 TO L3: 0.8µH SUMIDA CEP125-0R8
M1, M3, M5: IRF7811W ×2 OR FDS6688 ×2
OR Si7860DP
M2, M4, M6: IRF7822 ×2 OR Si7892DP ×2

Figure 8. Basic 3-phase block using the LTC3731

12mΩ ESR) at the output, the output voltage variation is about 70mV$_{P-P}$. The AVP loadline slope is 0.9mΩ in this design.

3-Phase IMVP3 Compatible Power Supply for Mobile Northwood CPUs

Figure 5 shows an IMVP3 power supply for a mobile Northwood CPU. It uses the LTC3730 to drive six small PowerPak SO-8 MOSFETs for up to 45A output current. Like in the previous example, R_A and R_B implement the AVP to minimize the output capacitor size. The IMVP3 specs also require three digital signals in addition to the 5 VID bits to set the output voltage under different operational modes: battery optimized mode (BOM), performance optimized mode (POM), deep sleep mode (DPSLP), and deeper sleep mode (DRPSLPVR). Under the BOM, DPSLP and DPRSLPVR modes, the output voltage is reduced to conserve the battery energy.

Figure 6 shows the measured efficiency under performance mode and deeper sleep modes, where the input is 15V and the switching frequency is 250kHz. The efficiency in performance mode exceeds 82% at 1.3V output over a load range of 3A to 45A. Efficiencies in deeper sleep mode were measured for both Stage Shedding operation and conventional PolyPhase operation. Stage Shedding operation improves the efficiencies significantly in deeper sleep mode: about 10% improvement at 5A current. This corresponds to a power loss saving of 0.7W. In a notebook application, the idle time represents about 70% of the run time, this power saving at deeper sleep mode can generate about 4% longer battery run time (assuming 53Whr battery and 4 hour battery run time).

Versatile LTC3731 Powers Up to 200A Current with 12-Phase Operation

The LTC3731 has a CLKOUT pin that produces a 30 degree or 60 degree clock output (referenced to TG1 rising edge) based on the voltage level of the PHASMD pin. Therefore, multiple LTC3731s can be daisy-chained to produce a 6- or 12-phase operation. Since the error amplifier of the voltage feedback loop is a g_m amplifier, the g_m amplifiers of the LTC3731s can be paralleled, creating a common error amplifier that has an equivalent gain of (g_m • n), where n is the number of LTC3731s in parallel. Figure 7 shows the block diagram for a 6-phase and a 12-phase circuit. Figure 8 shows the detailed schematic diagram of one of the 3-phase blocks shown in Figure 7. Each 3-phase block is capable of 65A load current.

Conclusion

LTC3730, LTC3731 and LTC3732 based 3-phase power supplies can deliver high efficiency over a wide load range. Stage Shedding operation significantly improves efficiency at light loads, making this controller family particularly attractive for battery-powered applications where improved light load efficiency can increase battery run time. This family also includes features that make power supplies smaller and more robust, including overcurrent latchoff and overvoltage protection.