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Third-Generation DC/DC Controllers Reduce Size and Cost

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Introduction

The LTC1735 and LTC1736 are the newest members of Linear Technology's third generation of DC/DC controllers. These controllers use the same constant frequency, current mode architecture and Burst Mode™ operation as the previous generation LTC1435–LTC1437 controllers but with improved features. With OPTI-LOOP™ compensation, new protection circuitry, tighter load regulation and strong MOSFET drivers, these controllers are ideal for the current and future generations of CPU power applications.

The LTC1735 is pin compatible with the previous generation LTC1435/LTC1435A controllers with only minor external component changes. Protection features include internal foldback current limiting, output overvoltage crowbar and optional short-circuit shutdown. The 0.8V ±1% reference allows the low output voltages and 1% accuracy that will be demanded by future microprocessors. The operating frequency (synchronizable up to 500kHz) is set by an external capacitor, allowing maximum flexibility in optimizing efficiency.

The LTC1736 has all of the features of the LTC1735, plus voltage programming for CPU power, in a 24-lead SSOP package. The output voltage in LTC1736 applications is programmed by a 5-bit digital-to-analog converter (DAC) that adjusts the out-

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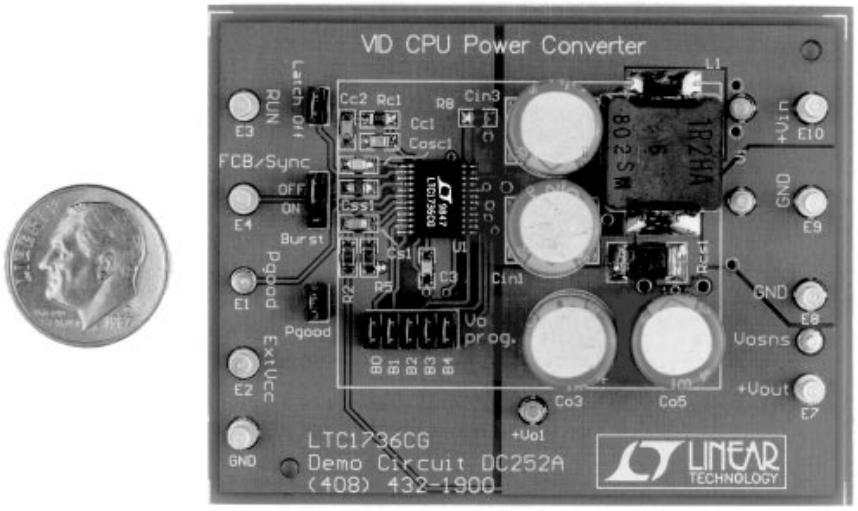

Figure 1. LTC1736 evaluation circuit: a complete 5V–24V to 0.9V–2V/12A converter in 2.15in² of PC board space

LTC1735/LTC1736, continued from page 1

put voltage from 0.925V to 2.00V, according to Intel mobile VID specifications.

Details

The LTC1735 and LTC1736 are synchronous step-down switching regulator controllers that drive external N-Channel power MOSFETs using a programmable fixed frequency OPTI-LOOP architecture. OPTI-LOOP compensation effectively removes the constraints placed on C_{OUT} by other controllers for proper operation (such as limits on low ESRs). A maximum duty cycle limit of 99% provides low dropout operation, which extends operating time in battery operated systems. A forced-continuous control pin reduces noise and RF interference and can assist secondary winding regulation by disabling Burst Mode when the main output is lightly loaded. Soft-start is provided by an external capacitor that can be used to properly sequence supplies. The operating current level is user-programmable via an external current sense resistor. A wide input-supply range allows operation from 3.5V to 30V (36V maximum).

Protection

New internal protection features in the LTC1735 and LTC1736 controllers include foldback current limiting, short circuit detection, short-circuit latch-off and overvoltage protection. These features protect the PC board, the MOSFETs and the load itself (the CPU) against faults.

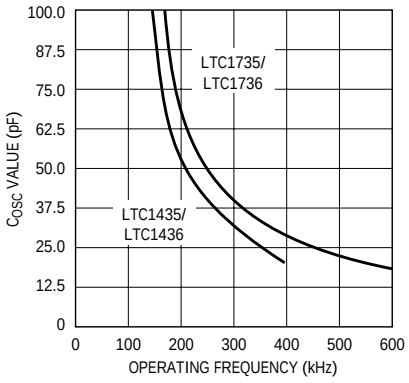

Figure 2. C_{OSC} value vs frequency for the LTC1435/36 and the LTC1735/36

Fault Protection: Overcurrent Latch-Off

The RUN/SS pin, in addition to providing soft-start capability, also provides the ability to shut off the controller and latch off when an overcurrent condition is detected. The RUN/SS capacitor, C_{SS}, (refer to Figure 5) is used initially to turn on and limit the inrush current of the controller. After the controller has been started and given adequate time to charge the output capacitor and provide full load current, C_{SS} is used as a short-circuit timer. If the output voltage falls to less than 70% of its nominal output voltage after C_{SS} reaches 4.2V, it is assumed that the output is in a severe overcurrent and/or short-circuit condition and C_{SS} begins discharging. If the condition lasts for a long enough period, as determined by the size of C_{SS}, the controller will be shut down until the RUN/SS pin voltage is recycled.

This built-in latch-off can be overridden by providing >5µA at a compliance of 4V to the RUN/SS pin (refer to the LTC1735/LTC1736 Data Sheet for details). This external current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during a severe overcurrent and/or short-circuit condition.

Why should you defeat overcurrent latch-off? During the prototyping stage of a design, there may be a problem with noise pickup or poor layout causing the protection circuit to latch off. Defeating this feature will allow easy troubleshooting of the circuit and PC layout. The internal short-circuit detection and foldback current limiting still remain active, thereby protecting the power supply system from failure. After the design is complete, you can decide whether to enable the latch-off feature.

Fault Protection: Current Limit and Current Foldback

The LTC1735/LTC1736 current comparator has a maximum sense voltage of 75mV, resulting in a maximum MOSFET current of $75mV/R_{SENSE}$. The LTC1735/LTC1736 includes current foldback to help further limit load current when the output is shorted to ground. If the output falls by more than one-half, the maximum sense voltage is progressively lowered from 75mV to 30mV. Under short-circuit conditions with very low duty cycle, the LTC1735/LTC1736 will begin cycle skipping in order to limit the short-circuit current. In this situation, the bottom MOSFET will be on most of the time, conducting the current. The average short-circuit current will be approximately $30mV/R_{SENSE}$. Note that this function is always active and is independent of the short circuit latch-off.

Fault Protection: Output Overvoltage Protection (OVP)

An output overvoltage crowbar turns on the synchronous MOSFET to blow a system fuse in the input lead when

Table 1. Overvoltage protection comparison

Operating Condition	Soft Latch	Hard Latch
Fast Transients	Controls Overshoot	Latches Off
Output Shorted to 5V	Output Clamped at OVP	Latches Off
VID Voltage Decrease	Regulates New Voltage	Latches Off
Noise	Controls Output	Latches Off
Shorted Top MOSFET	Bottom MOSFET Overloads	Bottom MOSFET Overloads
Output Voltage Can Reverse	No	Yes
When Overload is Removed	Resumes Normal Operation	Remains Latched Off
Troubleshooting Faults	Easy DC Measurements	Difficult; May Require Digital Oscilloscopes

Table 2. FCB possible states

FCB Pin	Condition
DC Voltage: 0V–0.7V	Burst Disabled/ Forced Continuous, Current Reversal Enabled
DC Voltage: > 0.9V	Burst Mode, No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
($V_{FCBSYNC}$ > 1.5V)	Burst Mode Disabled, No Current Reversal

the output of the regulator rises much higher than nominal levels. The crowbar can cause huge currents to flow, greater than in normal operation. This feature is designed to protect against a shorted top MOSFET or short circuits to higher supply rails; it does not protect against a failure of the controller itself.

Previous latching crowbar schemes for overvoltage protection have a number of problems (see Table 1). One of the most obvious, not to mention most annoying, is nuisance trips caused by noise or transients momentarily exceeding the OVP threshold. Each time that this occurs with latching OVP, a manual reset is required to restart the regulator. Far more subtle is the resulting output voltage reversal. When the synchronous MOSFET latches on, a large reverse current is loaded into the inductor while the output capacitor is discharging. When the output voltage reaches zero, it does not stop there, but rather continues to go negative until the reverse inductor current is depleted. This requires a sizable Schottky diode across the output to prevent excessive negative voltage on the output capacitor and load.

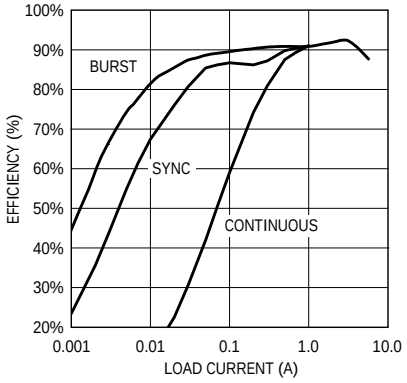

Figure 3. Efficiency vs load current for three modes of operation

A further problem on the horizon for latching OVP circuits is their incompatibility with on-the-fly CPU core voltage changes. If an output voltage is reprogrammed from a higher voltage to a lower voltage, the OVP will temporarily indicate a fault, since the output capacitor will momentarily hold the previous, higher output voltage. With latching OVP, the result will be another latch-off, with a manual reset required to attain the new output voltage. To prevent this problem, the OVP threshold must be set above the maximum programmable output voltage, which would do little good when the output voltage was programmed near the bottom of its range.

In order to avoid these problems with traditional latching OVP circuits, the LTC1735 and LTC1736 use a new "soft latch" OVP circuit. Regardless of operating mode, the synchronous MOSFET is forced on whenever the output voltage exceeds the regulation point by more than 7.5%. However, if the voltage then returns to a safe level, normal operation is allowed to resume, thereby preventing latch-off caused by noise or voltage reprogramming. Only in the case of a true fault, such as a shorted top MOSFET, will the synchronous MOSFET remain latched on until the input voltage collapses or the system fuse blows.

The new soft latch OVP also provides protection and easy diagnosis of other overvoltage faults, such as a lower supply rail shorted to a higher voltage. In this scenario, the output voltage of the higher regulator is pulled down to the OVP voltage of the soft-latched regulator, allowing the problem to be easily diagnosed with DC measurements. On the other hand, latching OVP provides only a millisecond glimpse of the fault as it latches off, forcing the use of expensive digital oscilloscopes for troubleshooting.

Three Operating Modes/One Pin: Sync, Burst Disable and Secondary Regulation

The FCB pin is a multifunction pin that controls the operation of the synchronous MOSFET and is an input for external clock synchronization. When the FCB pin drops below its 0.8V threshold, continuous mode operation is forced. In this case, the top and bottom MOSFETs continue to be driven synchronously regardless of the load on the main output. Burst Mode operation is disabled and current reversal is allowed in the inductor.

In addition to providing a logic input to force continuous synchronous operation and external

Table 3. Comparison of LTC1735/36 controllers with LTC1435A/36A-PLL controllers

Parameter	LTC1735/1736	LTC1435A/1436A-PLL
Reference	0.8V	1.19V
Load Regulation	0.1% Typ, 0.2% Max	0.5% Typ 0.8% Max
Max Current Sense	75mV	150mV
Minimum On-Time	200ns	300ns
Synchronizable	Yes	LTC1436A-PLL Only
Int V_{CC} Voltage	5.2V (7V Max)	5V (10V Max)
Power Good Output	LTC1736 Only	LTC1436A/36A-PLL Only
Current Foldback	Internal	External
Output OV Protection	Yes	No
Output OI Latch-Off	Optional	No
Packages	SO16, GN16/G24	SO16, G16/GN24
MOSFET Drivers	3×	1×

Table 4. VID output voltage programming

B4	B3	B2	B1	B0	V_{OUT} (V)
0	0	0	0	0	2.000V
0	0	0	0	1	1.950V
0	0	0	1	0	1.900V
0	0	0	1	1	1.850V
0	0	1	0	0	1.800V
0	0	1	0	1	1.750V
0	0	1	1	0	1.700V
0	0	1	1	1	1.650V
0	1	0	0	0	1.600V
0	1	0	0	1	1.550V
0	1	0	1	0	1.500V
0	1	0	1	1	1.450V
0	1	1	0	0	1.400V
0	1	1	0	1	1.350V
0	1	1	1	0	1.300V
0	1	1	1	1	*
1	0	0	0	0	1.275V
1	0	0	0	1	1.250V
1	0	0	1	0	1.225V
1	0	0	1	1	1.200V
1	0	1	0	0	1.175V
1	0	1	0	1	1.150V
1	0	1	1	0	1.125V
1	0	1	1	1	1.100V
1	1	0	0	0	1.075V
1	1	0	0	1	1.050V
1	1	0	1	0	1.025V
1	1	0	1	1	1.000V
1	1	1	0	0	0.975V
1	1	1	0	1	0.950V
1	1	1	1	0	0.925V
1	1	1	1	1	**

Note: *, ** represent codes without a defined output voltage as specified in Intel specifications. The LTC1736 interprets these codes as a valid inputs and produces output voltage as follows: [01111]=1.250V, [11111]=0.900V.

synchronization, the FCB pin provides a means to regulate a flyback winding output. It can force continuous synchronous operation when needed by the flyback winding, regardless of the primary output load. In order to prevent erratic operation if no external connections are made, the FCB pin is pulled high by a 0.25µA internal current source.

The LTC1735 internal oscillator can be synchronized to an external oscillator by applying a clock signal of at least $1.5V_{P-P}$ to the FCB pin. When synchronized to an external frequency, Burst Mode operation is disabled but cycle skipping occurs at low load currents since current reversal is inhibited. The bottom gate will come on every 10 clock cycles to ensure that the bootstrap cap is kept refreshed and to keep the frequency above the audio range. The rising edge of an external clock applied to the FCB pin starts a new cycle.

The range of synchronization is from $0.9 \times f_O$ to $1.3 \times f_O$, with f_O set by C_{OSC}. Attempting to synchronize to a higher frequency than $1.3 \times f_O$ can result in inadequate slope compensation and cause loop instability with high duty cycles. If loop instability is observed while synchronized, additional slope compensation can be obtained by simply decreasing C_{OSC}. A plot of operating frequency versus C_{OSC} value is shown in Figure 2.

Table 2 summarizes the possible states available on the FCB pin.

Figure 3 gives a comparison of efficiencies in a regulator for the three operating modes: forced continuous operation, pulse skipping mode (synchronized at $f = f_O$) and Burst Mode operation.

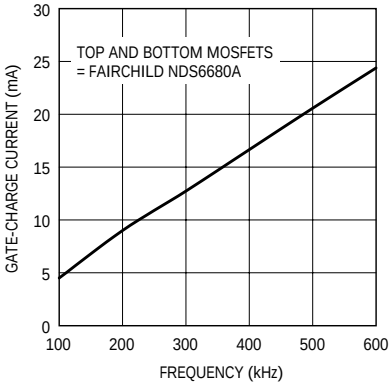

Figure 4. MOSFET gate-charge current vs frequency

Converting to the LTC1735

The LTC1735 is pin compatible with the LTC1435/LTC1435A, with minor component changes. Table 3 shows the differences between the two controllers. The important items to note are:

1. The LTC1735 has a 0.8V reference (versus 1.19V for the LTC1435) that allows lower output voltage operation (down to 0.8V). Thus, the output feedback divider will have to be recalculated for the same output voltage.
2. The LTC1735's maximum current sense voltage is half that of the LTC1435. This reduces the power lost in the sense resistor by half. Hence, for the same maximum output current, the current sense resistor must be cut in half.

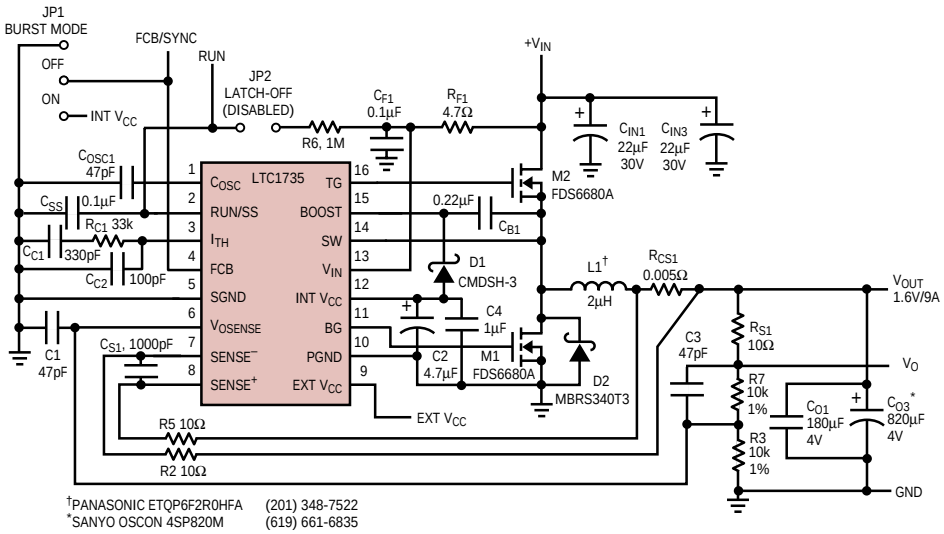

Figure 5. High efficiency 1.6V/9A CPU power supply

3. The gate drivers of the LTC1735 are 3× the strength of those in the LTC1435. This equates to faster rise and fall times for driving the same MOSFETs plus the capability to drive larger MOSFETs with less efficiency loss due to transition losses.

Speed

The LTC1735/LTC1736 are designed to be used in higher current applications than the LTC1435 family. Stronger gate drives allow paralleling multiple MOSFETs or higher operating frequencies. The LTC1735 has been optimized for low output voltage operation by reducing the minimum on-time to less than 200ns. Remember, though, that transition losses can still impose significant efficiency penalties at high input voltages and high frequencies. Just because the LTC1735 can operate at frequencies above 300kHz doesn't mean it should. Figure 4 shows a plot of MOSFET charge current versus frequency.

Linear Current Comparator Operation

Since the trend in the marketplace has forced output voltages to lower and lower values, the current sense inputs have been optimized for low voltage operation. The current sense comparator has a linear response characteristic, without discontinuities, from 0V to 6V output voltages. In the LTC1435/LTC1435A, two input stages are used to cover this range, so an overlap exists together with a transition region. The LTC1735/LTC1736 uses only one input stage and includes slope compensation that operates over the full output voltage range. This allows the LTC1735/LTC1736 to be operated in grounded R_{SENSE} applications as well.

LTC1736 Additional Features

The LTC1736 includes all the features of the LTC1735, plus 5-bit mobile VID control and a power-good comparator in a 24-lead SSOP package. The window comparator monitors the output voltage and its open-drain output is pulled low when the divided voltage is *not* within ±7.5% of the 0.8V reference voltage.

The output voltage is digitally set to levels between 0.925V and 2.00V using the voltage identification (VID) inputs B0–B4. The internal 5-bit DAC configured as a precision resistive voltage divider sets the output voltage in 50mV or 25mV increments according to Table 4. The VID codes (00000–11110) are compatible with the Intel mobile Pentium® II processor. The LSB (B0) represents 50mV increments in the upper voltage range (2.00V–1.30V) and 25mV increments in the lower voltage range (1.275V–0.925V). The MSB is B4. When all bits are low or grounded, the output voltage is 2.00V.

The LTC1736 also has remote sense capability. The top of the internal resistive divider is connected to V_{OSENSE} and is referenced to the SGND pin. This allows a Kelvin connection for remotely sensing the output voltage directly across the load, eliminating any PC board trace resistance errors.

Applications

Figure 5 shows a 1.6V/9A application using the LTC1735. The input voltage can range from 6V to 26V. Figure 6 shows a VID application using the LTC1736 optimized for output voltages of 1.6V to 1.3V with a 5V to 24V input voltage range.

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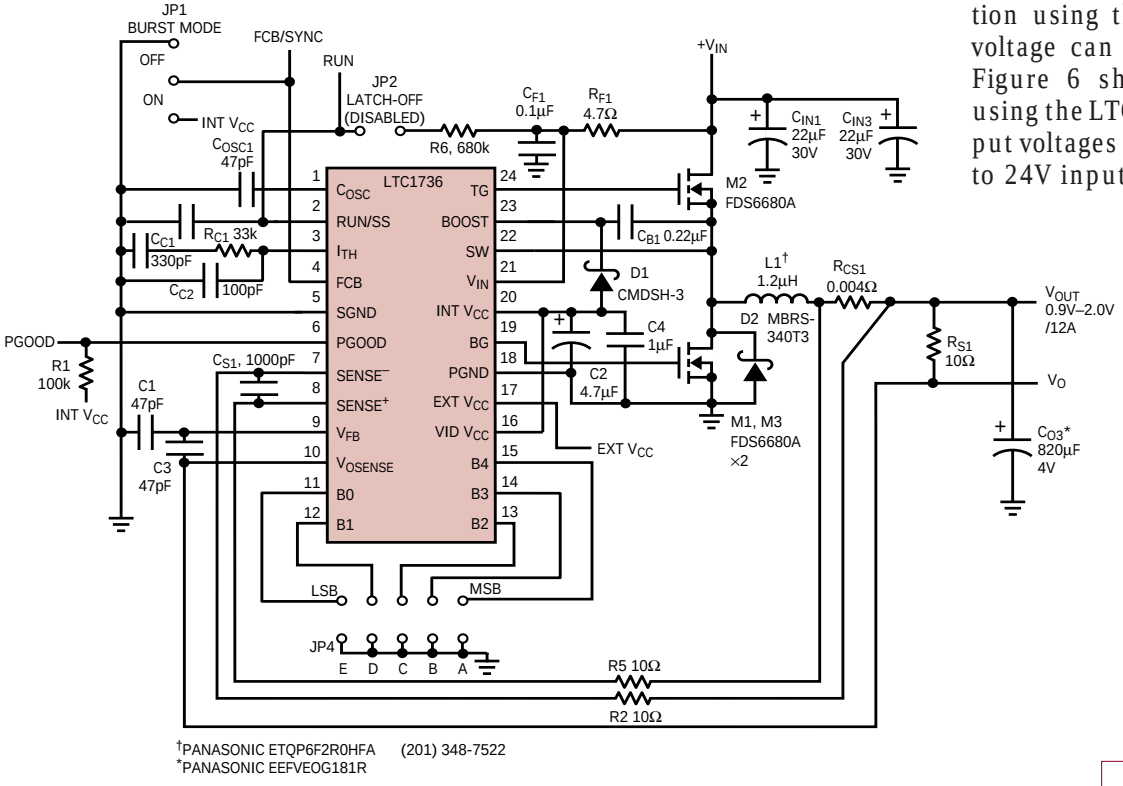

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Figure 6. High efficiency, VID programmable, 0.9V–2.0V/12A CPU power supply

LTC1735/LTC1736, continued from page 6

Conclusion

The LTC1735 and LTC1736 are the latest members of Linear Technology's family of constant frequency, N-channel high efficiency controllers. With new protection features, improved circuit operation and strong MOSFET drivers, the LTC1735 is an ideal upgrade to the LTC1435/LTC1435A for higher current applications. With the integrated VID control, the LTC1736 is ideal for CPU power applications. The high performance of these controllers with wide input range, 1% reference and tight load regulation makes them ideal for next generation designs.