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New 16-Bit 50Msps DAC Offers Highest AC and DC Performance

by James L. Brubaker and William C. Rempfer

New 16-Bit 50Msps DAC

The new LTC1668 is a 16-bit, 50Msps, differential current output DAC with exceptional AC and DC performance. Spurious free dynamic range (SFDR) of greater than 87dB, glitch impulse of <4pV-s, 18ns full-scale settling time (to 0.1%) and 1LSB DNL and 3LSB INL (typical) provide the highest combination of AC and DC specifications available. The LTC1668 is part of a pin-compatible family that includes the 14-bit LTC1667 and the 12-bit LTC1666.

Block Diagram and Function

Referring to Figure 1, the LTC1668 has a 16-bit parallel input, an internal reference and differential 10mA full-scale current outputs. It runs on a ±5V supply and dissipates 180mW. The DAC contains an array of current sources that are steered to I_{OUTA} or I_{OUTB} with NMOS differential current switches. The four most significant

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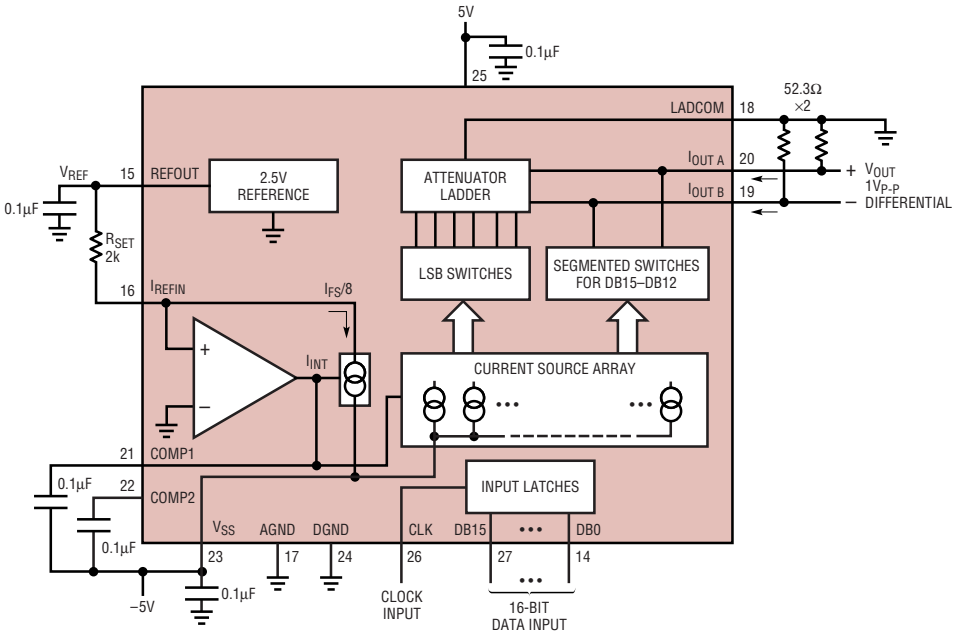

Figure 1. LTC1668 block diagram

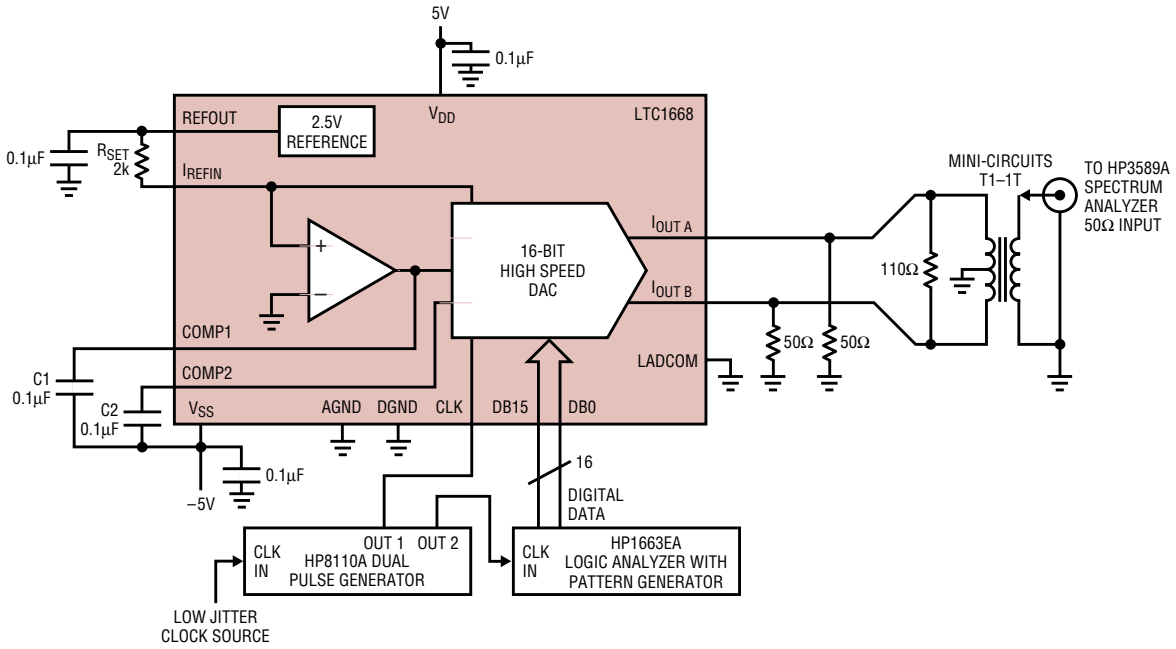

Figure 2. AC characterization setup

LTC1668, continued from page 1

bits (DB15–DB12) are segmented into fifteen equal currents. The lower bits (DB11–DB0) are binary weighted using a combination of current scaling and a differential resistive attenuator ladder.

The DAC has an internal 2.5V reference. The full-scale DAC output current, I_{OUTFS}, is set by a resistor (R_{SET}) between REFOUT and I_{REFIN}. (For I_{OUTFS} of 10mA, R_{SET} is 2k.)

The digital inputs can accept CMOS levels from either 3V or 5V logic and can be clocked at up to 50Msps. They are latched on the rising edge of the clock input, CLK.

The differential current outputs have a compliance range of ±1V and may be used in single-ended or differential configurations. The outputs can be converted to a voltage by resistor loading, transformer coupling or by using an op amp current-to-voltage converter.

Best AC and Frequency Domain Performance

The LTC1668 offers the best frequency domain performance available today. It excels with single-tone and multi-tone signals at full scale and even with reduced amplitude signals.

Single-Tone Spurious Free Dynamic Range (SFDR)

Figure 2 shows the AC characterization setup used for the LTC1668. Figure 3 shows the single tone SFDR at 50Msps with a 1MHz output signal. The signal amplitude is 0dBFS (that is, a full-scale digital sine wave) and the doubly terminated output gives an output level of –8.25dBm. The SFDR of 87dB is the best in the industry.

Figure 4 shows the single-tone SFDR versus output frequency for a variety of sample rates and output frequencies. The figure shows that SFDRs of greater than 90dB are achievable at low frequencies. The SFDR rolls off with output frequency but remains better than 80dB at 5MHz output and better than 70dB at 20MHz output.

2-Tone Spurious Free Dynamic Range (SFDR)

Figure 5 shows how the performance holds up at 50Msps with the DAC generating two tones at 4.9MHz and 5.1MHz, each with a half-scale digital

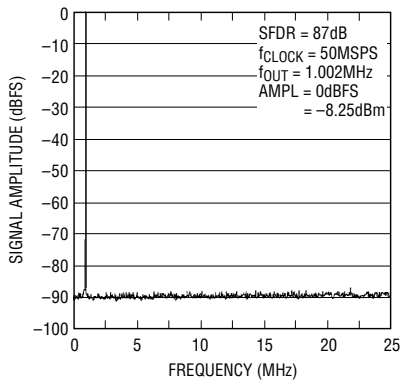

Figure 3. Single-tone SFDR at 50Msps

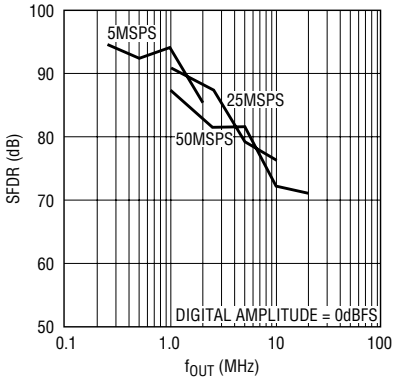

Figure 4. SFDR vs f_{OUT} and f_{CLOCK}

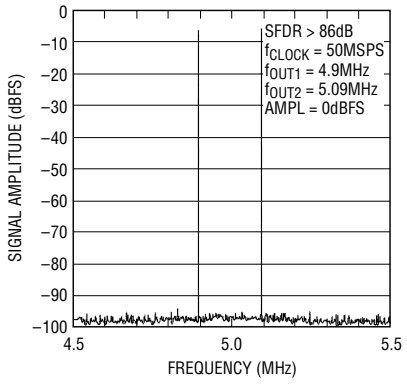

Figure 5. 2-tone SFDR

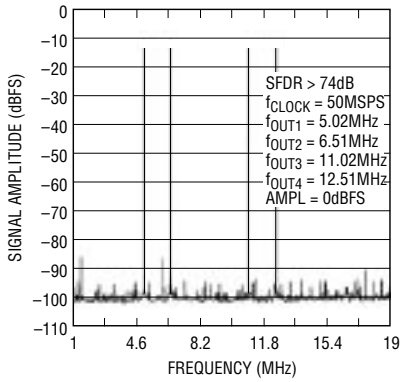

Figure 6. 4-tone SFDR, f_{CLOCK} = 50Msps

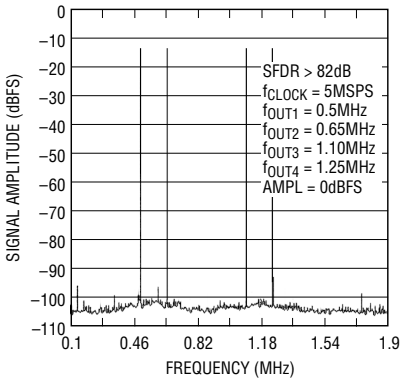

Figure 7. 4-tone SFDR, f_{CLOCK} = 5Msps

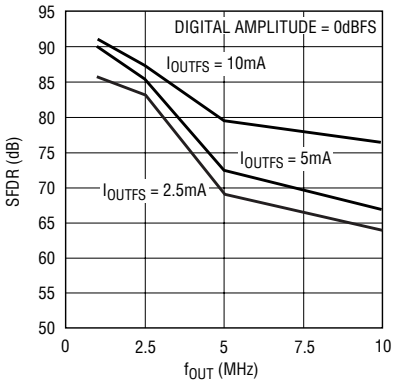

Figure 8. SFDR vs f_{OUT} and I_{OUTFS} at f_{CLOCK} = 25Msps

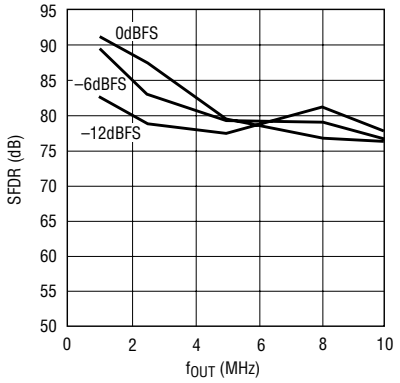

Figure 9. SFDR vs f_{OUT} and digital amplitude (dBFS) at f_{CLOCK} = 25Msps

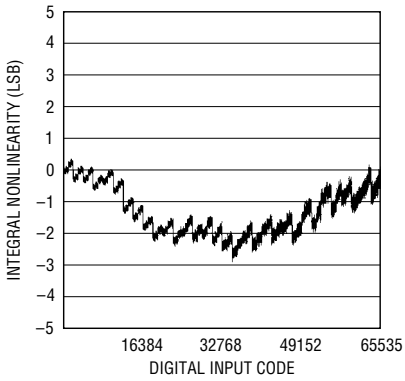

Figure 10. Integral nonlinearity

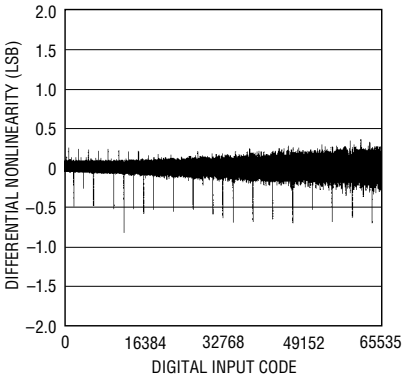

Figure 11. Differential nonlinearity

sine wave amplitude (–6dBFS). By convention, the composite signal amplitude is called a 0dBFS signal and the SFDR is measured relative to either –6dBFS tone. The SFDR in a 1MHz output span is 86dB, which includes the 3rd order intermodulation products.

Four-Tone SFDR

Moving to a four-tone measurement in Figure 6, we have tones of 5MHz, 6.5MHz, 11MHz and 12.5MHz, each with a quarter-scale digital sine wave amplitude. At the same 50Msps rate and with much more stringent conditions of higher output frequencies and 18MHz measurement bandwidth, the SFDR is 74dB, relative to any of the –12dBFS tones. Taking the same digital waveform used in Figure 6 and reducing the clock rate by a factor of 10 (to 5Msps) we see the results of Figure 7, where the SFDR improves to 84dB, relative to any of the –12dBFS tones. This puts the worst spur at 96dB below the 0dB full scale of the DAC.

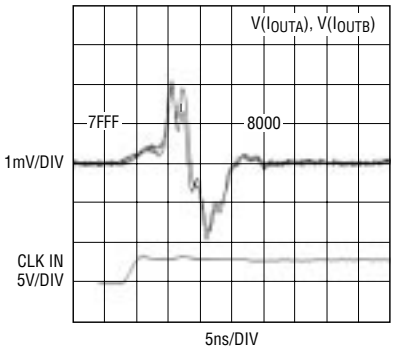

Figure 12. Single-ended midscale glitch impulse

SFDR with Reduced Output Amplitudes

In the past, it has been common to use a DAC as a gain control by lowering the full-scale output current of the DAC. Figure 8 shows the SFDR with reduced full-scale output current. As an alternative to that method, the 16-bit resolution of the LTC1668 allows attenuation to be done in the digital domain. Figure 9 shows the SFDR with reduced digital sine wave amplitude. Comparing Figures 8 and 9, we see that a 12dB reduction in the full-scale current (2.5mA I_{OUTFS}) gives an 83dB SFDR at 2.5MHz but the SFDR rolls off with increasing output frequency. On the other hand, a 12dB reduction in digital signal amplitude results in an SFDR that is a little lower at low frequencies (78dB at 2.5MHz) but it remains virtually flat up to 10MHz, giving a much better result than the reduced I_{OUTFS} case.

DC and Time-Domain Performance

Because of its good linearity, fast settling time and low glitch, the LTC1668 also excels in applications requiring good DC and time-domain performance.

1LSB DNL and 3LSB INL

The LTC1668 is a precision DAC in addition to being fast. It uses precision bipolar transistors and laser trimmed thin-film resistors (which puts it in a class by itself when compared to competitors' CMOS parts). Figures 10 and 11 show the superior INL and DNL for the DAC.

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LTC1668, continued from page 4

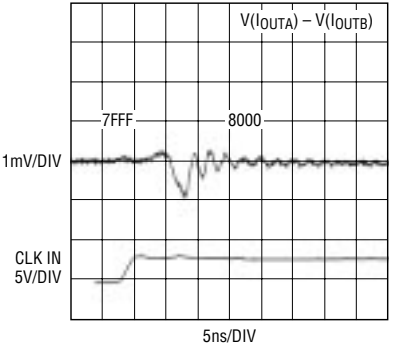

Figure 13. Differential midscale glitch impulse

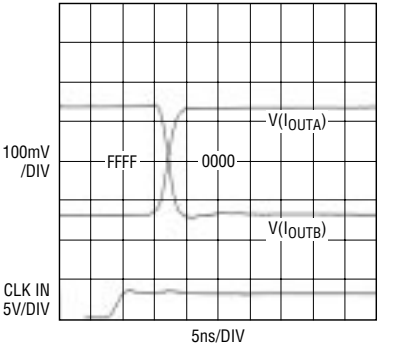

Figure 14. Single-ended output, full-scale transition

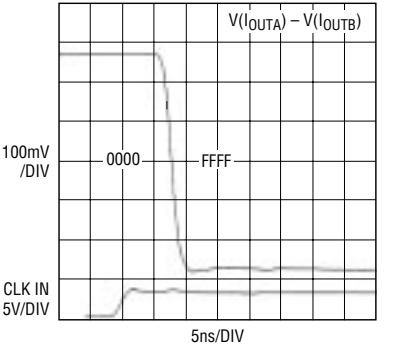

Figure 15. LTC1688 differential settling time

Glitch

Figure 12 shows the single-ended glitch impulse on both I_{OUTA} and I_{OUTB}. The glitch impulse is 15pV-s on either output and the difference is seen to be very small. Figure 13 shows the differential output glitch impulse which is less than 4pV-s.

Full-Scale Step Response

For waveform generation applications, the fast settling time of the LTC1668 is ideal. Figure 14 shows the full-scale settling for each output (I_{OUTA} and I_{OUTB}). Figure 15 shows the differential settling time, which is also 18ns. Differential settling time to 0.1% is 18ns.

Conclusion

The LTC1668 offers the highest level of both AC and DC performance of any DAC for new communications and instrumentation applications. As such, it should be the DAC of choice for new designs.