Low Voltage Amplifiers Give Choice of Accuracy or Speed

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Introduction

Two new families of single, dual and quad amplifiers, the 1mA LT6220/1/2 and the 3mA LT1803/4/5, provide high speed amplification on supplies as low as 2.5V. The 85MHz LT1803 series is optimized for large signals, with a 100V/µs slew rate, while the 60MHz LT6220 series focuses on excellent DC performance at low current, with a maximum input offset specification of only 350µV. Both series have rail-to-rail output stages that can swing to within 20mV of the rails, and rail-to-rail inputs that can be used anywhere within the supplies. The supply range is 2.5 to 12V. DC accuracy is insured by trimming of the input offset voltage and cancellation of input bias current. Figures 1 and 2 show the results of a proprietary bias current cancellation circuit.

The devices are available in small packages; singles in the SOT-23, and duals in the DFN as well as the larger SO packages.

Performance

Table 1 summarizes the performance of the devices. Note that input offset voltage and input bias current are specified and guaranteed with the common mode voltage near each rail. Histograms of input offset voltage are shown in Figures 3 and 4. The large signal transient response is shown in Figures 5 and 6. The response is clean with no aberrations.

Circuit Description

Figure 7 shows a simplified schematic of the amplifiers. The circuit is composed of three distinct stages: an input stage, an intermediate stage, and an output stage. The input stage consists of two differential amplifiers, a PNP stage (Q1 and Q2) and an NPN stage (Q3 and Q4), that are active over different portions of the input common mode range. The intermediate stage is a folded cascode configuration formed by Q8, Q9, Q11 and Q12, which provides most of the voltage gain. A pair of complementary common emitter devices, Q14 and Q15, creates an output stage which can swing from rail to rail.

In the input stage, devices Q18 and Q19 act to cancel the bias current of the PNP input pair. When Q1 and Q2 are active, the current in Q16 matches the current in Q1 and Q2, thus the base current of Q16 is nominally equal to the base current of Q1/Q2. The base current of Q16 is mirrored by devices Q17, Q18 and Q19 to each input. The cancellation is effective for common mode voltage

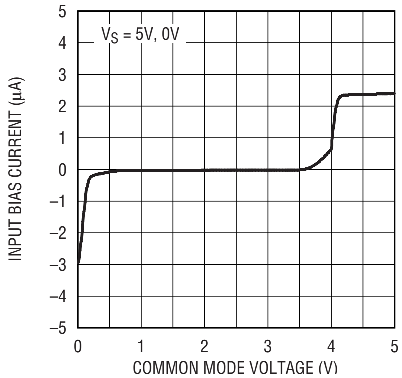

Figure 1. LT1803 I_B vs common mode voltage

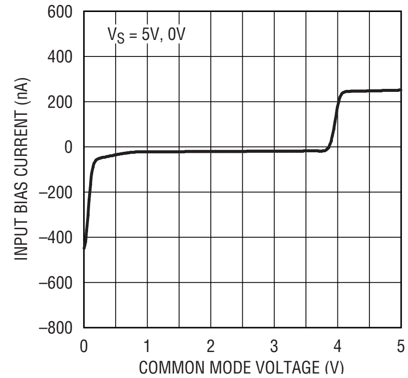

Figure 2. LT6220 I_B vs common mode voltage

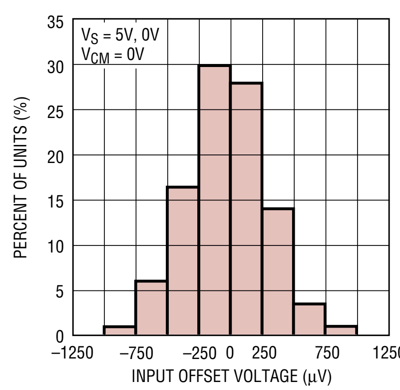

Figure 3. LT1803 offset voltage distribution

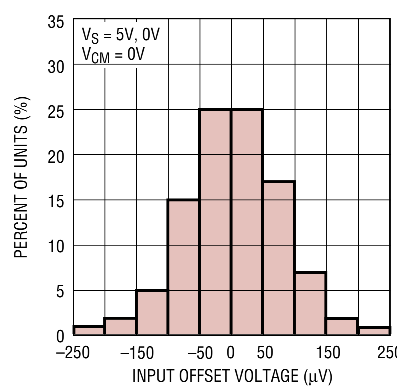

Figure 4. LT6220 offset voltage distribution

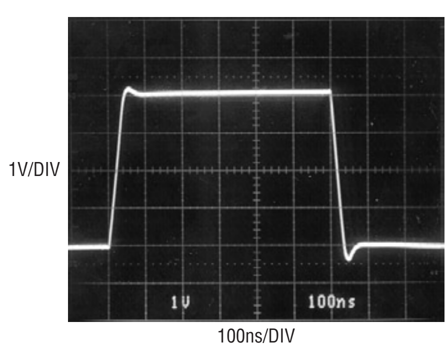

Figure 5. LT1803 slew rate

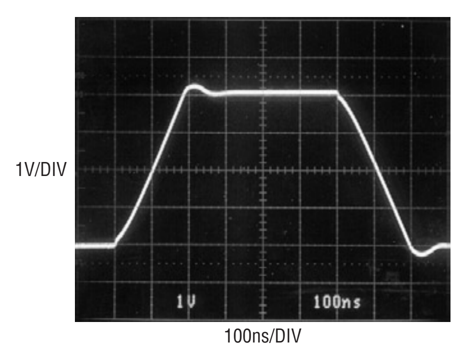

Figure 6. LT6220 slew rate

Table 1. Specifications of LT1803 and LT6220 at 25°C, V_S = 5V, 0V

Parameter	Conditions	LT1803	LT6220	Units
–3dB Bandwidth	A_V = 1	60	55	MHz
Gain-Bandwidth Product		85	60	MHz
Slew Rate	R_L = 1k	100	20	V/µs
Supply Current		3.0	1.0	mA (Max)
Operating Supply Range		2.5 to 12	2.5 to 12	V
Input Offset Voltage	$V_{CM} = V^-$, SO-8	2	0.35	mV (Max)
	$V_{CM} = V^-$,SOT-23	5	0.85	
Input Bias Current	$V_{CM} = V^-+1V$	750	150	nA (Max)
	$V_{CM} = V^+$	5500	600	
CMRR		66	85	dB (Min)
PSRR	V_S = 2.5V to 10V, V_{CM} = 0V	68	86	dB (Min)
Input Voltage Noise	f = 10kHz	21	10	$nV/\sqrt{Hz}$
Harmonic Distortion	V_S = 5V, A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 500kHz (LT6220) f_C = 1MHz (LT1803)	–75	–75	dBc
A_{VOL}	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k	20	30	V/mV (Min)
Output Voltage Swing LOW	I_L = 0mA	60	40	mV (Max)
	I_L = 15mA (LT1803) I_L = 20mA (LT6220)	300	650	
Output Voltage Swing HIGH	I_L = 0mA	60	40	
	I_L = 15mA (LT1803) I_L = 20mA (LT6220)	600	900	

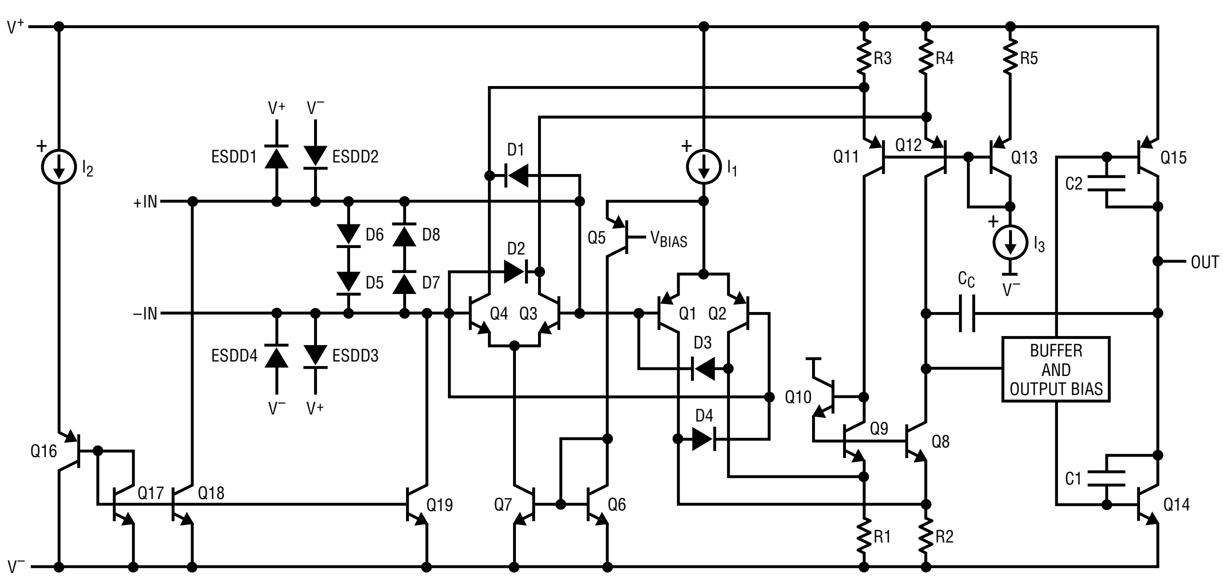

Figure 7. Simplified schematic

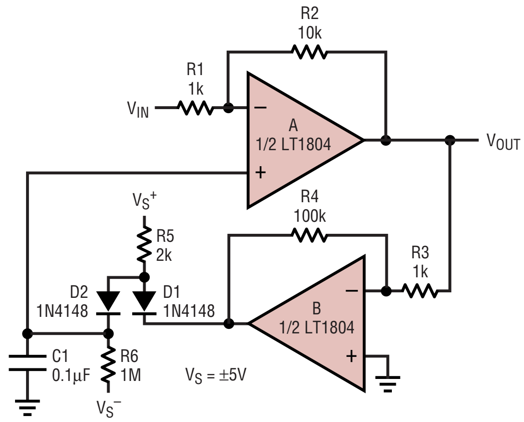

Figure 8. Inverting DC restore

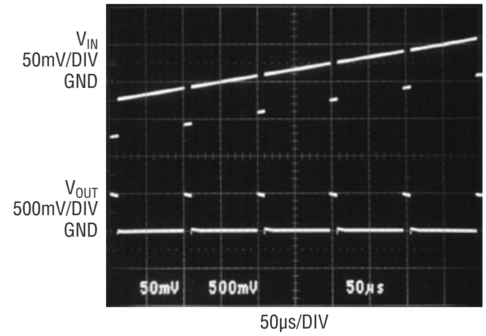

Figure 9. Inverting DC restore oscillograph

greater than the saturation voltage of Q18 and Q19, about V^- + 0.2V, up to the voltage that the PNP devices switch off, about V^+ – 1.3V.

Inverting Amplifier with DC Restore

The circuit of Figure 8 shows half of the LT1804 used as a gain of –10 amplifier, and the other half as a DC restore. This type of circuit is often associated with photomultiplier tubes and photodiodes (see Figure 10), which are inherently unipolar but can be subject to annoying DC components caused by amplifier offsets, dark current, and the presence of residual light. The oscillograph in Figure 9 shows how effectively the circuit rejects the varying DC level which the incoming negative going pulses are riding on (top trace). The pulses are inverted and restored to a 0V ground reference (bottom trace)[1]. Note that this is not the same as AC coupling, which would simply center the average output waveform around ground. The DC restore function has three operating regions: output high or "ignore," output low or "restore," and output zero or "lock."

When the output is high, op amp B's output falls low turning D1 on and D2 off. This leaves the pull down R6 in place, so the voltage on C1 falls slowly. Therefore the positive output voltage also starts to fall back towards ground via op amp A. The long time constant of R6 • C1 is what makes this the "ignore" function. Of course, it does not fully ignore positive outputs, as that would make the circuit useless. The point is, though, that a positive signal indicates the presence of signal, so the restore circuit does little to zero the output.

When the output is low, however, we have a situation where we have negative light. Since that situation is unlikely to exist outside of academic circles, we can assume that we have zero light, or at least are at the light signal floor, and would like to set that as the DC reference level. To that end, op amp B's output goes high turning D1 off and D2 on. This now leaves R5 to pull up on C1 about 500 times harder than R6 had pulled down. Again, through op amp A, this positive going voltage causes the output to rise quickly. When the output reaches 0V, op amp B detects this and pulls down on D1, stopping the restore function and entering "lock" mode.

In lock mode, light is presumably absent, and the output is held close to 0V. D1 and D2 are both on, and although they are running different currents, the resultant mismatch voltage is relatively small output referred because of the high gain around op amp B. Should a negative going "light present" pulse occur at V_{IN}, the circuit goes again into ignore mode.

Photodiode Amplifier

The circuit in Figure 10 is a stepped gain transimpedance photodiode amplifier. At low signal levels, the circuit has a high 100kΩ transimpedance gain, but at high signal levels the circuit automatically and smoothly changes to a low 3.1kΩ gain. The benefit of a stepped gain approach is that it maximizes dynamic range,

continued on page 29

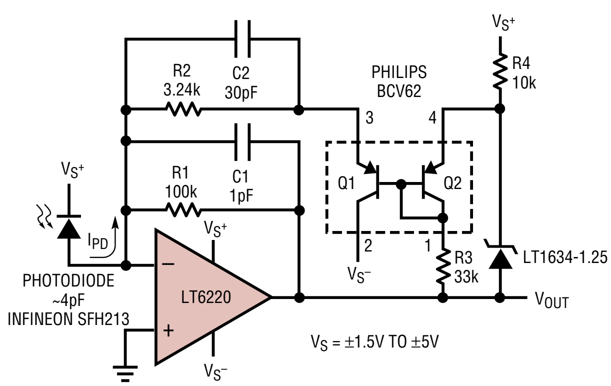

Figure 10. Photodiode amplifier

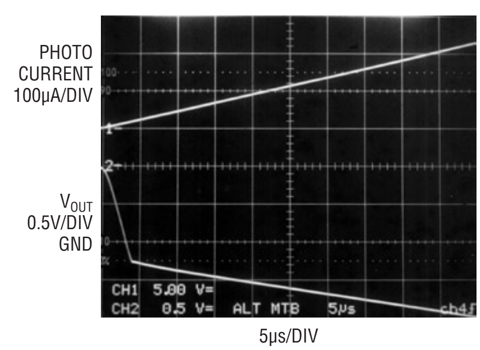

Figure 11. Stepped gain photodiode amplifier oscillograph

Discharging (Battery Mode)

When the adapter input falls, so that the system bus voltage requirements can no longer be met, the LTC1980 switches to the regulator mode. In this mode the LTC1980 no longer functions as a battery charger. It instead acts as a battery discharger. Power flows "backwards" from the battery to the linear regulator. The output voltage of the flyback, which is input to the linear regulator, should be as low as possible in order to maximize efficiency and battery run time. The efficiency of the battery to system bus voltage conversion can be as high as 88%.

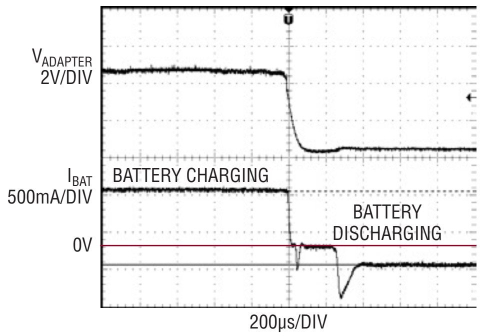

Figure 2. Adapter voltage and battery current (adapter removal)

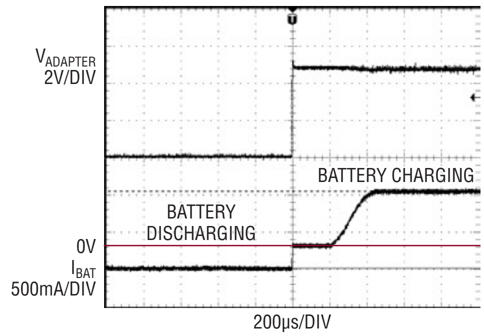

Figure 3. Adapter voltage and battery current (adapter insertion)

The Linear Regulator

A low dropout regulator, using an external P-FET as the pass element, regulates the system bus voltage. The linear regulator takes its power from the output of the AC adapter. Dissipation in the linear regulator is lowest when the AC adapter voltage is near the system bus voltage. When the system is in battery discharging mode, the voltage input to the linear regulator is the output of the synchronous flyback converter. This voltage should be set to be only a percent or two above the required output voltage (allowing for IR drops in the pass element). This prevents saturating the gate drive to the pass element and will aid in transient recovery.

Figure 1 shows a typical application circuit for charging a single 4.1V Li-Ion cell. The adapter voltage can vary from 4V to 9V, demonstrating one key advantage of the flyback topology. Figures 2 and 3 show battery current and adapter voltage during the transition from battery charging (adapter present) to regulator mode (battery discharging). The load on the linear regulator is 200mA, supported either by the battery or the adapter. When the adapter is present the battery is charged at about 650mA. Once the wall adapter is removed the battery is discharged as power flows back through the synchronous flyback converter to support the 200mA load on the linear regulator.

Conclusion

The LTC1980 manages both battery charging *and* system voltage regulation, which is typically the work of two separate devices and their corresponding external circuitry. This feature combined with the fact that the design of the LTC1980 also allows for battery voltages either above or below the adapter voltage, greatly simplifies the task of integrating a battery and adapter into a portable device.

LT1803 and LT6220, continued from page 27

which is very useful on limited supplies. Put another way, in order to get 100kΩ sensitivity and still handle a 1mA signal level without resorting to gain reduction, the circuit would need a 100V negative voltage supply.

The operation of the circuit is quite simple. At low photodiode currents (below 10µA) the output and inverting input of the op amp are no more than 1V below ground. The LT1634 in parallel with R3 and Q2 keep a constant current though Q2 of about 20µA. R4 maintains quiescent current through the LT1634 and pulls Q2's emitter above ground, so Q1 is reverse biased and no current flows through R2. So for small signals, the only feedback path is R1 (and C1) and the circuit is a simple transimpedance amplifier with 100kΩ gain.

As the signal level increases though, the output of the op amp goes more negative. At 12.5µA of photodiode current, the 100kΩ gain dictates that the LT6220 output is about 1.25V below ground. At that point, however, the emitter of Q2 is at ground, and the base of Q1 is one V_{be} below ground. Thus, Q1 turns on and photodiode current starts to flow through R2. The transimpedance gain is therefore now reduced to R1||R2, or about 3.1kΩ. The circuit response is shown in Figure 11. Note the smooth transition between the two operating gains, as well as the linearity of both regions.

Conclusion

The LT1803 series and LT6220 series deliver exceptional performance, and the rail-to-rail inputs and outputs of these devices maximize signal dynamic range while simplifying design for single supply systems. The LT1803 series and the LT6220 series feature reduced supply current, lower input offset voltage, lower input bias current, and higher DC gain than other devices with comparable bandwidth, which is critical in circuits having high input impedance, such as active filters, or in circuits having precision requirements, such as current sensing amplifiers. The LT1803 and LT6220 series are offered in a variety of small packages including a 3mm × 3mm dual fine pitch leadless package with the standard dual op amp pinout and also in the SOT-23 package for a single amplifier. The combination of speed, DC accuracy and low power makes the LT1803 series and the LT6220 series a preferred choice for battery powered, low voltage signal conditioning.

Notes

[1] A DC bias on op amp B's + input could set the output restore to some other reference voltage.