Very Low Dropout (VLDO) Linear Regulator Outperforms Switching Regulators in Low V_{OUT} Applications

by Anthony Bonte

Introduction

Each new generation of computing systems demands more power, lower operating voltages and more supply voltages. CPU core, logic and termination voltages below 1.8V are common. Three or more supply voltages are the norm, where a high efficiency synchronous switching regulator typically generates each voltage. These systems have stringent output voltage regulation specifications for input voltage change, output load current change, temperature change and output load step response. These requirements mandate the need for an accurate, high-speed regulator. In applications that draw 1A–10A of output current, a VLDO™ linear regulator that operates from a low V_{IN} has several advantages over a switching regulator. A VLDO consumes less board space, requires fewer components and costs less than a switcher solution. When the input-to-output voltage differential is low, efficiency is comparable. Figure 1 shows a VLDO replacing a switching regulator in a multiple supply system.

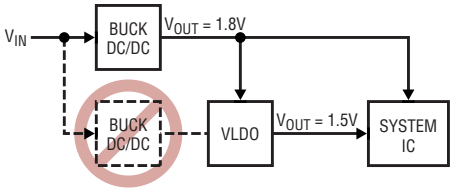


Figure 1. VLDO replaces a switching regulator in a multiple output power supply

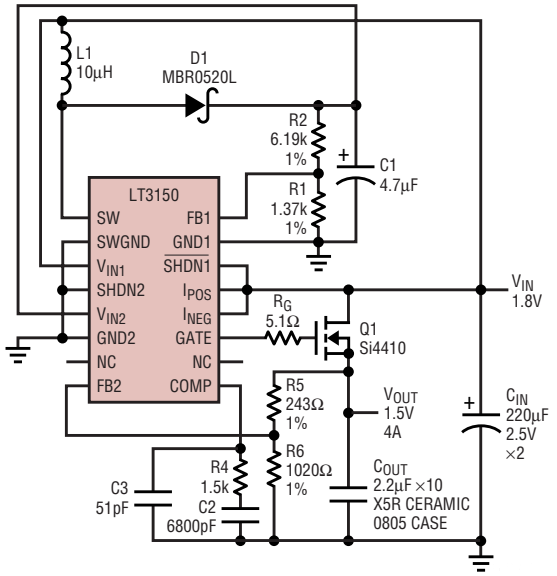
The LT3150 VLDO Combines Accuracy, Fast Response and High Efficiency

The LT3150 controller drives an external N-channel MOSFET as a source follower to create an extremely low dropout, ultra-fast transient response linear regulator. The MOSFET $R_{DS(ON)}$ sets the dropout voltage performance and dropout voltage is proportional to the output load current. The LT3150's precision-trimmed reference provides ±0.6% initial accuracy, ±1% tolerance over temperature and accommodates low-voltage outputs. Transient response performance is optimized around low cost, low ESR, readily available ceramic capacitors. Depending on the individual power supply requirements, the output decoupling network typically consists of multiple 1µF–10µF ceramic capacitors in parallel. Eliminating bulk output capacitors significantly reduces cost.

The LT3150 includes a fixed frequency boost regulator that generates gate drive for the external N-channel MOSFET. The internally compensated current mode PWM architecture combined with a 1.4MHz switching frequency permits the use of tiny, low cost capacitors and inductors. The LT3150 also incorporates current limiting, on/off control for power supply sequencing and overvoltage protection or thermal shutdown with a few external components.

1.8V to 1.5V Linear Regulator

Figure 2 shows a 1.8V to 1.5V linear regulator employing the LT3150 and all surface-mount components. The regulator provides up to 4A of output current using a low-cost, logic-level Siliconix Si4410 N-channel MOSFET for Q1, the pass element. The boost converter composed of L1, D1, R1–R2 and C1 generates a 6.8V gate-drive supply for Q1. The circuit's dropout voltage at 4A is typically 65mV. Due to the low input-to-output voltage differential, efficiency for this circuit is 83.3%. Figure 3 shows the well-behaved transient response of the circuit. Only 22µF of output capacitance limits a 3.9A load step with 50ns rise/fall times to just ±55mV peak deviation in the output. R4, C2 and C3 provide



CIN: PANASONIC SP SERIES EEFUE0E221R 20% (714) 373-7334
C1: AVX TAJA475M020R 20V 20% (207) 282-5111
L1: MURATA LQH32CN100K11 OR SUMIDA CDRH3D16100 (814)237-1431

Figure 2. 1.8V to 1.5V, 4A very low dropout linear regulator (typical dropout voltage is 65mV at 4A)

LT3150 Features

- ❑ Fast transient response optimized with ceramic output capacitors
- ❑ MOSFET $R_{DS(ON)}$ defines dropout voltage
- ❑ ±1% reference tolerance over temperature
- ❑ Multifunction LDO shutdown pin with latchoff
- ❑ Fixed frequency 1.4MHz boost converter generates MOSFET gate drive
- ❑ Current mode PWM boost converter uses tiny capacitors and inductor
- ❑ Independent boost converter shutdown pin permits LDO V_{OUT} supply sequencing
- ❑ Available in 16-Lead SSOP package

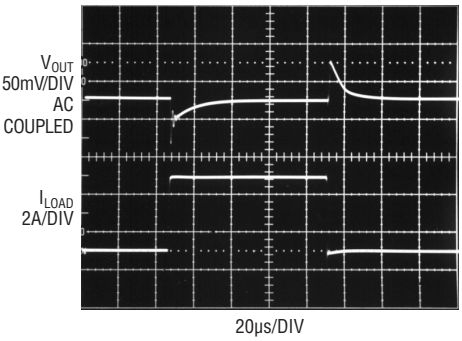


Figure 3. Transient response for a 0.1A to 4A output load step

loop frequency compensation tailored to Q1 and C_{OUT}'s characteristics. Given a worst-case maximum input supply voltage of 1.9V and 4A maximum load current, the Si4410 dissipates 1.6W. Temperature rise in Q1 is about 40°C. No airflow or additional heatsinking beyond that provided by a proper PCB layout is required.

No R_{SENSE} Current Limit

The circuit shown in Figure 2 does not provide any output current limiting under a fault condition. In this scenario, the DC/DC converter generating the 1.8V input supply is the only source of protection and the assumption is that it provides current limiting. Figure 4 shows a solution for users who need further protection but don't want to impact dropout voltage with the loss across a sense resistor. This circuit utilizes the LT3150 No R_{SENSE}™ current limit scheme, which employs a programmable timer. The user sets a time-out period, via C4 at the SHDN2 pin, that limits the duration of a fault condition before latching the VLDO controller off.

The I_{NEG} pin connection to ground activates the No R_{SENSE} internal circuitry. A fault condition, such as an output short circuit, starts the timer at the SHDN2 pin because internal circuitry detects that the GATE pin is driven to within 1V (typically) of the positive rail. During the time-out period, C5's reservoir provides power to the I_{POS} pin's internal circuitry. D2 reverse-biases if V_{IN} is in current limit and its voltage collapses. After exceeding the time out period, V_{OUT} is shut down and latched off. To restore normal operation, reset the timer capacitor with an active pulldown or cycle power to the V_{IN2} pin while providing an external bleed path for the timer capacitor.

Note that this technique does not limit the MOSFET current during the time-out period. Only the input power supply and the input-to-output impedance limit output current. The timer period is set to keep Q1 within its SOA (safe operating area) and its temperature rise under control. Savvy engineers will recognize that this technique imposes two restrictions; a very slow input supply ramp and operation in dropout both activate the timer. Applying the input supply of 1.8V within 50ms starts this circuit properly. Also, a logic signal at the $\overline{SHDN1}$ pin provides on/off control and provides power supply sequencing for the LDO output. As an example, holding this pin low until the 1.8V supply is stable eliminates the input supply startup ramp considerations for the 1.5V supply.

Conclusion

An LT3150-based solution is a cost- and space-saving alternative to a switching regulator in low output voltage applications down to 1.2V. The LT3150 combines the benefits of low input voltage operation, very low dropout voltage performance, precision regulation and fast transient response. The LT3150 drives a variety of MOSFET pass elements, making it simple to scale output power and dropout performance.

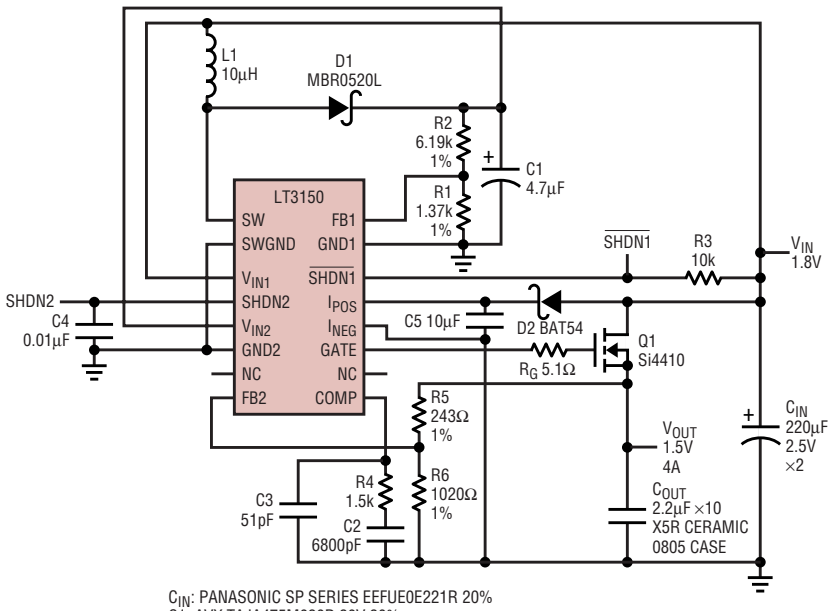


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Figure 4. 1.8V to 1.5V, 4A VLDO linear regulator with No R_{SENSE} current limiting and on/off control