LT1468: An Operational Amplifier for Fast, 16-Bit Systems

by George Feliz

Introduction

The LT1468 is a single operational amplifier that has been optimized for accuracy and speed in 16-bit systems. Operating from ±15V supplies, the LT1468 in a gain of −1 configuration will settle in 900ns to 150µV for a 10V step. The LT1468 also features the excellent DC specifications required for 16-bit designs. Input offset voltage is 75µV max, input bias current is 10nA maximum for the inverting input and 40nA maximum for the noninverting input and DC gain is 1V/µV minimum. The LT1468 specifications are summarized in Table 1. Two key applications that illustrate its use are current-to-voltage (I/V) conversion following a fast, 16-bit current output digital-to-analog converter (DAC), such as LTC1597 (Figure 1), and buffering the input of an analog-to-digital converter (ADC), such as the 333ksps LTC1604 (Figure 2). Both applications will be discussed in detail to highlight the LT1468 design requirements and trade-offs.

16-Bit DAC Current-to-Voltage Converter with 1.7µs Settling Time

The key AC specification of the circuit of Figure 1 is settling time as it limits the DAC update rate. The settling time measurement is an exceptionally difficult problem that has been ably addressed by Jim Williams, beginning in the August 1998 issue

and concluding in this issue of *Linear Technology* magazine and, in greater detail, in Linear Technology Application Note 74. Minimizing settling time is limited by the need to null the DAC output capacitance, which varies from 70pF to 115pF, depending on code. This capacitance at the amplifier input combines with the feedback resistor to form a zero in the closed-loop frequency response in the vicinity of 200kHz–400kHz. Without a feedback capacitor, the circuit will oscillate. The choice of 20pF stabilizes the circuit by adding a pole at 1.3MHz to limit the frequency peaking and is chosen to optimize settling time. The settling time to 16-bit accuracy is theoretically bounded by 11.1 time constants set by the 6kΩ and 20pF. Figure 1's circuit settles in 1.7µs to 150µV for a 10V step. This compares favorably with the 1.33µs theoretical limit and is the best result obtainable with a wide variety of LTC and competitive amplifiers. This excellent settling requires the amplifier to be free of thermal tails in its settling behavior.

The LTC1597 current output DAC is specified with a 10V reference input. The LSB is 25.4nA, which becomes 153µV after conversion by the LT1468, and the full-scale output is 1.67mA, which corresponds to 10V at the amplifier output. The zero-scale offset contribution of the LT1468 is the input offset voltage and the

inverting input current flowing through the 6k feedback resistor. This worst-case total of 135µV is less than one LSB. At full-scale there is an insignificant additional 10µV of error due to the 1V/µV minimum gain of the amplifier. The low input offset of the amplifier ensures negligible degradation of the DAC's outstanding linearity specifications.

With its low 5nV/√Hz input voltage noise and 0.6pA/√Hz input current noise, the LT1468 contributes only an additional 23% to the DAC output noise voltage. As with any precision application, and particularly with wide bandwidth amplifiers, the noise bandwidth should be minimized with an external filter to maximize resolution.

ADC Buffer

The important amplifier specifications for an analog-to-digital converter buffer application (Figure 2) are low noise and low distortion. The LTC1604 16-bit ADC signal-to-noise ratio (SNR)
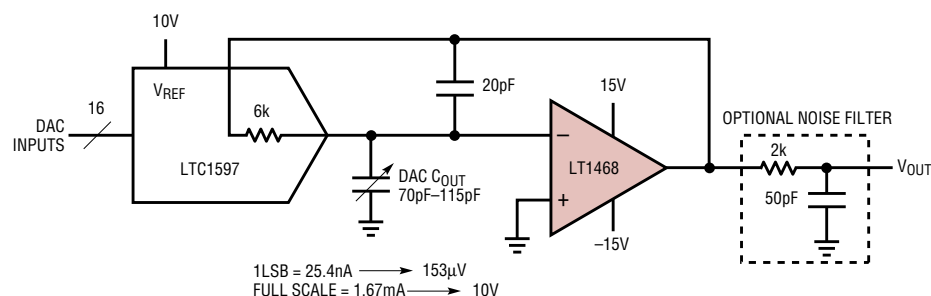
Table 1. LT1486 key specifications	
Input Offset Voltage	75µV Max
Inverting Input Bias Current	10nA Max
Noninverting Input Bias Current	40nA Max
DC Gain	1V/µV Min
CMRR	96dB Min
Input Noise Voltage	5nV/√Hz
Input Noise Current	0.6pA/√Hz
Gain Bandwidth	90MHz
Slew Rate	22V/µs
THD for 10V$_{P-P}$, 100kHz	−96.5dB
DAC Settling Time to 150µV, 10V Step (Figure 1's Circuit)	1.7µs
A$_V$ = −1 Settling Time to 150µV, 10V Step	900ns
Supply Current, V$_S$ = ±15V	5.2mA Max

Figure 1. 16-bit DAC I/V converter with 1.7µs settling time

Figure 2. ADC buffer

Figure 4. LT1468 gain and phase vs frequency
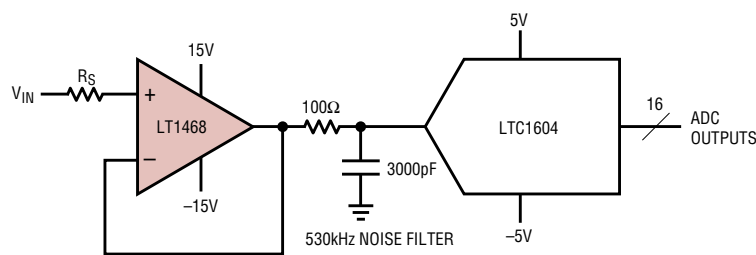
of 90dB implies $56\mu V_{RMS}$ noise at the input. The noise for the amplifier, $100\Omega/3000pF$ filter and a high value $10k\Omega$ source is $15\mu V_{RMS}$, which degrades the SNR by only 0.3dB. The LTC1604 total harmonic distortion (THD) is a low –94dB at 100kHz. The buffer/filter combination alone has 2nd and 3rd harmonic distortion better than –100dB for a $5V_{P-P}$, 100kHz input, so it does not degrade the AC performance of the ADC.

The buffer also drives the ADC from a low source impedance. Without a buffer, the LTC1604 acquisition time increases with increasing source resistance above 1k and therefore the maximum sampling rate must be reduced. With the low noise, low distortion LT1468 buffer, the ADC can be driven at maximum speed from higher source resistances without sacrificing AC performance.

The DC requirements for the ADC buffer are relatively modest. The input offset voltage, CMRR (96dB minimum) and noninverting input bias current through the source resistance, R_S, affect the DC accuracy,

but these errors are an insignificant fraction of the ADC offset and full-scale errors.

Circuit Description

A simplified schematic of LT1468 is shown in Figure 3. The circuit is a single, folded-cascode gain stage for fast settling and high bandwidth. The inputs are PNP transistors Q1 and Q2 with bias current cancellation from current source I7–Q12 to match Q1 and Q2, and the current mirror composed of Q13, Q14 and Q15. I7 is trimmed to minimize the inverting input current (critical for errors in DAC I/V circuits). The input devices are protected by 100Ω resistors and back-to-back diodes D1 and D2. The collectors of Q1 and Q2 are loaded by current sources I3 and I4 and the emitters of cascode transistors Q3 and Q4. I3 and I4 are trimmed to null the input offset voltage.

The mirror formed by Q5 and Q6 performs differential-to-single ended conversion into the high gain node at the collectors of Q4 and Q6. To increase the gain of this single stage,
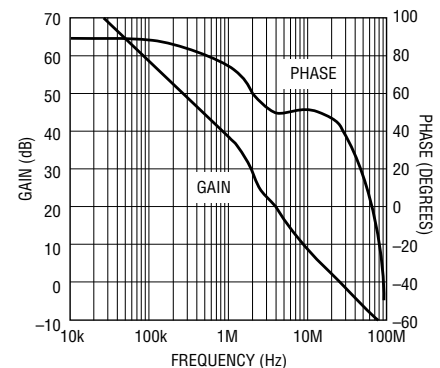
the Q5–Q6 mirror is bootstrapped by follower Q7 and current source I2 so that the mirror floats with the output level. With this scheme, Q6 never sees a change in base-collector voltage and does not degrade the gain with its output impedance, which is a factor of 5–10 lower than that of NPNs Q3 and Q4. By choosing I2 so that Q7 runs at twice the collector current of Q5–Q6, the base current of Q7 balances the combined base currents of Q5 and Q6. A benefit of this balanced design is low offset voltage drift ($2\mu V/°C$ maximum).

The output stage is formed by Q8, Q9, Q10 and Q11 and current sources I5 and I6. This stage further buffers the gain node from the output. The path from the emitter of Q7 to the output has symmetrical current gain, as it contains both an NPN and PNP, whether sourcing or sinking current. This balance reduces 2nd harmonic distortion.

Frequency compensation is set by capacitor C1 on the gain node for a 90MHz gain bandwidth at 100kHz. Capacitor C2 rolls off the mirror gain, which produces a pole-zero pair so that the open-loop response reaches unity gain at 25MHz with 42° of phase margin. C2 is bootstrapped to the output so that it does not degrade slew rate. The gain and phase versus frequency are shown in Figure 4. Slew rate is set by I1 and C1 and is typically $22V/\mu s$.

Design Trade-Offs

Previous precision designs had multiple gain stages and highly balanced configurations. The price paid by these classic designs is lack of
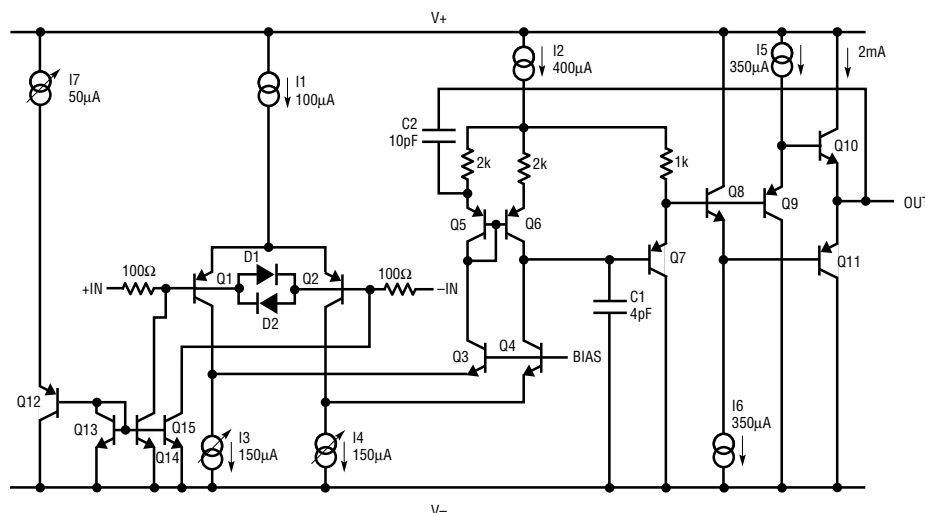

Figure 3. LT1468 simplified schematic

bandwidth, slew rate and settling time. The LT1468 uses a single stage topology to obtain excellent AC specifications with high bandwidth and state-of-the-art 16-bit settling. The demands of precision dictate a fully balanced design and painstaking care in the die layout. The AC performance is ultimately limited, however, by the need for high gain and low input bias current. High gain requires bootstrapping the current mirror in the signal path, which degrades phase margin at high frequency. For this reason the mirror is compensated to lower the unity-gain frequency of the amplifier, which reduces bandwidth at low closed-loop gains.

To obtain low input bias current, the choice of operating currents is limited by the accuracy of the input bias current cancellation circuitry. With trimming, up to a 50× reduction
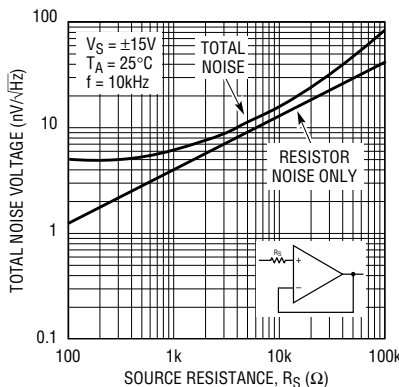

Figure 5. Total noise vs unmatched source resistance

in I_B can be achieved. This constraint sets the maximum value of current source I1, which also places limits on bandwidth, slew rate, noise voltage and noise current. The LT1468 total noise is best with source resistance in the 1kΩ to 20kΩ region, where any

increase in noise is due to the resistor (Figure 5).

It should be noted that the input bias current cancellation current is not bootstrapped to the input stage to provide constant I_B vs input common mode voltage. The reason is simple: this circuitry runs at submicroamp current levels and has no chance of settling if it is allowed to move with the inputs. The I_B is optimized for inverting configurations with a constant input voltage and provides excellent settling.

Conclusion

The LT1468 has an unequaled blend of speed and precision that is ideal for 16-bit applications. Its unique virtues also provide outstanding performance in low distortion active filters and precision instrumentation. *LT*