An Optimized, Low Distortion, Lower Power ADSL Line Driver Using the LT1207

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Introduction

High speed ADSL modems require high output voltage/current, high speed operational amplifiers to deliver large signals under peak conditions depending upon the characteristics of the line code used. In the ADSL market, two prevalent codes are in use: DMT (discrete multitone) and CAP (carrierless amplitude/phase) modulation. DMT modulation uses a large number of phase-locked carriers to transmit data over cable. As a result, current DMT systems for ADSL exhibit high crest factors (peak to RMS) of 5.33:1. CAP-based systems, on the other hand, use single-carrier modulation and exhibit lower crest factors of 3:1. In these ADSL systems, data is transmitted over two separate frequency bands and at different RMS power levels. The lower frequency band, labeled "upstream," is defined by a 30kHz to 140kHz spectral band with the upper frequency band, labeled "downstream," defined by a 170kHz to 1.5MHz spectral band. In these systems, the RMS signal power transmitted over the downstream band is 20dBm. The RMS signal power transmitted over the upstream band is 13dBm and the reference impedance level for ADSL systems in general is 100Ω.

Even though the transmitted RMS power is fairly low, large crest factors produce large peak signal/power levels that must be cleanly processed to avoid bit-error-rate degradation. DMT systems require 70dBc dynamic performance under peak conditions; CAP-based systems require 60dBc dynamic performance. Table 1 summarizes peak voltage and current levels required for DMT- and CAP-based systems.

To handle these peak signal levels, current solutions in the marketplace use amplifiers with very high quiescent currents—35mA or more. To generate the required peak output voltage drive, these amplifiers are commonly operated from ±15V supplies and, as a result, can produce a zero-load power dissipation over 1 Watt. It is this high static power dissipation that prevents modem manufacturers from implementing multiline modem cards in the central office because of the large amount of PC board area required to heat sink the device.

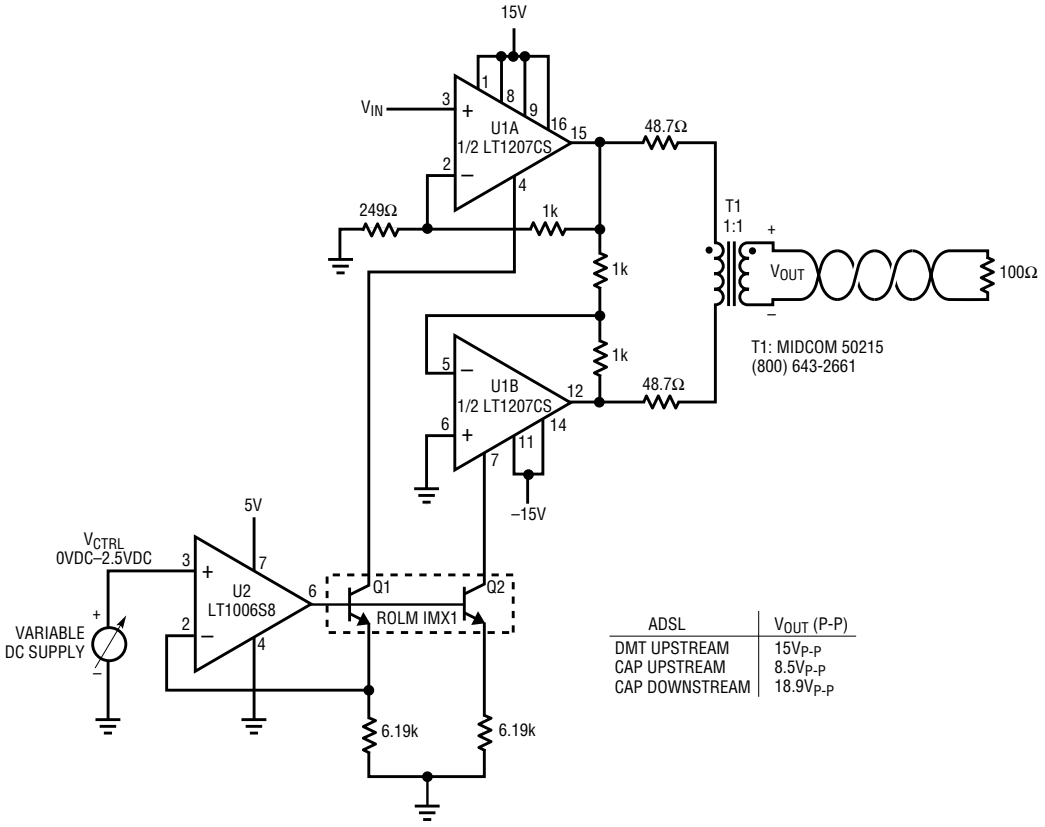

Figure 1. A versatile, high performance, LT1207-based differential ADSL transmitter with amplifier quiescent current control

Table 1. Peak voltage and current levels for DMT- and CAP-based systems

ADSL	Nominal Transmit Power	Peak Voltage	Peak Current
DMT Upstream	13dBm	$15V_{P-P}$	$150mA_{P-P}$
CAP Upstream	13dBm	$8.5V_{P-P}$	$85mA_{P-P}$
CAP Downstream	20dBm	$18.9V_{P-P}$	$189mA_{P-P}$

The circuit in Figure 1 builds upon differential line driver design ideas first illustrated in the May 1996 issue of *Linear Technology* magazine[1] with a twist to address the issue of static and dynamic power dissipation in line-driver amplifiers.

Line-Driver Quiescent Current Control

Line-driver amplifiers expend a significant amount of power to deliver signal power to the load (otherwise known as dynamic power dissipation). Of the total power dissipated by an amplifier, 50% to 60% of the power consumed can come from static power dissipation. Reducing the quiescent power without sacrificing speed or performance allows the line driver circuit to run cooler and use less pc board area—two factors that are very important in the implementation of multiline high speed modem cards.

A unique feature in the LT1207 family of CFAs (for example, the LT1210 and the LT1206) is the ability to control amplifier quiescent current via the SHUTDOWN pin. Originally intended to be used with an external resistor connected to GND or with an open-collector/-drain device under digital control, a programmable current sink can be used to change the bias current to properly match the power dissipation in the amplifiers to the dynamic requirements of the application.

To use this feature, an amplifier-quiescent-current control loop circuit has been added to the basic differential line driver circuit shown in Figure 1. The control loop consists of U2, Q1/Q2 (a dual matched NPN transistor), and a pair of 6.19k resistors. These components are combined to form two matched current sinks designed to operate from 0µA to 400µA. Over this control current range, the quiescent current of the LT1207's internal CFAs can be set from 200µA to 18mA each.

A DC voltage of 0V to 2.5V is applied to U2's noninverting input to set amplifier quiescent current. As designed for the LT1207CS, the control circuit's transfer characteristic is 7.2mA/V. Thus, a zero-volt setting on V_{CTRL} places both amplifiers in a shutdown state, where the amplifier supply current drops to less than 200µA for each. A 2.5V setting on V_{CTRL} biases both amplifiers to their maximum supply current. If a DC voltage source or a voltage-output DAC is not available for the control circuit, a housekeeping microcontroller's timer output can generate a PWM signal that can be filtered and then used as the DC control voltage.

Performance

The circuit in Figure 1 was evaluated at each of the three peak output levels shown in the table. For ADSL upstream applications, a 100kHz single-tone sine wave was used to evaluate the line driver's harmonic distortion performance as a function of amplifier quiescent current control. In each of the three cases, the output signal was attenuated to obtain maximum sensitivity from the HP4195A network analyzer used for the measurements.

Figure 2 illustrates the dynamic performance of the line driver circuit at an output level of $15V_{P-P}$ into the 100Ω load. The 3rd order harmonic distortion (3HD) is approximately 70dBc (sufficient for peak-power DMT remote-terminal operation); this was achieved with an amplifier quiescent current of 6mA each. With an output level of $8.5V_{P-P}$ for CAP-based remote-terminal applications, the circuit exhibits 64dBc dynamic performance (shown in Figure 3), with the line-driver amplifiers operating at 2mA each. The presence of a pronounced 2nd order artifact (2HD) is indicative of current starvation in the line-driver amplifier core. Incrementally increasing the supply current of the amplifier is effective in reducing this 2nd order harmonic distortion.

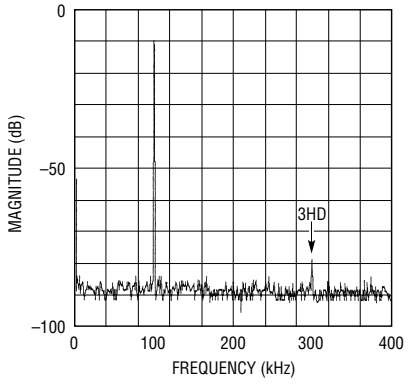

Figure 2. Harmonic distortion performance of Figure 1's circuit with a 100kHz sine wave at $15V_{P-P}$ into 100Ω

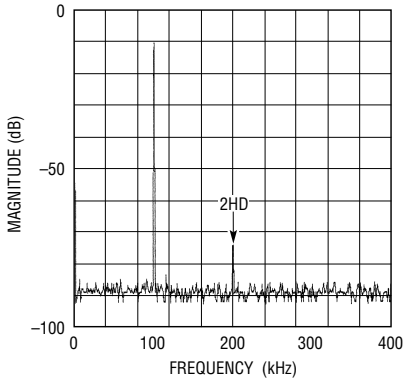

Figure 3. Harmonic distortion performance of Figure 1's circuit with a 100kHz sine wave at $8.5V_{P-P}$ into 100Ω

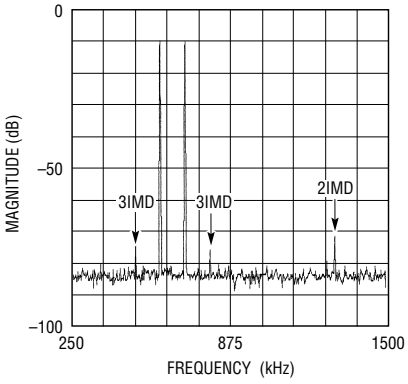

Figure 4. 2-tone intermodulation distortion performance of Figure 1's circuit (See text for additional details.)

Although single-tone distortion measurements are a good indicator of circuit performance in single-carrier applications, they do not provide any insight into amplifier linearity when processing more that one tone at a time. An effective tool in gauging dynamic performance in these applications is 2-tone intermodulation. Figure 4 illustrates the performance of Figure 1's circuit with two sine waves at 600kHz and 700kHz. The frequency spectrum displayed is representative of both DMT and CAP downstream operation, and the two tones were chosen to show both 2nd and 3rd order IMD products (2IMD and 3IMD) that fall in-band. With a 1:1 turns-ratio transformer, the output level of the circuit was adjusted to produce an $18.9V_{P-P}$ envelope across the 100Ω load. This output voltage level implies a peak differential voltage across the line driver outputs of approximately $38V_{P-P}$. With each amplifier operating at a supply current of 13mA, the circuit achieves a spur-free dynamic performance of 63dBc, sufficient for peak power operation in CAP-based systems. Improved performance at lower supply currents can be achieved with a transformer turns ratio greater than 1:1, whereby amplifier output current drive is substituted for amplifier output voltage drive.

Conclusion

Under DC voltage or digital control, the quiescent supply current of the line-driver CFAs can be adjusted (statically or dynamically) to reduce their static power dissipation without sacrificing either downstream or upstream dynamic performance. In addition, this supply-current control can be coupled with a reduction of the line-driver supply voltage to reduce an amplifier's dynamic power dissipation. The supply voltage should not be reduced below a level that causes the amplifier output stage to clip the peak transmitted signal, however. The best method for gauging dynamic performance is to monitor the bit-error-rate (BER) performance of the modem. Under normal DMT or CAP operation (downstream or upstream), the supply voltage and quiescent currents of the line-driver amplifiers can be reduced until the system BER degrades beyond an acceptable minimum.

For additional information on a complete line of driver solutions, featuring the LT1210 (1.1A), the LT1206 (250mA) and the LT1497 (125mA), please consult the LTC factory.

Note:

[1] Hoskins, Kevin. "The LT1207: An Elegant Dual 60MHz, 250mA Current Feedback Amplifier." *Linear Technology* VI:2 (May 1996), pp. 9–13.