Multichannel, 3V and 5V, 16-Bit ADCs Combine High Performance, Speed, Low Power and Small Size

by Ringo Lee

Introduction

Many of today's data acquisition applications require low-power and/or remote sensing capabilities while occupying a minimum amount of board space. Linear Technology introduces a pin-compatible family of 12-bit and 16-bit A/D converters that meet these requirements. The flagship device of this new family is the LTC1867. It consists of an 8-channel analog input multiplexer (MUX), a high performance and lower-power 16-bit switched capacitor A/D converter, a simple serial I/O, and fits in a small 16-pin narrow SSOP package (5mm × 6mm footprint).

Product Features

- Sample Rate: 200ksps (LTC1867); 175ksps (LTC1867L)
- 16-Bit No Missing Codes
- 8 Single-Ended or 4 Differential Channels
- SPI/MICROWIRE™ Serial I/O
- On-Board or External Reference
- Low Power Operation: 1.3mA (LTC1867); 0.75mA (LTC1867L)
- Automatic Nap and Sleep Modes
- 16-Pin Narrow SSOP Package

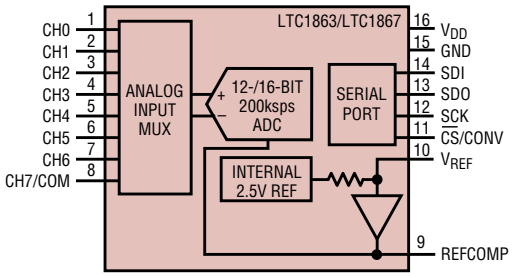

Figure 1. The simplified block diagram of the LTC1863 and LTC1867, which include a programmable 8-channel input multiplexer, 16-bit switched capacitor ADC and an on-board reference.

Table 1 identifies the differences between the four members of this new family of high performance A/D converters. The members are classified according to supply voltage and resolution. The 16-bit LTC1867 and the 12-bit LTC1863 operate on a single 5V supply while sampling at 200ksps. The LTC1867L and the LTC1863L operate on a reduced 3V supply with the same features of the LTC1867 and the LTC1863, respectively. The LTC1867L and LTC1863L key specifications are guaranteed for 2.7V operation. In addition, all four parts provide an automatic Nap mode, Sleep mode, unipolar and bipolar operation, and an internal bandgap reference. Figure 1 shows a block diagram for the LTC1867/LTC1863.

Table 1. LTC1867 Family Members

Part Number	LTC1867	LTC1863	LTC1867L	LTC1863L
V_{DD}	5V	5V	3V	3V
Resolution	16-Bit	12-Bit	16-Bit	12-Bit
f_{SAMPLE}	200ksps	200ksps	175ksps	175ksps
Input Ranges	0V–4V, ±2V	0V–4V, ±2V	0V–2.5V, ±1.25V	0V–2.5V, ±1.25V
Supply Current	1.3mA	1.3mA	0.75mA	0.75mA
INL (Unipolar)	±2LSB	±1LSB	±3LSB	±1LSB
INL (Bipolar)	±2.5LSB	±1LSB	±3LSB	±1LSB
No Missing Codes	YES	YES	YES	YES

MUX Configuration

The eight-channel analog input multiplexer can be selected either in 4 differential pairs, 8 single-ended, 7 single-ended channels versus COMMON pin (pin 8, CH7/COM acts as COMMON MINUS) or combinations thereof. These configurations are set up by a 7-bit input word defined in Table 2 through the SDI/SCK serial port. The channel-to-channel matching for offset and gain error are excellent. For the LTC1867, the offset error match and gain error match are both specified as ±2LSB (max). The crosstalk between channels is typically better than 110dB. Figure 2 illustrates the flexibility of the 8-channel MUX.

Unipolar and Bipolar Mode

These A/D converters can sample the difference of positive input ($+V_{IN}$) and negative input ($-V_{IN}$) at the same instant either in unipolar or bipolar modes depending on UNI bit of the Input Word. For the LTC1867 and LTC1863, the input ranges (i.e. $+V_{IN}$ minus $-V_{IN}$) are 0V to 4V in unipolar mode and ±2V in bipolar mode. For example, the $+V_{IN}$ can swing from 0V to 4V if $-V_{IN}$ is tied to Ground in unipolar mode, and the $+V_{IN}$ can swing from

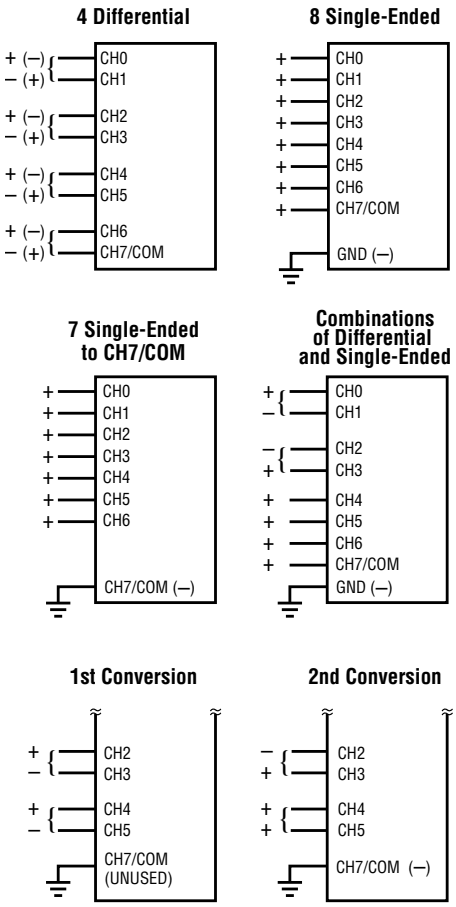

Figure 2. These examples show the flexibility of the LTC1867 8-channel input multiplexer.

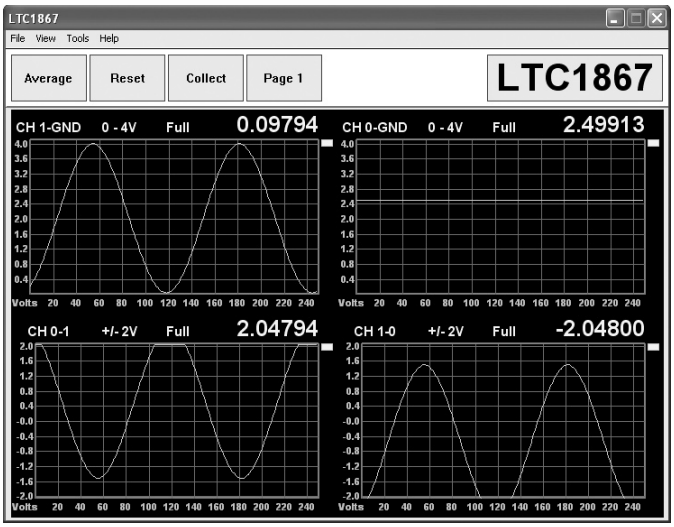

Figure 3. The upper two traces show the digitized results from the LTC1867 operating in the unipolar mode with signals applied to Channel 1 and Channel 0. The lower traces demonstrate how the results are changed when LTC1867 is configured to operate in the bipolar mode with the same signals applied to Channel 1 and Channel 0.

0.5V to 4.5V if $-V_{IN}$ is tied to 2.5V in bipolar mode.

Figure 3 depicts the unipolar and bipolar operation for the LTC1867. On the upper half of Figure 3, the LTC1867 samples and digitizes a sinewave on Channel 1 (CH1) that swings from 0V to 4V and measures a DC voltage of 2.5V on Channel 0 (CH0), both in unipolar mode. On the lower half of Figure 3, the ADC performs a bipolar operation with CH0 versus CH1, and vice versa. Under these conditions the differential input signals applied to the ADC exceed the bipolar input range of ±2V. For example, in the case of CH0 minus CH1 the resulting digitized input range will be –1.5V to 2.0V.

In both unipolar and bipolar operation, $+V_{IN}$ and $-V_{IN}$ are sampled simultaneously; so common mode noise on both inputs is rejected by the truly differential inputs. In the unipolar mode, the $+V_{IN}$ range of the LTC1867 is from 0V to V_{DD} and the $-V_{IN}$ range is from 0V to $V_{DD}/2$. Some competing devices only allow the minus input to reach a few hundred millivolts to one volt above ground. By comparison the LTC1867 offers about twice the range on the minus input. This makes the LTC1867 a great choice for remote applications where large common mode voltages can be present. In the bipolar mode, both $+V_{IN}$ and $-V_{IN}$ can accept signals from 0V to V_{DD}.

Table 2. 7-Bit Input Word (SD = MSB)

SD	OS	S1	S0	COM	UNI	SLP

1. SD = SINGLE/$\overline{\text{DIFFERENTIAL}}$ BIT
2. OS = ODD/$\overline{\text{SIGN}}$ BIT
3. S1 = ADDRESS SELECT BIT 1
4. S0 = ADDRESS SELECT BIT 0
5. COM = CH7/COM CONFIGURATION BIT
6. UNI = UNIPOLAR/$\overline{\text{BIPOLAR}}$ BIT
7. SLP = SLEEP MODE BIT

Simple Serial I/O Allows Easy Isolated or Remote Applications

The serial I/O employed by the LTC1867 and its other family members is compatible with the industry standard SPI/MICROWIRE interface. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both the transmitting and receiving systems. After the conversion is complete, the input word is shifted into the ADC through the SDI/SCK ports, and at the same time, data bits are

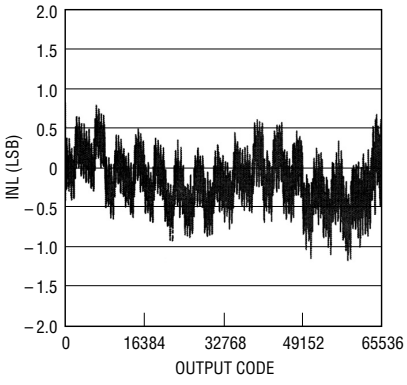

Figure 4. The DC accuracy of the LTC1867 is shown in the INL curve. The accuracy is achieved with capacitor matching, which is very stable over time and temperature.

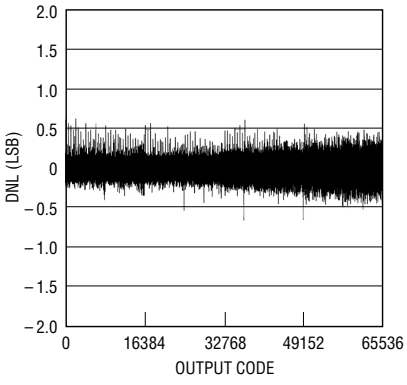

Figure 5. No missing codes and very accurate capacitor matching found in the LTC1867 DAC is illustrated by the DNL curve.

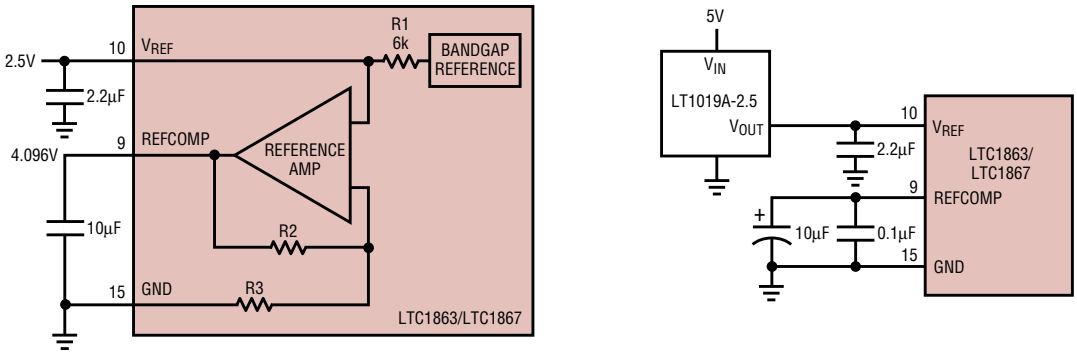

Figure 6. LTC1863/LTC1867 reference circuit. The internal reference can be overdriven by an external Reference, LT1019A-2.5 for better drift and/or accuracy performance.

released through the SDO/SCK ports. The A/D converter starts to acquire the analog input signals after reading in the 7-bit Input Word. These ADCs have an internally trimmed conversion clock which allows the sampling frequency to approach DC without affecting the conversion results. The 4-wire interface allows the LTC1867 and its siblings to fit well with isolated or remotely located applications.

Outstanding DC and AC Performance

Operating from a 5V supply and sampling up to 200ksps, the LTC1867 delivers 16-bit, no missing codes performance with an accurate INL specification of ±2LSB(max) in unipolar mode and ±2.5LSB(max) in bipolar mode. Typical INL and DNL plots for LTC1867 versus output code are shown in Figures 4 and 5. This performance is achieved with capacitor matching which is very stable over time and temperature.

Along with outstanding DC performance, the LTC1867 also has very good AC performance. The signal-to-noise ratio (SNR) is typically 89dB with an input range of 4V and improves to 90.5dB when an external reference

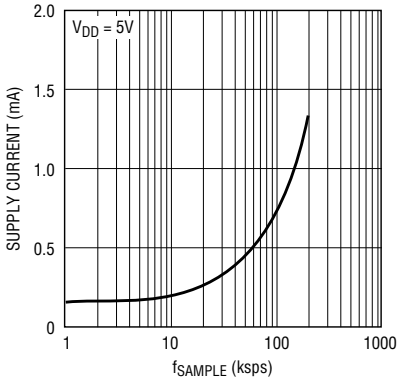

Figure 7. The LTC1867 features an Automatic Nap mode that cuts the power dissipation as the sampling frequency is reduced.

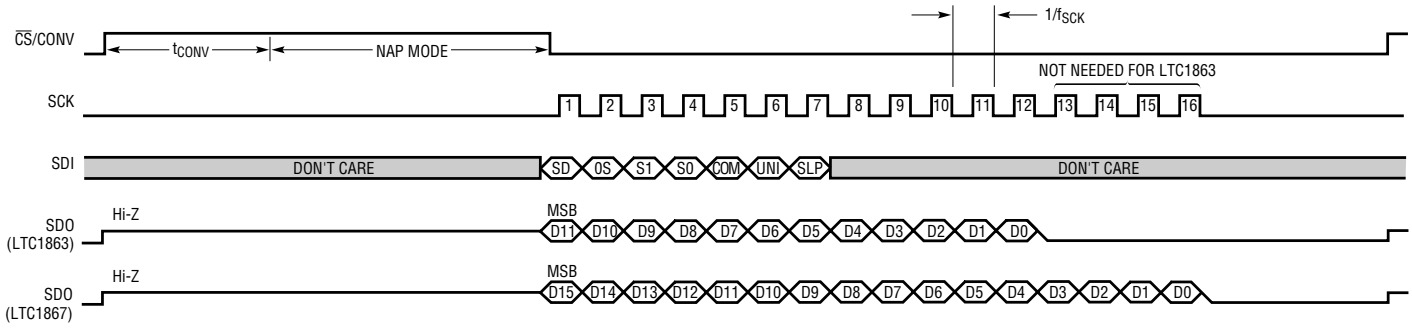

Figure 8. The Automatic Nap mode provides power reduction at reduced sample rates. This feature is activated when CS/CONV remains high after the conversion is completed.

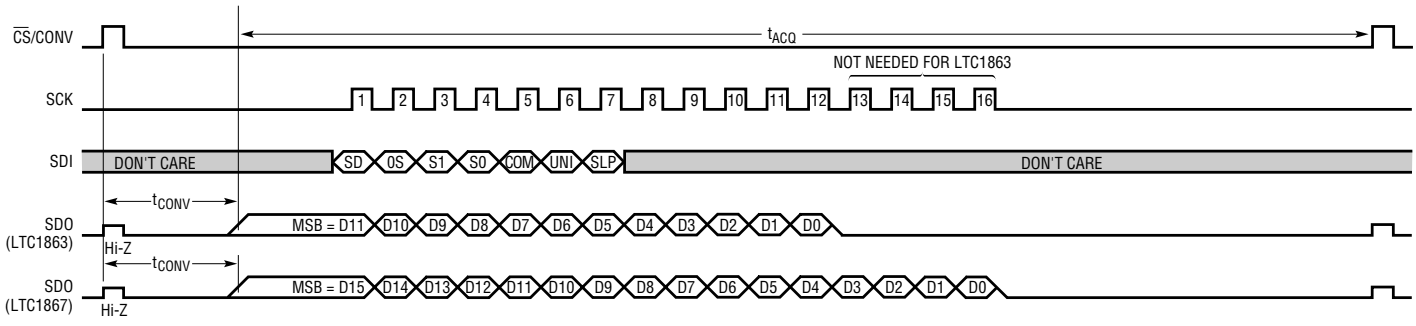

Figure 9. The Automatic Nap mode is not activated if the CS/CONV pulse is shorter than the conversion time. After the conversion the ADC remains powered up.

voltage of 5V is applied to the REFCOMP pin (tie V_{REF} pin to 0V to turn off internal reference buffer).

Internal Reference

This family has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.5V for the LTC1867 and the LTC1863, and 1.25V for the LTC1867L and the LTC1863L. The reference is internally connected to a reference amplifier and is available at V_{REF} (Pin 10). A 6kΩ resistor in the LTC1867 and the LTC1863 (3kΩ resistor for the LTC1867L and the LTC1863L) is in series with the output so that it can be easily overdriven by an external reference if better drift and/or accuracy are required as shown in Figure 6. The reference amplifier gains the V_{REF} voltage by 1.638 to 4.096V at REFCOMP (Pin 9). This reference amplifier compensation pin, REFCOMP, must be bypassed with a 10µF ceramic or tantalum in parallel with a 0.1µF ceramic for best noise performance.

Low Power Improves Battery Life

The LTC1867 and LTC1863 consume only 1.3mA at a sampling rate of 200ksps. As the sampling frequency is reduced, the converters use even less supply current with the automatic Nap feature. For example, the parts draw only 760µA and 200µA at sampling frequencies of 100ksps and 10ksps, respectively.

Automatic Nap mode is active when the $\overline{CS}$/CONV pulse width is longer than the conversion time of the A/D converter. The part goes to Nap mode automatically right after a conversion is completed and remains powered down (the ADC draws 150µA in Nap mode) as long as the $\overline{CS}$/CONV stays HIGH after conversion. The internal reference, however, is still active and provides a 2.5V output. In this way, the LTC1867/LTC1863 requires no additional wake up time before the next conversion is started. Figure 7 shows how the supply current is greatly reduced as the sample rate is decreased when using this feature.

The ADCs can also go into the Sleep mode during long inactive periods. In sleep mode the internal reference is also powered down, thus reducing the draw to leakage currents of less than 1µA. The wake up time out of the sleep mode is determined by how fast the reference bypass capacitors can be charged. The wake up time can be estimated with the values of bypass capacitor on V_{REF} and the on-chip resistor between the internal reference and V_{REF} pin. For the 16-bit LTC1867L, the wake up time can be estimated as:

(resistor value) • (bypass capacitor value) • (number of time constant needed to settle to 16-bit accuracy)

or (3k • 2.2µF • 11).

Typically with bypass capacitors of 2.2µF and 10µF on the V_{REF} and REFCOMP pins, this takes about 80ms for LTC1867L. However, if an external reference is used, the wake up time is less than 10ms.

When the $\overline{CS}$/CONV pulse is shorter than the conversion time, the ADCs stay powered up and the Automatic Nap mode is not activated. In this configuration, the digital output, SDO, becomes active after the conversion is completed. Figures 8 and 9 show the timing diagrams for the two cases described.

Conclusion

The LTC1867 family packs an 8-channel analog input multiplexer, low-power A/D converter, serial I/O, and an internal reference in a narrow 16-pin SSOP package. With outstanding DC and AC performance, and equipped with the automatic Nap and Sleep modes for power reduction, these complete A/D converters can be used in many space-sensitive as well as low power applications.

LT3724, continued from page 30

The current limit fold-back circuit provides additional control during the first few switch cycles of start-up, and provides reduced short-circuit output current. When the output is at ground, the diode/resistor clamp the VC pin to a value that corresponds to 25% of the programmed maximum current. This circuit is only active with V_{OUT} close to ground, and becomes completely disabled once the output voltage rises past about 10% regulation.

8V–16V to 24V, 50W Boost Converter

The 24V Boost converter shown in Figure 6 achieves over 95% conversion efficiency at 50W with less than 20 components. Because this is a boost converter, V_{CC} is driven by the input voltage to improve efficiency and lower power dissipation. Figure 7 shows efficiency and power loss vs load current.

Conclusion

The LT3724 is a feature packed DC/DC controller that is versatile enough to be configured to control multiple converter topologies. It offers a simple and inexpensive solution to regulating system voltages at high efficiencies over a wide input voltage range and wide load range.

The integrated high voltage regulator facilitates true single-supply operation. Burst Mode operation improves efficiency during light load and no load operation. The current mode control architecture allows for simple design of the power supply control loop and excellent transient response. Continuous current sensing protects the supply from being damaged during an over current or short circuit fault condition. The innovative soft start function limits output voltage overshoot and inrush current during startup, brownout or short circuit recovery.