Supply Tracking and Sequencing at Point-of-Load: Easy Design without the Drawbacks of MOSFETs

by Scott Jackson

Introduction

Multi-voltage electronics systems are often saddled with complex power supply voltage tracking or sequencing requirements, which, if not met, can result in system faults or even permanent failures in the field. The design difficulties in meeting these requirements are often compounded in distributed-power architectures where point-of-load (POL) DC/DC converters are scattered across PC board space, sometimes on different board planes. The problem is that power supply circuitry is often the last circuitry to be designed into the board, and it must be shoehorned into whatever little board real estate is left. Centralized sequencing-tracking solutions can work well, but when no significant contiguous space is left on a board and the system specifications are in flux, one wishes for a simple, drop-in, flexible option. That wish can be fulfilled with a tracking and sequencing solution that installs at the POL, and is tiny and versatile enough to be easily dropped into the board without disrupting the rest of the system design.

Wish Granted

The LTC2927 provides a simple and versatile solution in a tiny footprint for both tracking and sequencing without the drawbacks of series MOSFETs.

Each POL converter that must be tracked or sequenced can have a single LTC2927 placed at point-of-load as shown in Figure 1. By selecting a few resistors and a capacitor, the supplies are configured to ramp-up and ramp-down with a variety of voltage profiles. Figure 2 shows various tracking and sequencing scenarios, including concurrent voltage tracking (Figure 2a), offset tracking (Figure 2b), ratiometric tracking (Figure 2c), and supply sequencing (Figure 2d).

Many voltage tracking solutions use series MOSFETs, which adds an in-

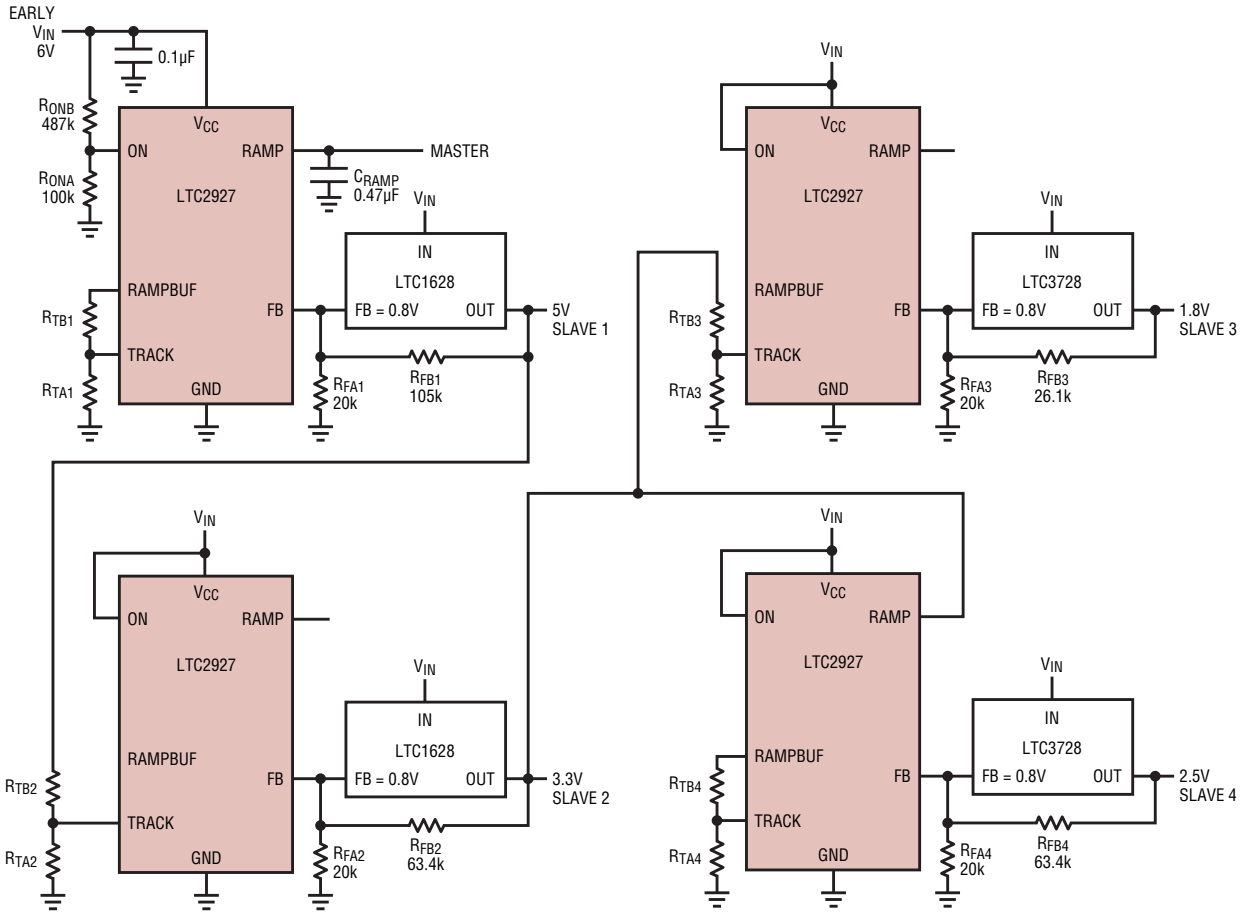
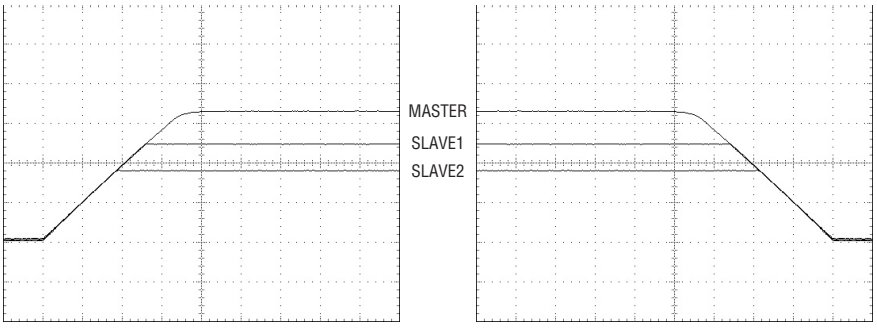
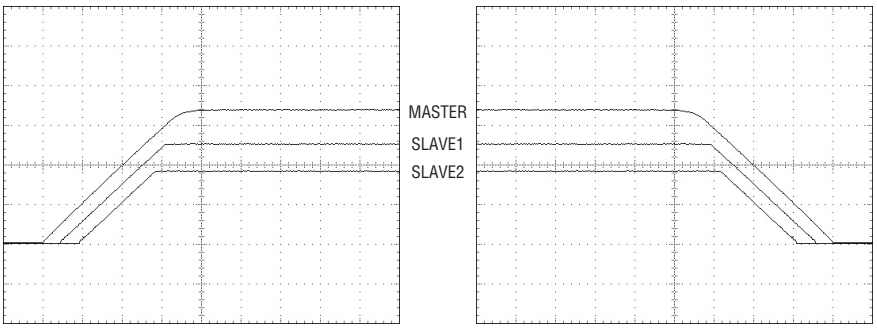


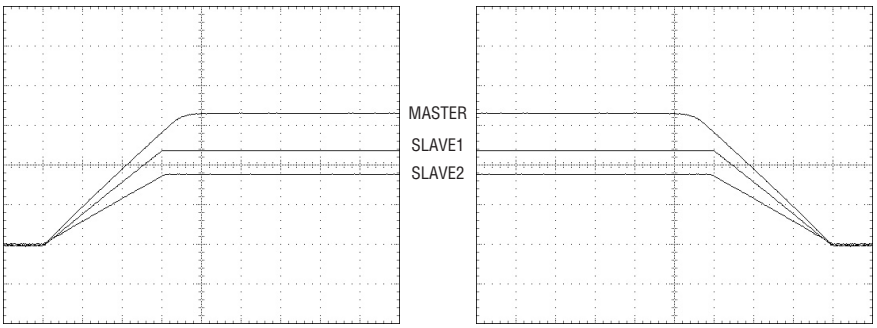
Figure 1. Typical tracking application



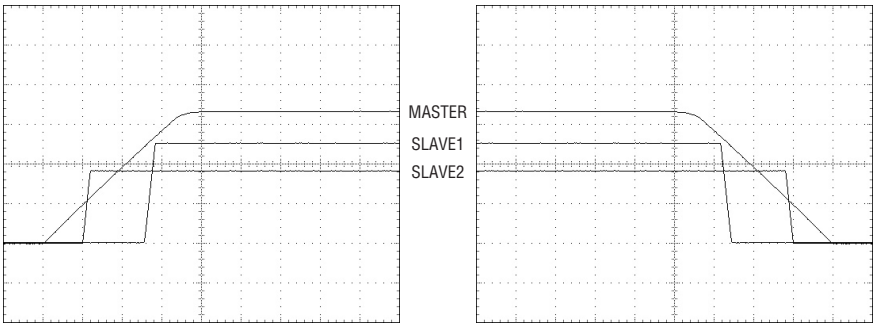
a. Coincident tracking



a. Offset tracking



c. Ratiometric tracking



d. Supply sequencing

Figure 2. Types of power supply voltage tracking

herent voltage drop, additional power consumption, and extra PC board real estate. Instead, the LTC2927 controls supplies by injecting current directly into the feedback nodes, thus controlling supply outputs without series MOSFETs. Figure 3 shows the simple "tracking cell" used to inject this current. *Furthermore, power supply stability and transient response remain unaffected because the injected current from the LTC2927 offsets the output voltage without altering the power supply control loop dynamics.*

Power supply tracking is straightforward with the LTC2927. A pair of resistors configures the behavior of a slave supply relative to a master signal. The choice of resistors can cause a slave supply to track the master signal exactly or with a different ramp rate, voltage offset, time delay, or combination of these.

A master signal is generated by tying a capacitor from the RAMP pin to ground or by supplying another ramping signal to be tracked as shown in Figure 1.

Examples

Consider a complex tracking system. The schematic in Figure 1 uses an LTC1628 dual synchronous step-down converter to produce 5.0V and 3.3V supplies and an LTC3728 dual synchronous step-down converter to produce 2.5V and 1.8V supplies from a 6.0V input. Four LTC2927s connected to the feedback nodes control the ramp-up and ramp-down behavior of these supplies. An early V_{IN} is supplied to the devices to guarantee correct operation prior to tracking the supplies.

The specification calls for the 5.0V and 3.3V supplies to track coincidently at ~20V/s, the 1.8V supply should ramp up quickly at 100V/s after the 3.3V supply reaches 2.0V, and the 2.5V supply should ramp up at the same rate as the 1.8V supply, but delayed by 20ms. The LTC2927 data sheet (available at www.linear.com) includes a 3-step design procedure that is followed for each supply. When using that procedure, use the following for equation (1) in Step 1, with a master signal ramp-rate S_M of 20V/s:

$$C_{RAMP} = \frac{10\mu A}{20\,V/s} \approx 0.47\mu$$

5V and 3.3V Supply Coincident Tracking

Because the master ramp rate is chosen to be equal to the desired ramp rate of the 5V and 3.3V supplies, coincident tracking is selected. If the feedback voltage of the switching power supply is 0.8V, as it is on the LTC1628, then coincident tracking can be configured by setting the tracking resistors equal to the feedback resistors (verified by

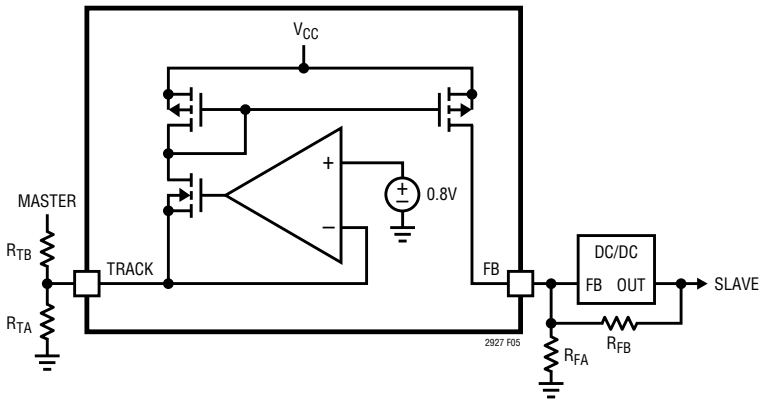


Figure 3. Simplified tracking cell

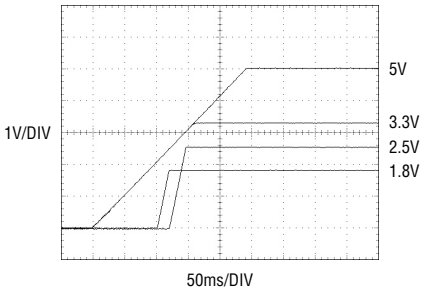


Figure 4. Output profile of the circuit in Figure 1

following Step 2 of the 3-Step Design Procedure),
From equation (2) of the 3-Step Design Procedure:

$R_{TB1} = R_{FB1} = 105k\Omega$
$R_{TB2} = R_{FB2} = 63.4k\Omega$

From Equation (3) of the 3-Step Design Procedure:

$R_{TA1}' = R_{FA1} = 20k\Omega$
$R_{TA2}' = R_{FA2} = 20k\Omega$

In the 3-step design procedure R_{TA}' represents the value of R_{TA} that produces no delay or offset. Since no delay is desired, $R_{TA} = R_{TA}'$, and Step 3 of the Design procedure is unnecessary.

1.8V and 2.5V Supply Sequencing

The 1.8V supply ramps up 2V below the 3.3V supply but at a ramp rate of 100V/s. Set the slave ramp rate to 100V/s in equation (2) to find R_{TB3}:

$$R_{TB3} = 26.1k\Omega \frac{21.3\,V/s}{100\,V/s} \approx 56.2k\Omega$$

Complete Step 2 by solving for R_{TA3}' using equation (3).

$R_{TA3}' = -10.755k\Omega$

Step 3 adjusts R_{TA3} for the desired delay between the 3.3V supply and the 1.8V supply. An offset of 2V results in a delay of ~100ms for the ramp rate chosen.

$R_{TA3}'' = 2.09k\Omega$

$R_{TA3} = R_{TA3}' \,||\, R_{TA3}''$
$\approx 2.61k\Omega$

The 2.5V supply has the same ramp rate as the 1.8V supply, but is delayed another 20ms. Repeating Step 2 and Step 3 for the 2.5V supply results in:

$$R_{TB4} = 43.2k\Omega \frac{21.3\,V/s}{100\,V/s} \approx 93.1k\Omega$$

$R_{TA4}' = -28.052k\Omega$

$R_{TA4}'' = 28.8k\Omega$

$R_{TA4} = R_{TA4}' \,||\, R_{TA4}''$
$\approx 3.24k\Omega$

The tracking profile for this system is shown in Figure 4.

Note that not every combination of ramp-rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to the master ramp rate must be reduced. In addition, the chosen resistor values should not require more than 1mA to flow from the TRACK and FB pins. Therefore, confirm that less than 1mA flows from TRACK when V_{MASTER} is at 0V.

$$I_{TRACK1} = \frac{V_{TRACK}}{R_{TA1} \,||\, R_{TB1}} = 0.05mA < 1mA$$

$$I_{TRACK2} = \frac{V_{TRACK}}{R_{TA2} \,||\, R_{TB2}} = 0.05mA < 1mA$$

$$I_{TRACK3} = \frac{V_{TRACK}}{R_{TA3} \,||\, R_{TB3}} = 0.45mA < 1mA$$

$$I_{TRACK4} = \frac{V_{TRACK}}{R_{TA4} \,||\, R_{TB4}} = 0.24mA < 1mA$$

The connections between each LTC2927 shown in Figure 1 allow extra control for each supply. With this system, the 3.3V supply uses the 5V supply as its master signal. If for some reason the 5V supply should collapse, the 3.3V supply follows it down. Likewise, the 1.8V and 2.5V supplies use the 3.3V supply as their master signal and track it up and down.

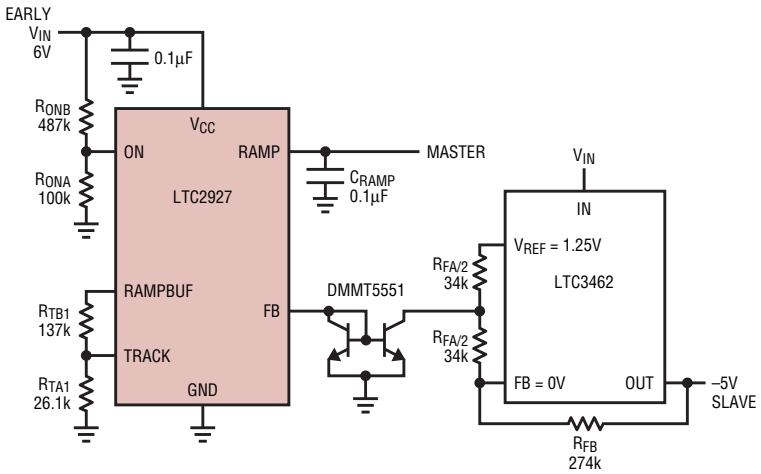
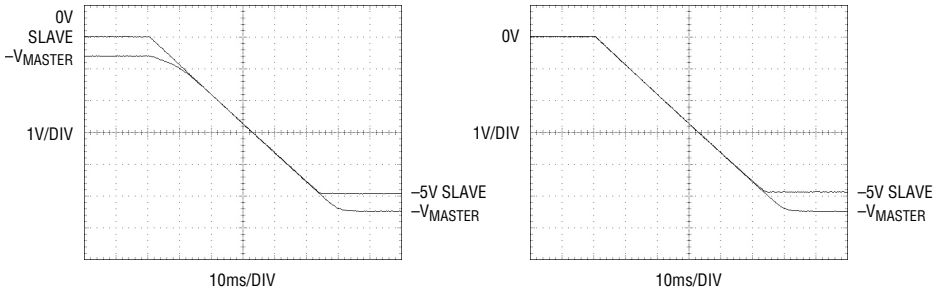


Figure 5. Supply tracking of GND referenced negative regulator



a. Tracking error due to current mirror pull-down limitation

b. Tracking without current mirror pull-down limitation

Figure 6. Output profile of circuit of Figure 9

Negative Supply Tracking

It is possible to track negative voltage regulators with the LTC2927. Figure 5 shows a tracking example using a LT3462 inverting DC/DC converter to produce a –5V supply. This converter has a ground-based reference, which allows current to be pulled from a node where R_{FA} has been divided in two. To properly pull current from the LT3462 FB network, a current mirror must be placed between the LTC2927 and the converter. The 3-Step design procedure remains the same with minor modifications to equations (2) and (3):

$$R_{TB} = \frac{R_{FB}}{2} \bullet \frac{S_M}{S_S}$$

$$R_{TA}' = \frac{V_{TRACK}}{\frac{2V_{REF}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}}}$$

All other equations remain the same.

Figure 6a shows the tracking profile of Figure 5 with a ramp rate of 100V/s. V_{MASTER} is positive, but the inverse is shown for clarity. The –5V slave does not pull all the way up to 0V at V_{MASTER} = 0V. This is because the ground referenced current mirror cannot pull its output all the way to ground. If the converter has a FB reference voltage greater than 0V or if a negative supply is available for the current mirror, the error can be removed. The resulting waveform is shown in Figure 6b.

Conclusion

The LTC2927 simplifies power supply tracking and sequencing by offering superior performance in a tiny point-of-load area. A few resistors can configure simple or complex supply behaviors. Series MOSFETs are eliminated along with their parasitic voltage drops and power consumption. The LTC2927 offers all of these features in a tiny 8-lead ThinSOT™ and 8-lead (3mm × 2mm) DFN package.

LTC3417, continued from page 8

ESR generates a loop zero at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects, requiring the designer to check loop stability over the operating temperature range. For these reasons, great care must be taken when using only ceramic input and output capacitors. The LTC3417 helps solve loop stability problems with its OPTI-LOOP phase compensation adjustment, allowing the use of ceramic capacitors. For details, and a process for optimizing compensation components, see Linear Technology Application Note 74 (AN76).

Although the LTC3417 is capable of operating at 4MHz, the frequency in this application is set for 1.5MHz by connecting the FREQ pin to V_{IN}.

Figures 5 through 7 show the trade off between mode and V_{OUT} ripple noise. Figure 5 shows the voltage ripple at V_{OUT1} and the current through the inductor while the LTC3417 is in Burst Mode operation. The ripple voltage in this example was taken at an I_{LOAD} of 40mA and is only $15mV_{P-P}$. The worst case output voltage ripple occurs just before the part switches from bursting to continuous mode, which occurs at about 250mA. At his point, the V_{OUT} ripple can be as high as $25mV_{P-P}$.

Figure 6 shows the V_{OUT1} ripple and the current through the inductor when the part is in Pulse Skipping Mode. Notice that the current through the inductor does go slightly negative, and then produces some high frequency components. The higher frequency components are due to the switching MOSFETS turning off. At lower currents, the part starts skipping pulses, and thus produces some lower frequency components. In this case, the voltage ripple does indeed show some higher frequency components, yet the ripple itself is at about $5mV_{P-P}$.

Figure 7 shows the voltage ripple at V_{OUT1} and the inductor current when the part is in Forced Continuous mode. Notice that the current through the inductor goes negative. At no time, during Forced Continuous doe the MOSFETS actually turn off, they keep switching. Therefore, the frequency component of the voltage ripple stays constant at the operating frequency. The voltage ripple therefore looks constant and stays below 5mV over all load currents.

Conclusion

The LTC3417 is a dual synchronous, step-down, current mode, DC/DC converter designed to fit in the tight spaces afforded by today's portable devices. Switching MOSFETS are integrated into the device, and high frequency operation enables the use of small sized components. It is also designed with versatility in mind with external components for loop compensation, variable frequency operation and different operating modes to optimize efficiency and noise.