Redundant 2-Wire Bus for High Reliability Systems

by John Ziegler

Introduction

The effort to achieve high reliability in data processing, data storage and communication systems has necessitated the use of circuitry to monitor parameters such as temperature, fan speed, and system voltages. These circuits often communicate through 2-wire serial buses, such as SMBus or I^2C. Redundant subsystems are important in high reliability systems, and the 2-wire bus subsystem is no exception. High reliability 2-wire bus systems incorporate two master controllers in a redundant configuration, to maintain system operation if one master fails or is removed. In a redundant configuration, each master is connected to its own 2-wire bus, while all of the slaves are connected to a single downstream redundant bus. Either master can take control of the redundant bus at any time.

Figure 1 shows a circuit using two LTC4302's, each dedicated to a master, to allow either master to take control of a redundant 2-wire bus. The LTC4302's GPIO pins default to a high impedance state at power-up, so that 10K pull-up resistors R5, R6 and R13 set each GPIO voltage high. With each LTC4302's GPIO1 pin connected to the CONN pin of the other, both LTC4302's are active at power-up and can be accessed via their SDAIN and SCLIN pins.

In this configuration, each master can take control of the downstream redundant bus with two Write Byte operations to its dedicated LTC4302. In the first operation, the master activates the connection to the downstream redundant bus, and writes both of its GPIO pins low. With the GPIO1 pin low, the other master is disconnected from the redundant bus and is also prevented from communicating with its LTC4302. In the second operation, the master writes a logic high to its GPIO1 pin, so that the other master is again free to communicate with its LTC4302. Using this technique, the common GPIO2 pin is low whenever one of the masters is connected to the

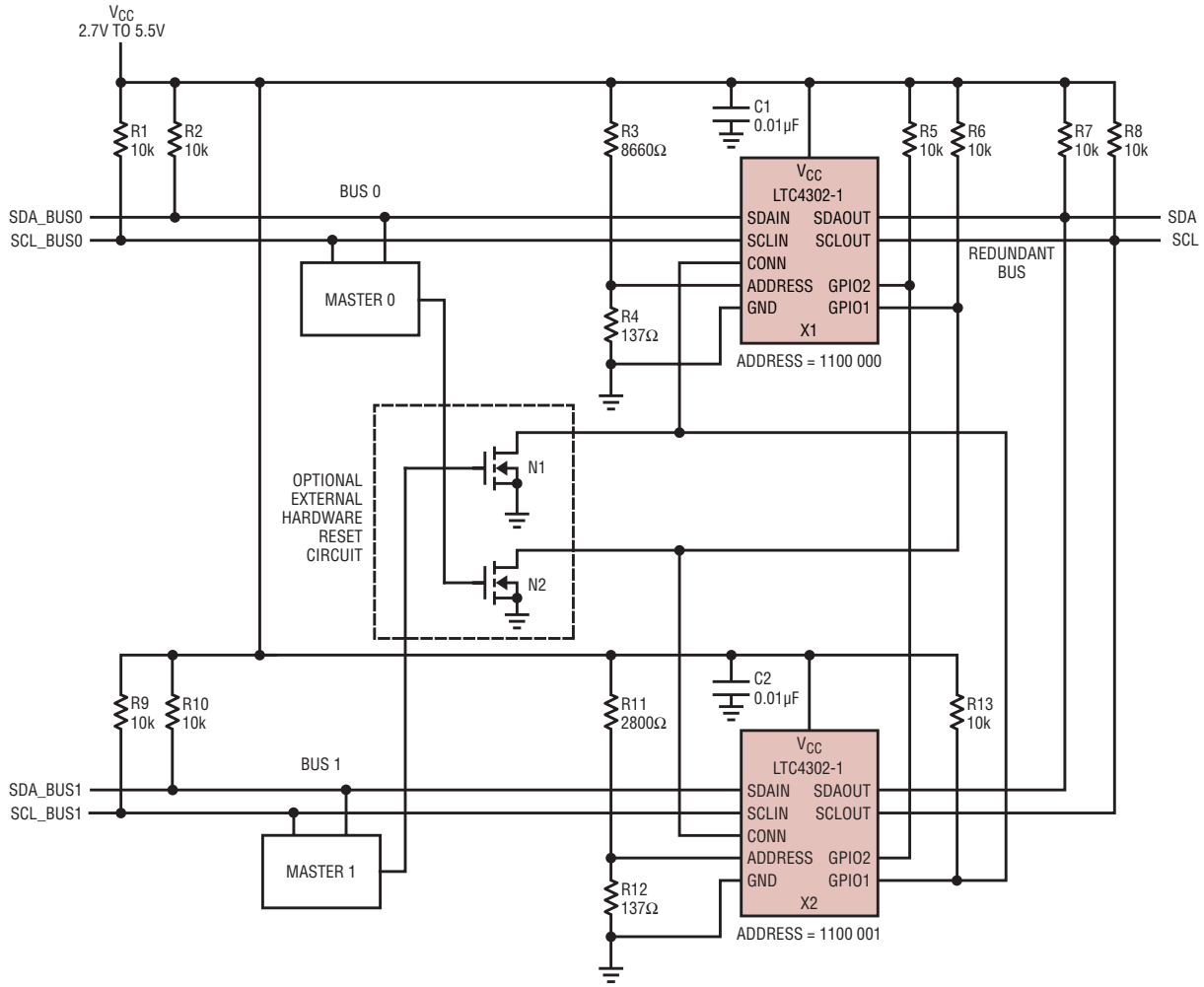

Figure 1. Two LTC4302s in a redundant bus application, with a hardware reset on the CONN pins

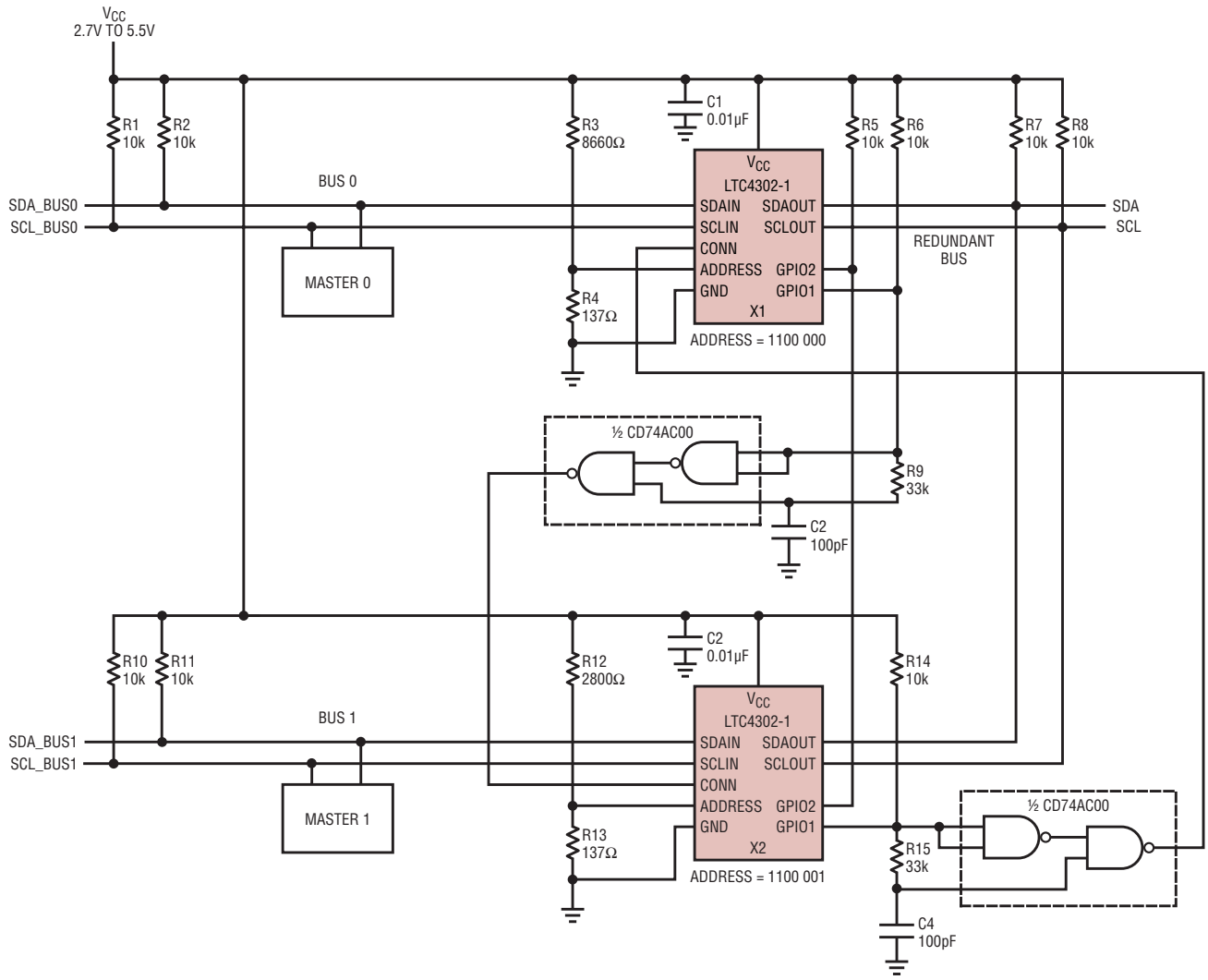

Figure 2. Alternate implementation of two LTC4302s in a redundant bus application, with lock-up prevention circuitry.

redundant bus, so that each master can read its LTC4302 to determine whether the other master has control of the redundant bus.

Either master can take control of the redundant bus at any time except under two conditions. First, if a master tries to access its LTC4302 and receives no Acknowledge signal, it knows that the other master has completed the first Write Byte operation, but has not yet re-written its GPIO1 pin back high. Second, if both masters try to connect to the redundant bus within 100ns of each other, both are connected to the bus temporarily, and are then disconnected.

A disadvantage of this scheme is that two separate write operations are required for a master to take control of the downstream bus properly. After the first operation, the new master has control of the redundant bus, and the other master cannot access its own LTC4302 because its CONN pin is low. If the new master is removed from the system, or if its 2-wire bus locks up before it can complete the second write operation to write a logic high to its GPIO1 pin, then the other master is permanently prevented from taking control of the redundant bus through the 2-wire interface. An externally controlled pull-down device would have to be used to pull the CONN pin of the new master low, as shown by N-Channel MOSFET transistors N1 and N2 in Figure 1.

Figure 2 shows an alternative approach to solve this problem. Each master can take control of the redundant bus using a single Write Byte operation. For example, Master 0 commands its LTC4302 to connect to the redundant bus and also to force logic lows on both of its GPIO pins. When its GPIO1 pin transitions high-to-low, the circuit formed by R9, C2 and the two two-input NAND gates generates a negative pulse on the other LTC4302's CONN pin. The duration of the pulse is set by the R9 • C2 time constant and is roughly 3.3µs. Pulsing CONN low resets the registers of the LTC4302 to their default states, thereby disconnecting Master 1 from the redundant bus. After 1µs, Master 1's CONN pin returns high, and Master 1 is again free to take control of the redundant bus.

The LTC4302 also provides bidirectional buffering, keeping the capacitances of the master buses and the redundant bus isolated from each other. Rise time accelerator circuitry

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at around 42V to protect the internal power devices.

Layout Considerations

Proper layout is important to achieve the best performance. Paths that carry high switching current should be kept short and wide to minimize the parasitic inductance. In the boost regulator, the switching loop includes the internal power switch, the Schottky diode (internal or external), and the output capacitor. In the negative output regulator, the switching loop includes the internal power switch, the flying capacitor between the SW2 and D2 pins, and the internal Schottky diode.

Connect the output capacitors of the AV_{DD} and LED switchers directly to the PGND14 pin before returning to the ground plane. Connect the output capacitor of the V_{ON} switcher to the PGND23 pin before returning to the ground plane. Also connect the bottom feedback resistors to the AGND pin. Connect the PGND14, PGND23 and AGND pins to the top layer ground pad underneath the exposed copper ground on the backside of the IC. The exposed copper helps to reduce thermal resistance. Multiple vias into ground layers can be placed on the ground pad directly underneath the part to conduct the heat away from the part.

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least 750mA from a V_{IN} as low as 3V. When fully charged to 4.2V, over 1A can be supplied. The photograph of a demonstration board in Figure 5 shows just how small the board area is for this application, 10mm × 12mm. Tiny ceramic bypass capacitors and surface mount inductors keep the design small.

Figure 6 shows efficiency exceeding 90% and remaining greater than 85% over a load range from 10mA to 900mA with a fully charged battery.

Component Selection

The LTC3426 requires just a few external components to accomodate various V_{IN} and V_{OUT} combinations. Selecting the proper inductor is important to optimize converter performance and efficiency. An inductor with low DCR increases efficiency and reduces self-heating. Since the inductor conducts the DC output current plus half the peak-to-peak switching current, select an inductor with a minimum DC rating of 2A. To minimize V_{OUT} ripple, use low ESR X5R ceramic capacitors. The average Schottky diode forward current is equal to the DC output current therefore the diode average current should be greater than 1A. A low forward voltage Schottky diode reduces power loss in the converter circuit.

Conclusion

The addition of the LTC3426 to Linear Technology's high performance boost converter family allows the designer to deliver high current levels with minimal board space. An on chip switch and internal loop compensation reduces component count to provide an inexpensive solution for spot regulation applications.

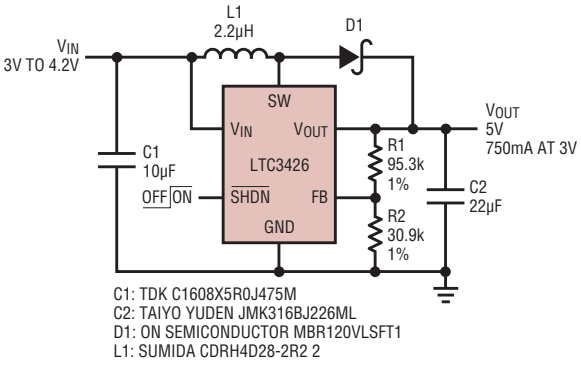

Figure 4. Compact application circuit for V_{OUT} at 5V

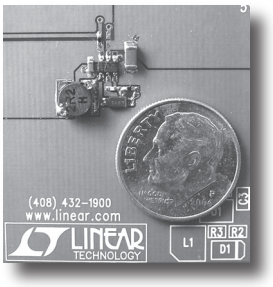

Figure 5. Photograph of demo board of circuit in Figure 4—board area is 10mm × 12mm

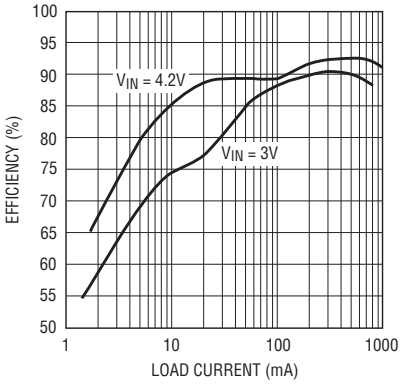

Figure 6. Up to 92% efficiency in Lithium-Ion battery to 5V output applications

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further eases the burden of heavy capacitive loads by providing strong pull-up currents during rising edges to reduce the rise time. Thanks to these two features, the LTC4302 enables the implementation of much larger 2-wire bus systems than are possible with a simple unbuffered multiplexer.

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assume that either the inductance is well damped, or it is shunted by large value capacitances.

Notes

1. This subject is treated in some detail in the LTC1647 data sheet, Figures 9, 10, and 11 inclusive.
2. An hp 5210A Frequency Meter or any common counter gives adequate accuracy for most measurements.