Characteristics of Polysilicon Resistors for Sub-Quarter Micron CMOS Applications

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Abstract

The characteristics of polysilicon resistors for sub-quarter micron CMOS applications have been investigated. Based on the presented sub-quarter micron CMOS borderless contact, both n^+ and p^+ polysilicon resistors with Ti- and Co-silicide self-aligned process are used at the ends of each resistor. A simple and useful model is proposed to analyse and calculate some important parameters of polysilicon resistors including interface resistance $R_{interfac}$ and bulk sheet resistance R_{bule}. The characteristics of voltage-coefficient resistor (VCR) are also studied. An interesting sine-wave voltage-dependent characteristic due to the strong relation to the $R_{interface}$ has been modelized in this work. This approach can substantially help engineers in designing and fabricating the precise polysilicon resistors in sub-quarter micron CMOS ULSI technology.

1. Introduction

Recently, in the ULSI's technologies, the "system-on-a-chip" (SOC) concept has become attractive for system designers. It is needed to integrate passive components (resistors, capacitors, and inductors) into the SOC. For analog IC design, the resistor is very crucial for circuit performance due to the small voltage-independent parasitic resistance. The stability of a polysilicon resistor is also very important because it directly affects the reference voltage accuracy and power consumption of an electrical circuit. Practically, the polysilicon resistor is a material which is widely used throughout the semiconductor industry. Generally, the doped polysilicon is used as a precise analog resistor element [1-3]. A mixed signal, that combines digital and analog circuit design in multiple logic CMOS process with polysilicon resistors, is commonly used in analog to digital (ADC) circuit application [4].

In this work, we report and demonstrate the highly precise n^+ and p^+ polysilicon resistors in sub-quarter micron multiple logic CMOS ULSI process. These polysilicon resistors are made by n^+ and p^+ source/drain (S/D) ion-implantation. The characteristics of n^+ and p^+ polysilicon resistors including the extraction of interface resistance ($R_{interface}$) and sheet resistance (R_{bulk}) are studied. Furthermore, the calculation and extraction of $R_{interface}$ and R_{bulk} on voltage-coefficient resistor (VCR) are also included.

2. Experimental

The studied n^+ and p^+ polysilicon resistors were fabricated by using CMOS process with a shallow trench isolation (STI). A 2000 Å-thick amorphous silicon film was deposited at 540^{O}C. After forming a polysilicon-gate, including polysilicon resistor and Si_3N_4 spacer, the shallow S/D junctions were achieved with n^+ S/D and p^+ S/D implantation for NMOS and PMOS devices, respectively. At the same time, the implantation was employed for the polysilicon resistor. The n^+ S/D and p^+ S/D were formed by the implant conditions of As/50keV/5.5x10^{15}cm^{-2} (As/40keV/5.0x10^{15}cm^{-2}) and BF_2/25keV/5.0x10^{15}cm^{-2} (B/5keV/3.5x10^{15}cm^{-2}) for Ti-(Co-) salicide process, respectively. A rapid thermal annealing (RTA) process was used to activate the dopants at 1025 ^{O}C for 30 seconds. A resist-protect-oxide (RPO) was performed to prevent the polysilicon resistor from silicidation. Both Ti- and Co-salicidation formed on the polysilicon-gate and S/D diffusion layers were then introduced respectively in our study. Due to the employed borderless contact process, Ti- and Co-salicide were formed at ends of each resistor for metal contact resistance. After the forming interconnects, a forming N_2 gas annealing at 400 ^{O}C was employed. Figure 1 depicts the schematic diagram of a studied polysilicon resistor.

3.1 The Extraction of R_{pure} and $R_{interface}$:

The width W and length L of studied polysilicon resistors are 0.60, 1.34, 2.08, 2.82, 3.56, 4.30, 7.26, 10.96 μm and 1W, 2W, 5W, 10W, respectively. The total dc equivalent total resistance (R) can be expressed as:

$$R = R_C + R_{Silicide} + R_{bulk} \cdot \frac{L}{W} + R_{\text{int}erface} \qquad (1)$$

$R_{interface}$ represents the interface resistance between the polysilicon resistor and silicide and R_{bulk} denotes the sheet resistance of the polysilicon resistor. R_C and $R_{Silicide}$ are the effective contact and silicide resistance, respectively. The typical values of R_C and $R_{Silicide}$ of $TiSi_2$ ($CoSi_2$) are 6.11 (5.61) Ω/contact and 3.48 (6.08) Ω/□, respectively.

In order to extract $R_{interface}$ and R_{bulk}, the measurement of total resistance of the polysilicon resistors with various square number □ are employed. When the polysilicon resistor width W is fixed, the R_{bulk} and $R_{interface}$ can be seen as constant values. With the variation of polysilicon resistor length L (or square number □), the R_{bulk} can be extracted as:

$$R_{pure} = (R_1 - R_2) \Big/ \left(\frac{L_1 - L_2}{W} \right) \qquad (2)$$

Thus the value of $R_{interface}$ can be extracted from Eq. (1). The relationship between R_{bulk} and W is illustrated in Fig. 2. Obviously, the R_{bulk} is independent of W when W ≥ 2.0 μm. However, the R_{bulk} exhibits a rapid increase once the sub-micron W is used. The presented size effect and increase of resistance within the sub-micron regime may be related to the surface scattering and grain-boundary scattering [5]. Similarly, at the fixed value of W, the R_{bulk} is increased with the decrease of L (or square number) especially in the sub-micron regime. The $R_{interface}$ versus inverse polysilicon resistor width W^{-1} is revealed in Fig. 3. An approximately linear relationship between $R_{interface}$ and W^{-1} is found. Obviously, the $R_{interface}$ of n^+ polysilicon resistor is much smaller than that of the p^+ polysilicon resistor. This result can be explained as followed. Under the same thermal cycle, the surface boron concentration under silicide is much less than the surface arsenic concentration [5-6] because boron ions are easier diffused into silicide than arsenic ions. Furthermore, since the standard deviation 3σ of $R_{interface}$ is large, a relatively larger polysilicon resistor width (W ≥ 2 μm) with larger square number (≥ 5 □) is recommended in the resistor design to minimize the $R_{interface}$ effect.

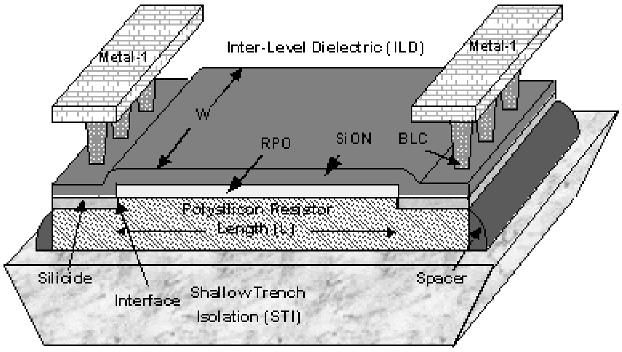


Figure 1. The schematic diagram of a polysilicon resistor

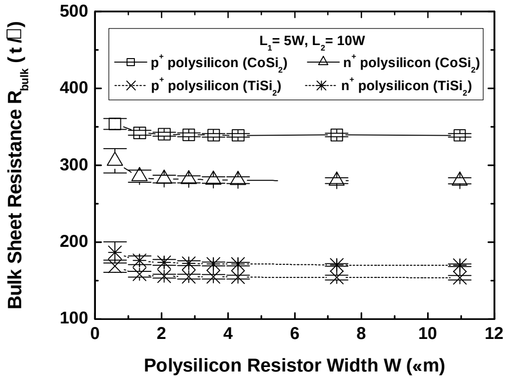


Figure 2. The relationship between the bulk sheet resistance (R_{bulk}) and the polysilicon resistor width W with the polysilicon resistor lengths of L_1= 5W and L_2= 10W

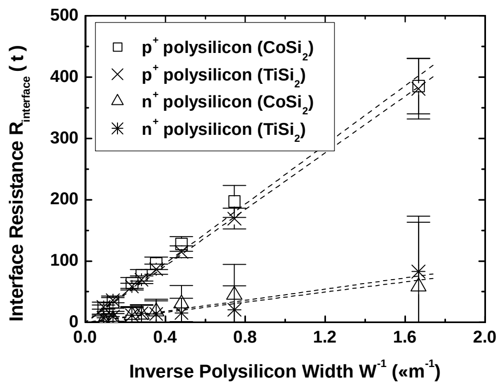


Figure 3. The relationship between the interface resistance $R_{interface}$ and the inverse polysilicon resistor width W^{-1}

3.2 Voltage Coefficient of Resistance (VCR):

The voltage coefficient of resistance (VCR) is a function of dopant, doping concentration, polysilicon resistor length and width. The total resistance R and VCR can be characterized as a function of the applied voltage :

$$R(V) = a_2 \cdot V^2 + a_1 \cdot V + a_0 = a_0\left(\frac{a_2}{a_0}V^2 + \frac{a_1}{a_0}V + 1\right) \quad (3)$$

and

$$VCR(V) = \frac{\partial R(V)}{\partial V} = a_0(2 \times VCR_2 \times V + VCR_1) \quad (4)$$

where V is the applied voltage, a_0, a_1, and a_2 are constant values, $VCR_1 = a_1/a_0$, and $VCR_2 = a_2/a_0$ [5].

An anomalous sine-wave like voltage-dependent characteristics is observed as the W shrinks to 0.60 μm. These interesting nonlinear voltage-dependent characteristics may be related to the behavior of $R_{interface}$.

For detailed study, the voltage-dependent phenomena of R_{bulk} and $R_{interface}$, extracted from Eq.(1), of Ti- and Co-silicide of n^+ and p^+ polysilicon resistor are shown in Figs. 4(a) and (b), respectively. The same W of 2.08μm and square number of 5□ and 10□ are employed. The variation of voltage-dependent characteristics of the total resistance can be seen as the combination of those of R_{bulk} and $R_{interface}$. Obviously, R_{bulk} is nearly independent of the DC voltage biased. However, $R_{interface}$ has strong dependence on the DC voltage biased especially when the W is decreased.

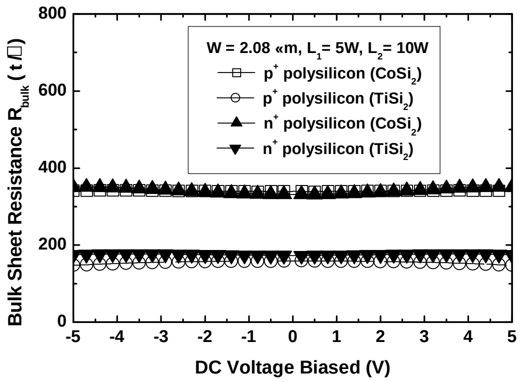
Thus, the nonlinear performance (sine-wave shape) of polysilicon resistors is related to the non-linear properties of $R_{interface}$. Hence, the voltage dependence on R_{bulk} can be neglected. Since $R_C + R_{Silicide} << R_{bulk}$ and $R_{interface}$, the total resistance R can be re-written as a function of the applied voltage:

$$R(V) \approx R_{interface} \times (1 + VCR_{int1} \times V + VCR_{int2} \times V^2) + R_{bulk} \times \frac{L}{W} \quad (5)$$

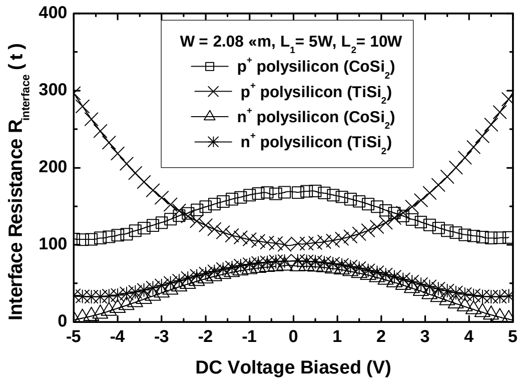
In addition, VCR phenomena can be characterized as the first order derivative of the applied voltage, i.e., the linear function of V, or the VCR can be defined as :

$$VCR \approx R_{interface} \times (VCR_{int1} + 2 \cdot VCR_{int2} \times V) \quad (6)$$

From Eq. (6), it is known that the magnitude and behavior of VCR characteristics are strongly influenced by $R_{interface}$, VCR_{int1} and VCR_{int2}. The VCR characteristics with W=2.08 μm and square numbers of 5□ of Ti- and Co-silicide of n^+ and p^+ polysilicon resistors are illustrated in Fig 5. The Ti-silicide p^+ polysilicon resistor has positive voltage-dependant VCR behaviors while other resistors exhibit the negative ones. Experimentally, under the same square number, the larger width of polysilicon resistor is employed, the better performances of VCR are obtained. Therefore, in order to obtain high performance and low magnitude of VCR, larger polysilicon width and length are needed.



(a)



(b)

Figure 4. The voltage-dependent characteristics of (a) R_{bulk} and (b) $R_{interface}$ with polysilicon resistor width W of 2.08 μm of n^+ and p^+ polysilicons with Ti- and Co-silicide

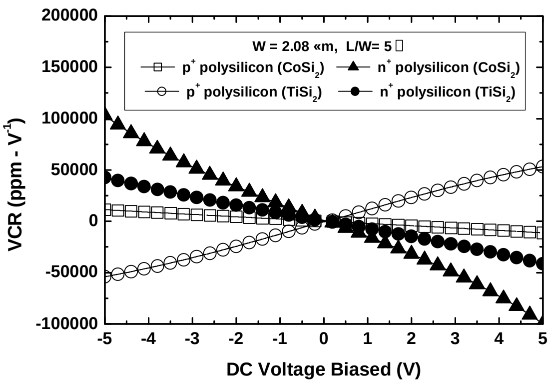


Figure 5. The VCR characteristics of Ti- and Co-silicide of n^+ and p^+ polysilicons with polysilicon resistor width W of 2.08 μm and square number of 5□

4. Conclusion

The characteristics of polysilicon resistor in sub-quarter micron CMOS ULSI applications have been studied and demonstrated. A simple model is proposed to analyze and calculate the important parameters of polysilicon resistors including R_{bulk} and $R_{interface}$. The size effect plays a key role on the resistor performances within the sub-micron regime. In addition, the interface resistance $R_{interface}$ has strong influence on the overall resistor characteristics. Therefore, in order to obtain a high-precise resistor, the accurate calculation of $R_{interface}$ is needed. Furthermore, the characteristics of VCR are also included in this study. Due to the $R_{interface}$ effect, an interesting sine-wave like voltage-dependent characteristic of polysilicon resistor is observed. Experimentally, better performances of VCR can be expected for the presented larger values of polysilicon resistor width and length. Based on the proposed model, it is helpful for the engineers in designing and fabricating the precise polysilicon resistors in sub-quarter micron CMOS ULSI technology.

References

[1] K. Kato, T. Ono, and Y. Amemiya, "Electrical trimming of poly-crystalline silicon resistors and its application to analog IC's," IEEE Trans. Electron Devices, vol. ED-27, no. 11, pp. 2194-2205, 1980.

[2] N. C. C. Lu, L. Gerzberg, C. Y. Lu, and J. D. Meindl, "A new conduction model for polycrystalline silicon films," IEEE Electron Device Lett., vol. 2, pp. 95-98, 1981.

[3] W. A. Lane and G. T. Wrixon, "The design of thin-film polysilicon resistors for analog IC applications," IEEE Trans. Electron Devices, vol. ED-36, no. 4, pp. 738-744, 1989.

[4] S. Nygren, D. T. Amm, D. Levy, J. Torres, G. Goltz, T. D'ouville, and P. Delpech, " Dual-type CMOS gate electrodes by dopant diffusion from silicide," IEEE Trans. Electron Devices, vol. ED-36, no. 6, pp. 1087-1093, 1989.

[5] S. M. Sze, Physics of Semiconductor Devices, New York: Wiley, 1983

[6] C. L. Chu, K. C. Saraswat, and S. S. Wong, " Measurement of lateral dopant diffusion in thin film silicide layers," IEEE Trans. Electron Devices, vol. ED-39, no. 10, pp. 2333-2340, 1992.