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Hybrid Beamforming Receiver Dynamic Range Theory to Practice

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Abstract

This article covers the following comparison of measurements vs. analysis for receiver dynamic range metrics in a phased array hybrid beamforming architecture. A commercially available 32-channel development platform is used to validate the analysis with measurements. The receiver analysis for subarray beamforming is reviewed, with an emphasis on handling the differences between signal gain and noise gain at the point where signals are combined in the analog subarray. An analysis is shown for the development platform receiver performance and compared against measured results. A summary of the results is discussed with the intention to provide a measured vs. modeled reference point that can be leveraged to predict the performance of larger systems.

Introduction

Phased array beamforming architectures can be roughly categorized as analog beamforming systems, digital beamforming systems, or some combination of both utilizing analog subarrays that are processed digitally to form the final antenna beam pattern. The latter category based on subarrays combined digitally is often called hybrid beamforming, as it uses a combination of both analog and digital beamforming.

In the industry quest toward software-defined antennas, there is a great desire for all-digital phased arrays to maximize antenna pattern programmability. In practice, particularly as frequency increases, the packaging, power consumption, and digital processing challenges force a reduction in the digital channel count. Hybrid beamforming provides the digital channel density relief often needed by implementation engineers and therefore will likely be around as a practical option for some time into the future.[1]

Figure 1 illustrates a representative hybrid beamforming architecture showing the major subsystems incorporated into the architecture. Most hybrid beamforming systems are some sort of variation of this concept. The architecture can be intuitively described by following the diagram from right to left: from the wavefront in the air incident onto the antenna elements, through the microwave circuitry to the data converters, then through the digital processing and into the final digital beam data. The diagram illustrates the hybrid beamforming architecture as a combination of seven subsystems:

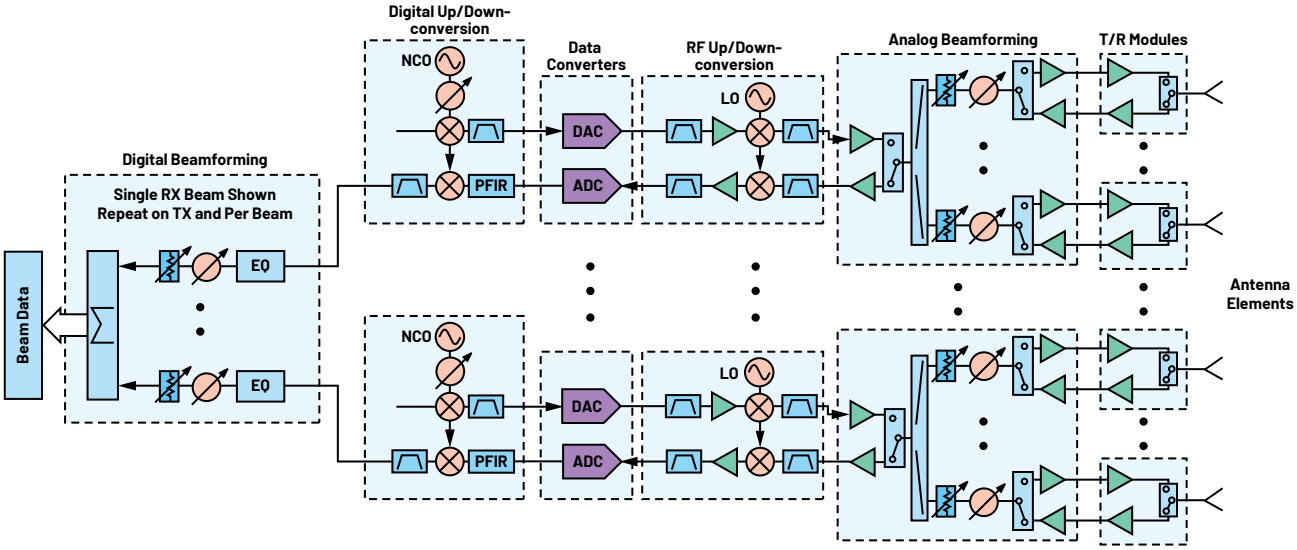

Figure 1. Generic hybrid beamforming RF block diagram.

- 1. Antenna elements: These convert the microwave energy in the air to a microwave signal on a coaxial medium.
- 2. Transmit/receive (T/R) modules: These contain the receive low noise amplifier (LNA) and the transmit high power amplifier (HPA) along with a switch to select between transmit and receive.
- 3. Analog beamforming: This combines a selected number of elements into an analog subarray.
- 4. Microwave up/downconversion: If the operating frequency is greater than the data converter operating range, frequency conversion is used to translate from the operating frequency to an intermediate frequency (IF) that is appropriate for the data converters.
- 5. Data converters: These convert a microwave frequency to a digital word.
- 6. Digital up/downconversion: With the proliferation of high speed data converters, typically the data converter rates are larger than necessary for the processing bandwidth. System power can be saved by using digital up/downconversion features embedded in the data converter integrated circuits (ICs) to reduce the in-phase/quadrature-phase (I/Q) data stream to a lower rate commensurate with the processing bandwidth of the application.
- 7. Digital beamforming: Finally, the I/Q data streams are combined in a weighted sum to form the final digital beam data.

One of the challenges microwave engineers face in hybrid beamforming architectures is a performance prediction as the system architecture evolves. Cascaded microwave analysis is well documented and understood. Digital beamforming measurements have been documented,[2,3,4] but there is limited measured vs. modeled hybrid beamforming microwave metrics documented to use as a reference when extrapolating to larger system designs.

This article documents a receiver dynamic range analysis for a hybrid beamforming system and compares measurements vs. predictions on a 32-element hybrid beamforming test platform. The hybrid beamforming prototype platform was initially developed to validate IC designs in a representative architecture and to enable rapid prototyping of X-band (8 GHz to 12 GHz) phased array architectures. However, as characterization began, it was clear a method to systematically predict performance metrics was needed. Our intention is to document the analysis method along with a comparison of measured data enabling engineers building similar but larger systems with a characterized reference.

Prototype Hardware

A 32-element hybrid beamforming prototype platform has been developed[5] and is shown in Figure 2. The detailed signal chain is shown in Figure 3.

The front end consists of 32 transmit/receive modules and eight analog beamforming ICs (BFICs). Two BFIC outputs combine to produce four 8-element subarrays. The four subarrays connect to a 4-channel microwave up/downconverter. The 4-channel microwave up/downconverter then connects to a digitizer IC that contains four analog-to-digital converters (ADCs) and four digital-to-analog converters (DACs). The ADCs sample at 4 GSPS whereas the DACs sample at 12 GSPS.

The microwave frequencies characterized are from 8 GHz to 12 GHz. The local oscillator (LO) is set to a high-side LO with a fixed IF centered at 4.5 GHz. At this IF frequency, the ADC is sampling in the third Nyquist zone.

A commercial FPGA board is used for data capture. A MATLAB® computer control interface has been developed enabling rapid characterization of simulated waveforms in real hardware. Data analysis was performed with postprocessing in MATLAB.

Analog Subarray Cascaded Analysis

All traditional cascaded equations apply to the cascaded analysis of an analog subarray except the point of the signal combination. If the signals are matched in amplitude and phase at the point of the combiner, and the noise is uncorrelated, the signal gain and noise gain will be different. Therefore, an approach is needed to track these terms differently.

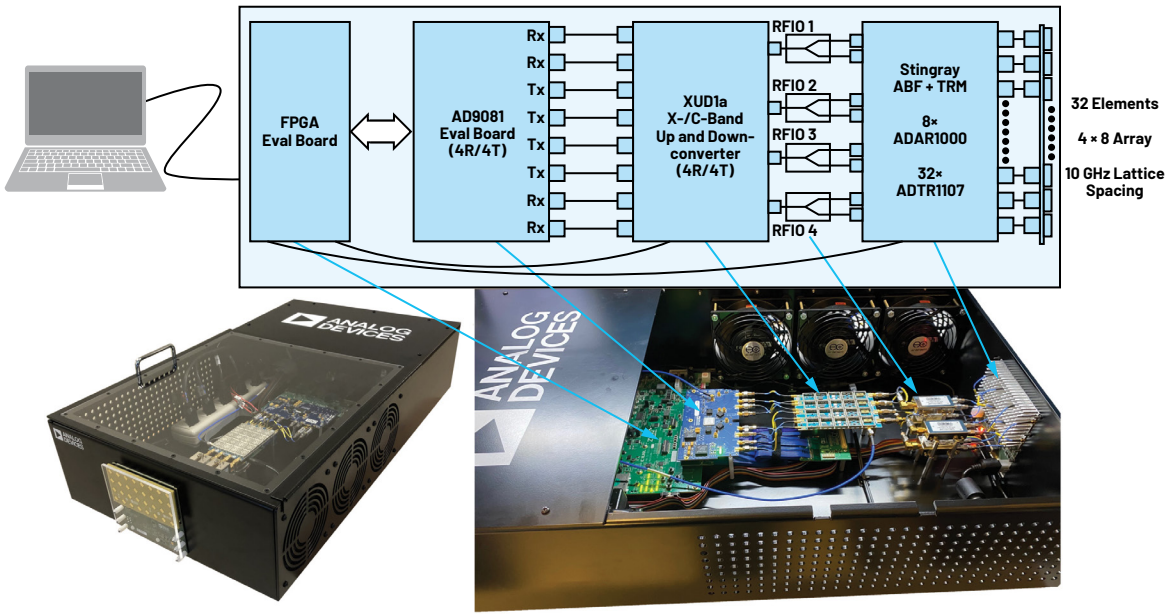

Figure 2. X-band (8 GHz to 12 GHz) phased array prototyping and development system.

Approach Used

Figure 4 illustrates the approach used. Figure 4a illustrates the point at which signal gain and noise gain diverge. A real combiner has an insertion loss term and a theoretical combining term. This can be accounted for as shown in Figure 4b. Finally, if noise temperature is tracked as shown in Figure 4c, then noise power can be tracked at the input and output of each stage.

To calculate a noise power at the output of any stage, component input-referred noise is added to the input noise linearly and then converted back to dBm/Hz and added to the component noise gain.

$$\begin{aligned} &Component\ Noise\ Out\left(\frac{\text{dBm}}{\text{Hz}}\right) = Component\ Noise\ Gain\ (\text{dB}) \\ &+ 10log10\left(10\,\frac{Noise\ In\left(\frac{\text{dBm}}{\text{Hz}}\right)}{10}\right. \\ &\left. + 10\,\frac{Input\ Referred\ Component\ Noise\left(\frac{\text{dBm}}{\text{Hz}}\right)}{10}\right) \end{aligned} \quad (1)$$

To calculate input-referred noise from a device noise figure, calculate noise temperature and convert to input referred noise power.

Noise temperature (T_e) can be calculated from a device noise figure as

$$T_e = T\left(10\,\frac{NF(\text{dB})}{10} - 1\right) \quad (2)$$

where T is the ambient temperature in degrees Kelvin.

From noise temperature, input-referred component noise can be calculated:

$$\begin{aligned} &Input\ Referred\ Component\ Noise = kT_e\,(\text{J}) \\ &Input\ Referred\ Noise\ Power\ in\ \frac{\text{dBm}}{\text{Hz}} = 10log10(kT_e) + 30 \end{aligned} \quad (3)$$

Where k is Boltzmann's constant.

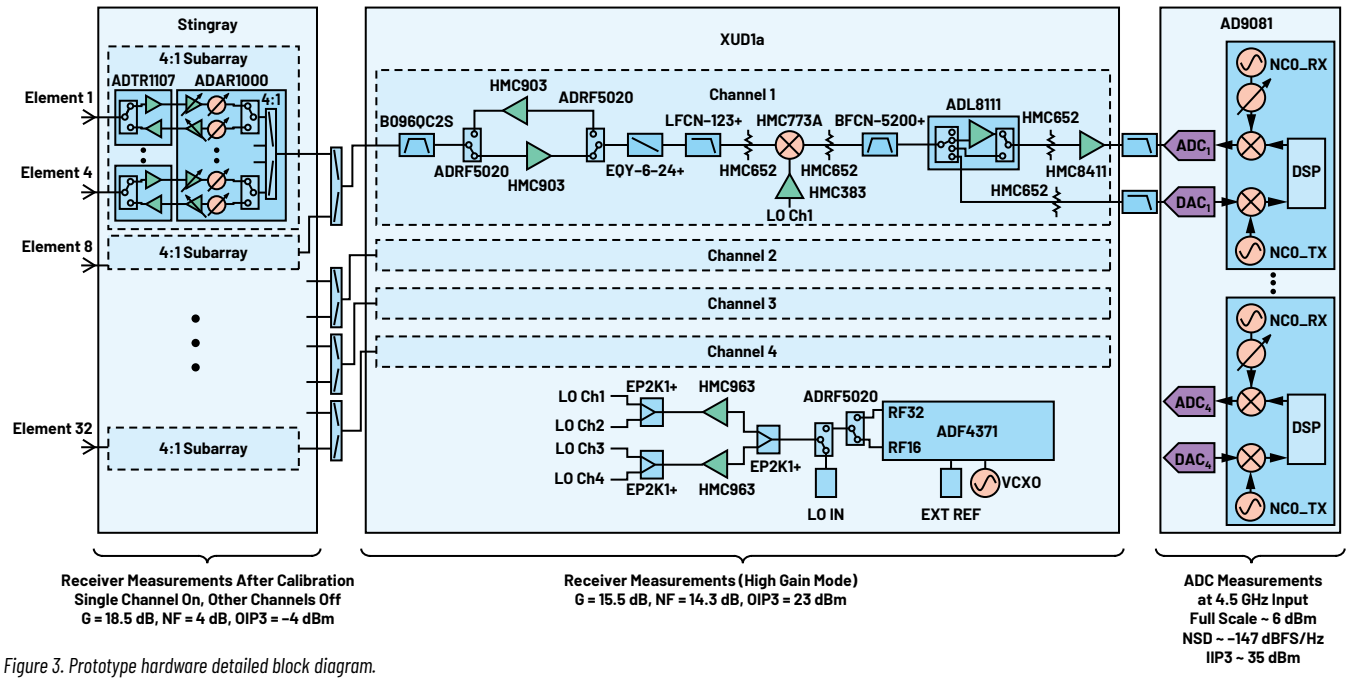

Figure 3. Prototype hardware detailed block diagram.

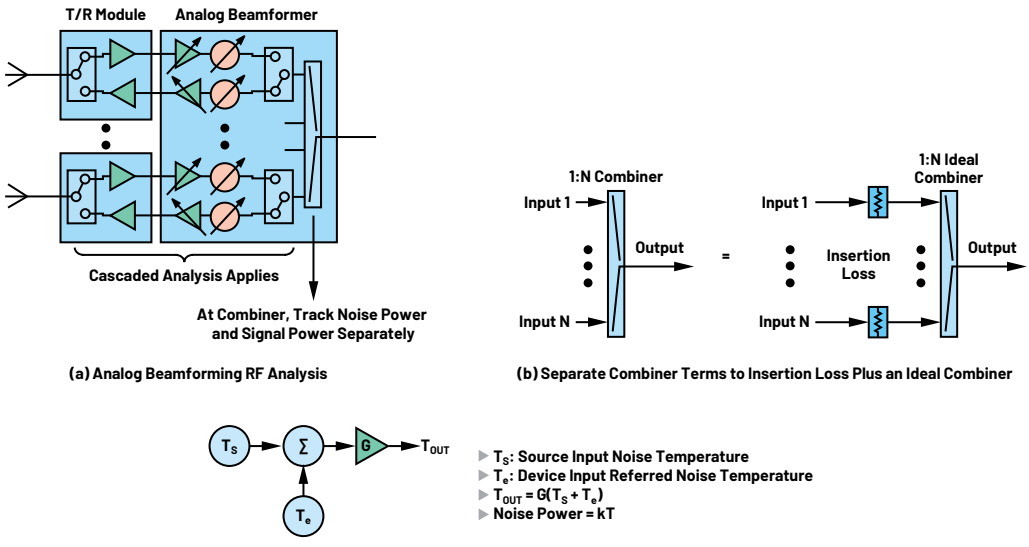

Figure 4. A cascaded analysis approach for analog coherent combining: signal gain and noise gain are tracked separately. Tracking device noise temperature and input-referred device noise power provide a method to track these gain terms separately.

Intuitive Description for Coherent Combing

An intuitive view of signal vs. noise combining can help visualize the purpose of the approach. We start with the assumption that a calibration has been performed, resulting in all signals being matched in both amplitude and phase, and the noise is uncorrelated yet also equal in amplitude across all channels at the combiner input.

We also need a method to track the result if only a subset of the elements is enabled, which is routinely the case in calibrations or varied test and debug configurations.

The signal and noise output levels can be calculated as:

Signal Power = Input Power + Signal Gain
Signal Gain = 20log (Number of Channels On) – Insertion Loss – 10log(Number of Combiner Input Ports)

Noise Power = Input Noise Power + Noise Gain
Noise Gain = 10log(Number of Channels On) – Insertion Loss – 10log(Number of Combiner Input Ports)

Note the result of this approach. Table 1 summarizes the signal gain and noise gain for several analog combiner channel counts with the case of every input being energized and calibrated, or with only a single input and the other ports terminated.

Table 1. Signal/Noise Gain for a Lossless Combiner

Number of Channels Combined	Signal Gain (All On)	Noise Gain (All On)	Signal Gain (One On)	Noise Gain (One On)
2	3	0	-3	-3
4	6	0	-6	-6
8	9	0	-9	-9

Cascaded Spreadsheets

Using the approach described, the cascaded spreadsheet of Figure 5 has been created. Provisions for tracking the number of elements enabled are included. Both the case of a single element enabled as well as the case of all eight elements enabled are shown.

Measurements are derived from the fast Fourier transforms (FFTs) of digital data after data capture by the data converters, so data converter specifications are included in the result. The final metrics tracked are ADC metrics referred to as the receiver input. For quick validation of the measurements, the expected FFT magnitude and intermodulation products are also calculated for a given input power.

Measured Data

Test Equipment

The test setup is shown in Figure 2 and Figure 3. The specific lab equipment used to provide the receiver input, LO, ADC sample clock, and overall system reference clock is shown in Table 2. The digitizer ICs within the system are leveraged to capture the samples shown in the following results.

Table 2. The Test Equipment That Is Used as Part of the Data Capture in the Following Sections

Equipment Function	Make/Model	Comments
Receiver Input Source	Keysight E8267D to 32-channel analog splitter	Input to transmit/receive modules calibrated for a power level of ~50 dBm
LO Source	Keysight E8267D	Input to up/downconverter board is 5 dBm
ADC Clock	Rohde & Schwarz SMA100B	12 GHz input frequency to the AD9081, internally divided by 3 provides a 4 GSPS ADC clock
Reference Clock	Keysight N5182B	100 MHz frequency

Single Channel

	Component Specs			Component Calcs			Cumulative Parameters				
	Signal Gain	Noise Figure	OIP3	Noise Gain	Te	kTe	Signal Gain	Noise Gain	Cum Noise Out	Cum NF	Cum IIP3
	(dB)	dB	dBm	dBm	k	dBm/Hz	dB	dB	dBm/Hz	dB	dBm
Components									-174.0		
Front End Loss	-0.2	0.2	50.0	-0.2	13.7	-187.2	-0.2	-0.2	-174.0	-0.2	50.2
Stingray + Comb	18.5	4.0	-4.0	18.5	438.4	-172.2	18.3	18.3	-151.5	4.2	-22.3
Ideal Combiner	0.0	0.0	50.0	0.0	0.1	-210.4	18.3	18.3	-151.5	4.2	-22.3
Cable	-1.0	1.0	50.0	-1.0	75.1	-179.8	17.3	17.3	-152.5	4.2	-22.3
XUD	15.5	14.3	23.0	15.5	7515.5	-159.8	32.8	32.8	-136.2	4.9	-22.5
Cable+Filter	-1.5	1.5	50.0	-1.5	119.6	-177.8	31.3	31.3	-137.7	4.9	-22.5

RF Section Total	Signal Gain	Noise Gain	Cum Noise Out	Cum NF	Cum IIP3
	(dB)	(dB)	(dBm/Hz)	(dB)	(dBm)
	31.3	31.3	-137.7	4.9	-22.5

A/D Specs	Full Scale	NSD	IIP3
	(dBm)	(dBFs/Hz)	(dBm)
	6	-147	35

Receiver Total	RX Full Scale Input	NSD	Cum IIP3
	(dBm)	(dBFs/Hz)	(dBm)
	-25.3	**-142.1**	**-22.5**

Validation		
	Input Power (dBm)	-50
	FFT Mag (dBFs)	-24.7
	IMD (dBc)	54.9

8 Channel Subarray

	Component Specs			Component Calcs			Cumulative Parameters				
	Signal Gain	Noise Figure	OIP3	Noise Gain	Te	kTe	Signal Gain	Noise Gain	Cum Noise Out	Cum NF	Cum IIP3
	(dB)	dB	dBm	dBm	k	dBm/Hz	dB	dB	dBm/Hz	dB	dBm
Components									-174.0		
Front End Loss	-0.2	0.2	50.0	-0.2	13.7	-187.2	-0.2	-0.2	-174.0	-0.2	50.2
Stingray + Comb	18.5	4.0	-4.0	18.5	438.4	-172.2	18.3	18.3	-151.5	4.2	-22.3
Ideal Combiner	18.1	0.0	50.0	9.0	0.1	-210.4	36.4	27.3	-142.4	4.2	-22.3
Cable	-1.0	1.0	50.0	-1.0	75.1	-179.8	35.4	26.3	-143.4	4.2	-22.3
XUD	15.5	14.3	23.0	15.5	7515.5	-159.8	50.9	41.8	-127.8	4.3	-28.9
Cable+Filter	-1.5	1.5	50.0	-1.5	119.6	-177.8	49.4	40.3	-129.3	4.3	-28.9

RF Section Total	Signal Gain	Noise Gain	Cum Noise Out	Cum NF	Cum IIP3
	(dB)	(dB)	(dBm/Hz)	(dB)	(dBm)
	49.4	40.3	-129.3	4.3	-28.9

A/D Specs	Full Scale	NSD	IIP3
	(dBm)	(dBFs/Hz)	(dBm)
	6	-147	35

Receiver Total	RX Full Scale Input	NSD	Cum IIP3
	(dBm)	(dBFs/Hz)	(dBm)
	-43.4	**-135.1**	**-29.1**

Validation		
	Input Power (dBm)	-50
	FFT Mag (dBFs)	-6.6
	IMD (dBc)	41.8

Figure 5. Cascaded calculations.

Calibration

For all measurements there is a calibration prior to data analysis. The system is comprised of 32 antenna elements, eight BFICs, and one digitizer IC that includes four ADCs. Each of the four digitizer IC ADC signal chains include hardened digital signal processing (DSP) blocks in the form of digital downconverters, inside which are numerically controlled oscillators (NCOs) capable of applying phase shifts on each of the four digitized channels at the subarray level. As such, eight antenna elements form a single subarray as defined for this paper and share a common ADC and DSP signal chain. The phase and amplitude adjustments available in the system are implemented in the analog domain via the BFICs as well as in the digital domain via the NCOs and programmable finite impulse response (PFIR) blocks.

Initially, Channel 1 is chosen as the baseline upon which all other channels are aligned. Within the analog domain, the BFIC variable gain amplifier (VGA) is used to align amplitudes across the entire array and the BFIC phase shifter (PS) is used to align phases within a subarray. Within the digital domain, the NCO phase offsets are used to align the phases across each subarray.

The calibration begins by enabling one analog channel per subarray at a time (for example, Channel 1, Channel 3, Channel 17, and Channel 19, as shown on the right of Figure 6) such that a total of four signals are simultaneously digitized by the four ADCs on the digitizer IC. This allows for a relative phase offset error per subarray channel to be calculated that is directly related to the phase errors between each subarray. After this phase offset error is calculated for all three channels relative to the reference Channel 1, the calculated NCO phase offsets are applied and compensate for this phase error on a per channel basis such that all subarrays are aligned in phase.

After this, the original three channels in subarrays 2, 3, and 4 are disabled and three separate channels in subarrays 2, 3, and 4 are enabled. A simultaneous capture of all four channels, relative to the baseline Channel 1 on Subarray 1, allows for the phase errors to be calculated for these three new channels. Once these phase errors are computed, the BFIC phase shifters are used to compensate for this phase error. This process is repeated until all channels are phase-aligned in both the analog and digital domains. To align each channel in Subarray 1, the phase aligned Channel 3 in Subarray 2 is used as a comparison point, as it was phase aligned earlier with the first step of the calibration sequence. The result is a situation where the analog phase adjustments compensate for phase errors within a subarray, whereas the NCO phase offsets compensate for phase errors across subarrays.

FFTs

All performance measurements are evaluated based on FFTs of continuous wave (CW) data captures. Signal generators are set to coherent frequencies and no weighting is applied in the FFTs. Figure 7 shows representative FFTs of single tone measurements.

The plots from left to right are: a single element enabled, all eight elements in the subarray, and four subarrays digitally combined. From these FFTs we can begin to observe the hybrid beamforming impact to receiver dynamic range.

- As N elements are enabled in the subarray, the signal power increases 20logN. The noise power also increases, and the overall SNR improves.
- As subarrays are combined digitally, there is bit growth in the data. Performing FFTs based on the extra bits results in the signal level relative to full scale remaining the same, but the noise is reduced relative to full scale.
- Spurious content on many of the elements increase in magnitude at the subarray level but is uncorrelated across the subarrays and is reduced into the noise at the full array level.

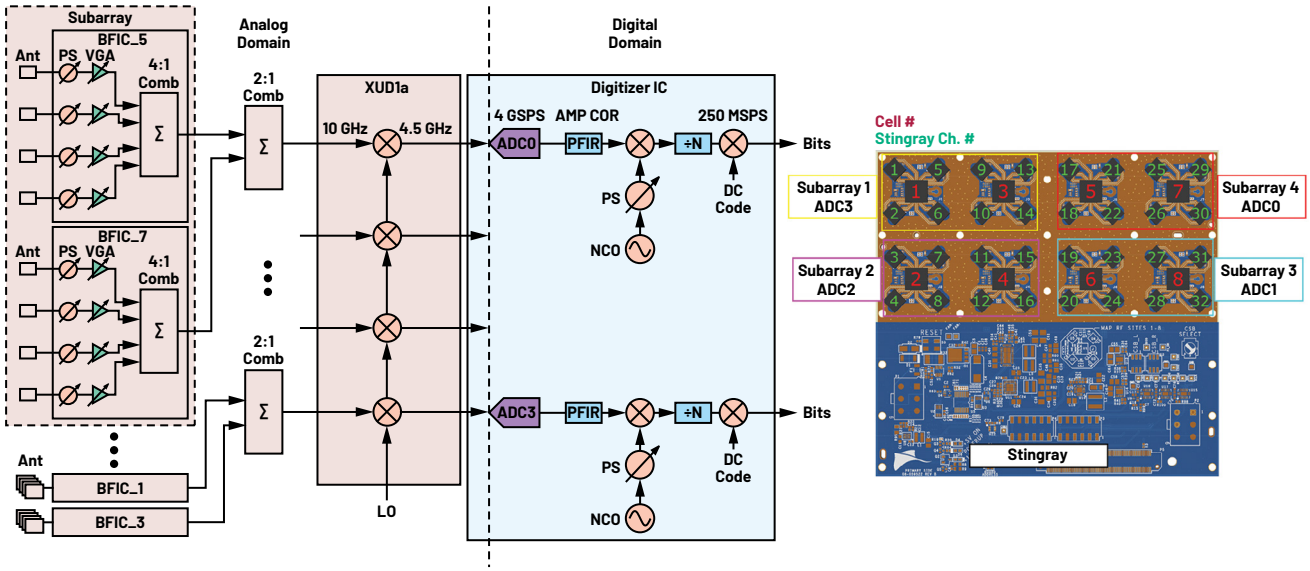

Figure 6. The calibration leveraged both analog phase control and digital phase control knobs.

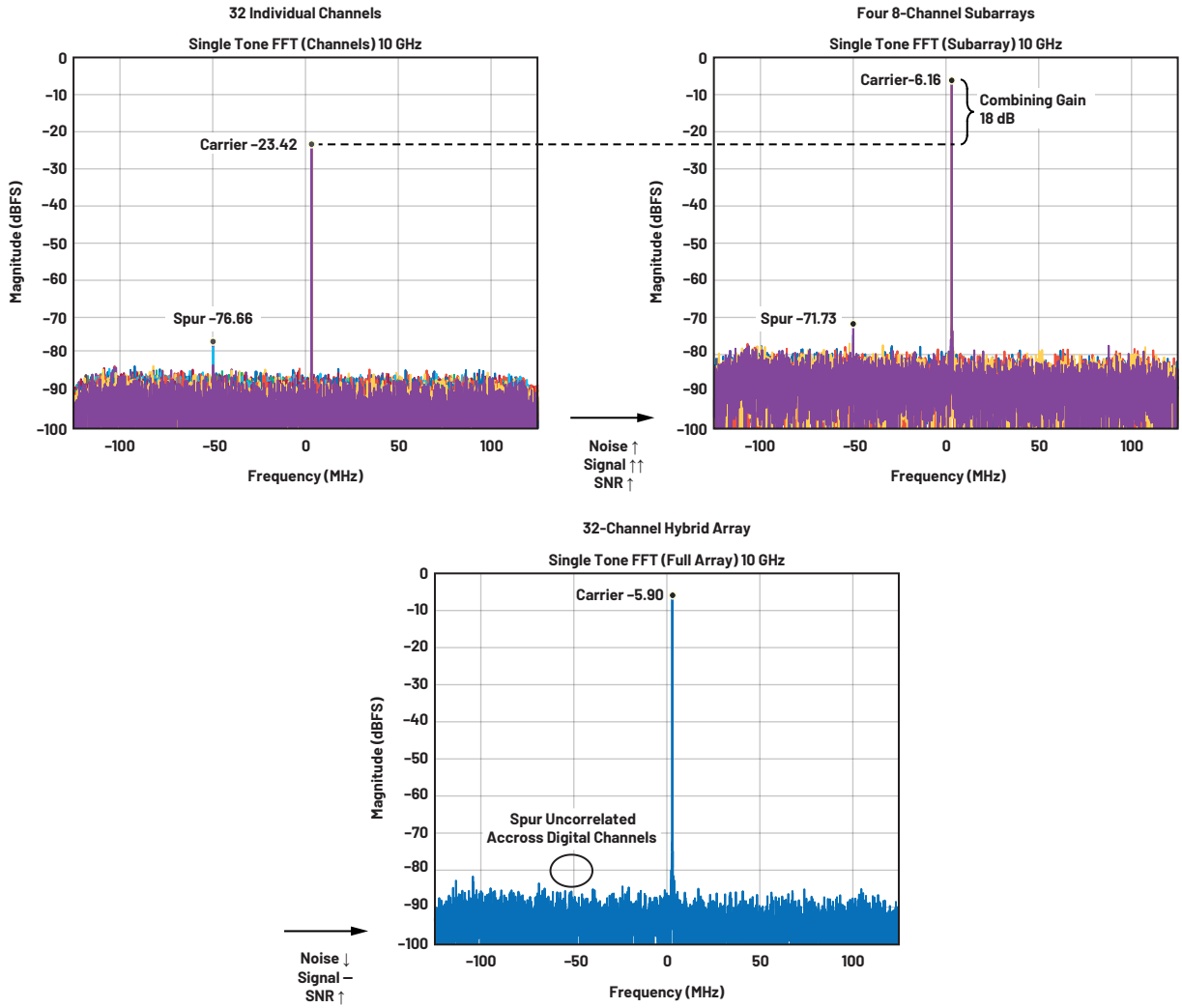

Figure 7. Single Tone FFT showing the RF input with ~10 GHz, –50 dBm, LO = 14.5 GHz, 5 dBm, the ADCs with 4 GSPS, coarse NCO = 550 MHz, DDC: 16×, 250 MSPS I/Q data rate, and FFTs with 4096 samples.

Figure 8 shows representative FFTs of two-tone measurements. These plots from left to right are: a single element enabled, all eight elements in the subarray, and four subarrays digitally combined. The FFT span is reduced to enable the visualization of the intermodulation products.

The intermodulation products increase as elements are enabled. This is due to higher power in the circuitry after the combiner and thus higher intermodulation products. However, as analog subarrays are combined digitally, the magnitude of both the two-tone signals and the intermodulation products approach the average.

Correlated phase noise off the skirt of the main carrier is observed in the case of this test configuration. In this configuration there is a common LO, a common RF input, and common power supplies across all the channels. In practice for large arrays, this should be avoided. Further discussion of tracking correlated vs. uncorrelated noise in arrays is discussed in the articles "Empirically Based Multichannel Phase Noise Model Validated in a 16-Channel Demonstrator," "A Measurement Summary of Distributed Direct Sampling S-Band Receivers for Phased Arrays," and "System-Level LO Phase Noise Model for Phased Arrays with Distributed Phase-Locked Loops."

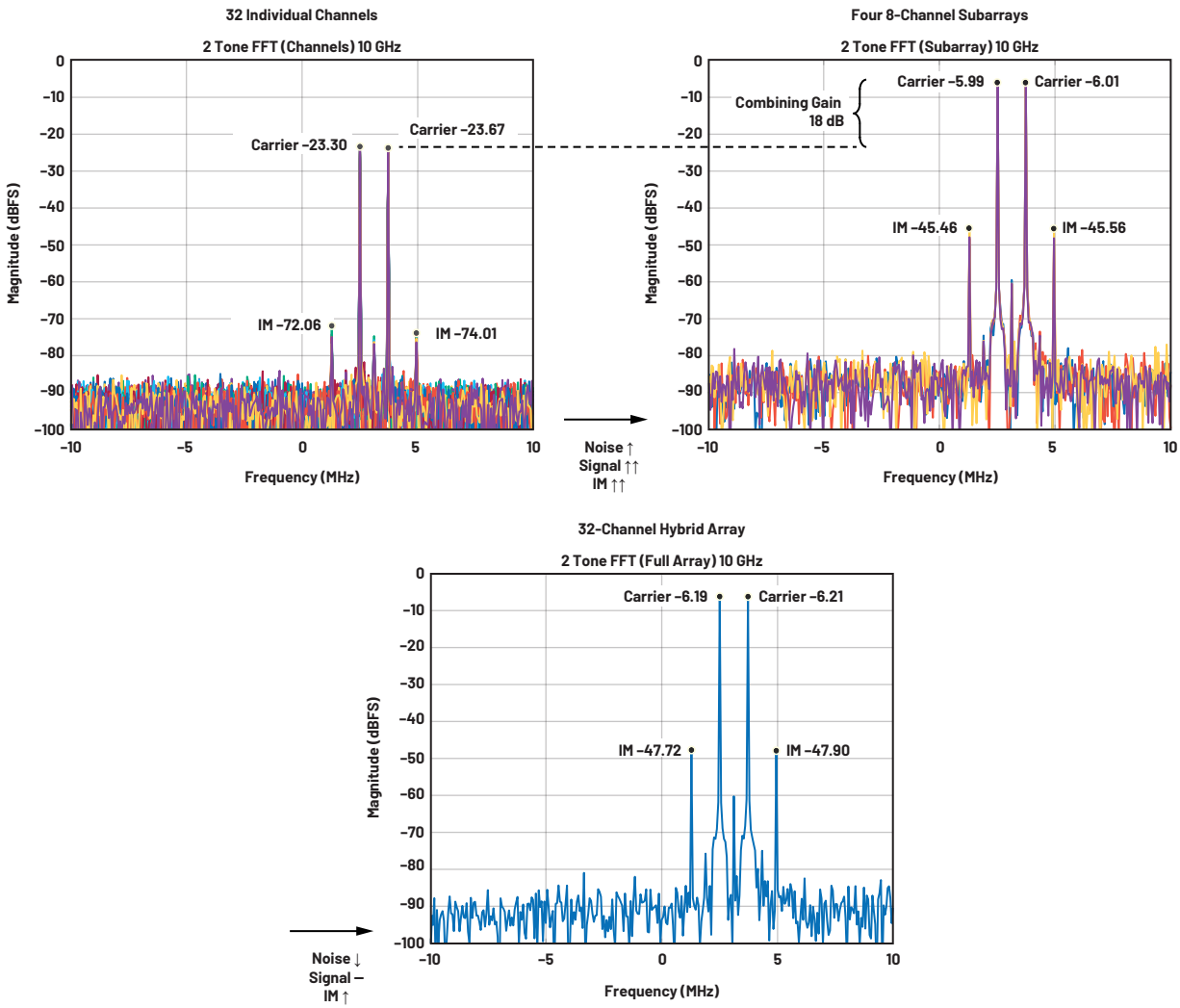

Figure 8. Two-tone FFTs with RF input: ~10 GHz, -50 dBm LO = 14.5 GHz, 5 dBm, ADCs with 4 GSPS, coarse NCO = 550 MHz, DDC: 16×, 250 MSPS I/Q data rate, and FFTs with 4096 samples, plots zoomed to ±10 MHz.

Performance Measurements

A comprehensive receiver performance measurement summary is provided in Figure 9.

Figure 9a is the magnitude relative to full scale of the FFTs across frequency. Using this data along with the input power, the receiver full scale level can be calculated as shown in Figure 9b.

Figure 9c is the noise spectral density (NSD) in dBFS/Hz that is calculated in the FFT processing. Several FFT bins around the carrier were removed so the noise represents white noise and is not impacted by the phase noise of the test configuration.

Based on Figure 9a and Figure 9c, the signal-to-noise ratio (SNR) can be calculated and is shown in Figure 9d. Two effects are observed. First, at the subarray level the SNR increases slightly more than 10logN. This is because noise power after combing is higher and the noise figure of devices after the combiner have less impact. Second, the SNR increases 10logN as subarrays are combined digitally.

Figure 9e shows the spurious-free dynamic range (SFDR) of individual elements, subarrays, and the full digitized array. We see a continual improvement as more elements are added to the array, indicating all spurs in the test configuration are uncorrelated.

Figure 9f shows the input third-order intercept point (IIP3). This result follows intuitively from the two-tone FFTs. The subarray IIP3 is lower due to the inter-modulation products increasing. The array-level IIP3 approaches the average of the subarray level.

Note for all these measurements, the data is remarkably close to the modeled values in the cascaded analysis. The modeled values are included for all plots except Figure 9d and 9e because those plots are determined indirectly and are not explicitly defined in the spreadsheet.

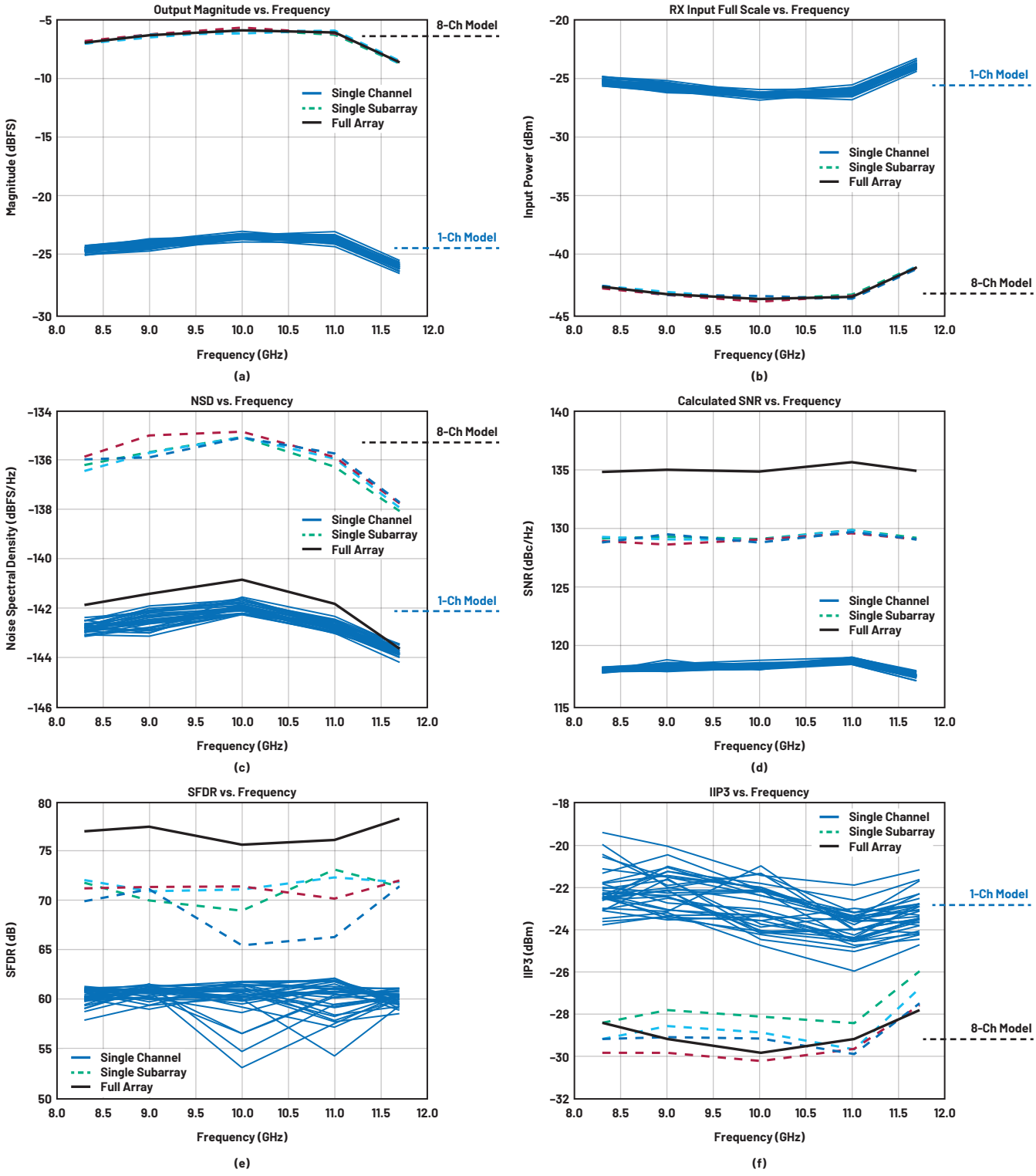

Figure 9. Receiver performance measurements.

Summary of Observations

Starting with the assumption that all signals are aligned in phase and amplitude, measurements agree well with predictions. The cascaded analysis requires separating signal gain and noise gain at the point of the analog combiner. Tracking noise power based on noise input and device input-referred noise is an effective method.

At the subarray level when turning channels on:

- SNR improves slightly greater than 10logN.
  - Signal increases 20logN.
  - Noise increases slightly less than 10logN.
    - Noise power after the analog combiner is larger.
    - The NF of components after the analog combiner has less impact.
- IIP3 decreases as signals combine due to larger signals at devices after the analog combiner.
- Spurs are generally correlated within the analog subarray. This is because the source is after the analog combiners and so the same spur is measured regardless of whether the microwave channel is enabled.

As subarrays are combined digitally:

- SNR increases 10logN
  - Signal power remains constant
  - The noise power in dBFS/Hz decreases
- IIP3 approaches the average
- Spurs observed are uncorrelated across digital channels.

Correlated phase noise terms are worth noting. Correlated phase noise is observed in this test configuration. This can be seen with the close-in noise in Figure 8 where the frequency axis is zoomed enough to show the effect. A common microwave input and LO input from test equipment is used. This means the microwave signals and LO phase noise are correlated. Shared power can also cause a correlated contribution and voltages are shared in this test configuration. In this test configuration we did not debug the dominant sources of correlated phase noise during receiver testing. However, this point is noted and remains an area for future investigation in this hardware.

Acknowledgements

The authors would like to acknowledge the many engineers at Analog Devices who made this work possible. This includes IC designers, circuit board designers, software developers, and technicians who assembled the prototype hardware. We would also like to thank the application-oriented managers who demonstrated foresight in the value of the test platform and showed patience during the lengthy process to bring the test platform to reality. Our description documents the receiver test results, but without the work of many others this description would not have been possible.

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