

How to Select a Boost Regulator/Controller IC and Use LTspice to Select Peripheral Components

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Introduction

The process of selecting an IC for a boost regulator is different than that for a buck regulator, where the main difference lies in how desired output current relates to regulator IC data sheet specifications. In a buck topology, the average inductor current is essentially the same as the load current. This is not the case for a boost topology, which requires calculations based on switch currents. This article covers both the selection criteria for a boost regulator IC (with internal MOSFET) or a controller IC (with external MOSFET), and how to use LTspice* to select appropriate peripheral components to complete the boost power stage.

Why Switch Current Is Important

What are the input and output voltages? This is the first question one asks when selecting a buck (step-down) or boost (step-up) dc-to-dc converter. The second question: what is the output current required to satisfy expected loads? Even though the input and output questions are the same for bucks and boosts, the process of selecting a suitable IC to satisfy input and output requirements is very different between bucks and boosts.

The first hint that the selection process for boosts is different from that for bucks is apparent if you compare a selection table of buck ICs vs. a selection table of boost ICs. Figure 1 shows the selection table for some internal power switch bucks. It can be seen that output current gets billing as one of the main selection parameters.

Part Number Filter parts	Number of II Outputs	Vin II min V	Vin max V	Output II Current typ A	Vout Min II typ V	Synchronous
1100	1 8	650m - 7.5	5 - 150	15m - 20	0 - 5	3 Values Selected ¥
351 parts	HIDE	HIDE	HIDE	HIDE	HIDE	HIDE
LTC3307A NEW	1	2.25	5.5	3	500m	Yes
LTC3308A NEW	1	2.25	5.5	4	500m	Yes
LTC3309A NEW	1	2.25	5.5	6	500m	Yes
LT8636 NEW	1	3.4	42	5	970m	Yes
LT7101 NEW	1	4.4	105	1	1	Yes
LTC3315A NEW	2	2.25	5.5	2	500m	Yes
LTC3376 NEW	4	3	20	3	400m	Yes
LT86538 NEW	2	2.6	42	2	800m	Yes
LT8650S-1 NEW	2	3	42	4	800m	Yes

Figure 1. Internal power switch buck selection table showing the output current as a selection parameter. Compare Figure 1, a selection table of internal power switch bucks, to Figure 2, a selection table of internal power switch boosts. In the boost table, output current does not even show up as a selection parameter, making way for switch current instead.

Part Number Filter parts	Number of II Outputs		Vin II min V		Vin max V	Switch Current typ A	Vout Max typ V	Synchronous
149 parts	1 HIDE	4	20m HIDE	5	500m - 100 HIDE	8m - 7.5 HIDE	3 - 140 HIDE	3 Values Select
ADP5072 NEW	2		2.85		5.5	1	35	No
ADP5076 NEW	2		2.85		5.5	2	2	No
LT8361	1		2.8		60	2	100	No
LT8362	1		2.8		60	2.5	60	No
LT8364	1		2.8		60	5	60	No
LT8335	1		3		25	2.5	28	No

Figure 2. Switch current shows up as a parameter in a selection table for a boost converter *IC*, instead of output current.

Another clue that boosts don't follow the same rules: the data sheet title for a boost has a subtle but important statement about current. For example, Figure 3 shows the front page of the data sheet for the LTC3621 monolithic buck, where 17 V max V_{IN} and 1 A continuous load capability are prominently noted.

	LTC3621/LTC3621-2
FEATURES	17V, 1A Synchronous
Wide V _{IN} Range: 2.7V to 17V	Step-Down Regulator with
Wide V _{OUT} Range: 0.6V to V _{IN}	3.5µA Quiescent Current
• 95% Max Efficiency • Low $I_Q < 3.5\mu A$, Zero-Current Shutdown	DESCRIPTION
Constant Frequency (1MHz/2.2SMHz) Full Dropout Operation with Low I _Q 1A Rated Output Current 1 ⁴ % Output Voltage Accuracy Current Mode Operation for Excellent Line and Load Transient Response	The LTC®3621/LTC3621-2 is a high efficiency 17V, 1A synchronous monolithic step-down regulator. The switching frequency is fixed to 1MHz or 2,25MHz with a 440% synchronizing range. The regulator features ultralow quiescent current and high efficiencies over a wide V _{0UT} range.

Figure 3. The LTC3621 buck regulator data sheet front page shows max typical operating voltage and current.

In contrast, the title of the data sheet for the LT8330 monolithic boost states the max voltage (60 V) and current (1 A) for the switch (the internal power MOSFET), instead of the typical maximum values for the load current and input voltage.

You can also see that for a boost the input voltage range of 3 V to 40 V differs from the 60 V max switch voltage.

	LT8330
	Low I _Q Boost/SEPIC/ Inverting Converter with <u>1A, 60V</u> Switch
FEATURES	DESCRIPTION
3V to 40V Input Voltage Range Ultralow Quiescent Current and Low-Ripple Burst Mode® Operation: 1 ₀ = 5µA 1A, 60V Power Switch	The LT®8330 is a current mode DC/DC converter capable of generating either positive or negative output voltages using a single feedback pin. It can be configured as a boost, SEPIC or inverting converter consuming as low as
 Positive or Negative Output Voltage Programming with a Single Feedback Pin 	6μA of quiescent current. Low ripple Burst Mode opera- tion maintains high efficiency down to very low output

Figure 4. The LT8330 boost regulator IC data sheet front page shows max power switch capabilities.

So, why the difference? In a buck regulator, the average inductor current is about equal to the output (load) current, whereas in a boost topology, this is not the case. Let's look at why by examining the boost topology in comparison to a buck.



Figure 5. An asynchronous boost.

Figure 5 shows the simplified schematic for an asynchronous boost topology, and Figure 6 shows the simplified schematic of an asynchronous buck topology. The D block for both is the PWM signal that drives the power MOSFET, with the duty cycles of switching periods determined by the input and output voltage ratio. In this article, to keep it simple I am using lossless continuous conduction mode (CCM) equations as they provide close enough results.





By using LTspice, we can clearly see the difference between the input and output currents of the two different topologies. Figure 7 shows a basic open-loop design for a buck, converting a 12 V input to a 3.3 V output that will provide 1 A (3.3 W) to the resistive load, R1. The PWM D block is implemented by V2, a floating supply, as we need $V_{GATE} > V_{SOURCE}$ to establish conduction for the N-channel MOSFET, M1. V2 is used as a PULSE voltage source to implement a 0 V to 5 V pulse, which begins at time 0 of the simulation, transitions from 0 V to 5 V in 5 ns and back down again in 5 ns with a T_{NN} of 550 ns, while T_{P} (full switching period) is equal to 2 µs.



Figure 7. A buck regulator open-loop topology converting 12 V to 3.3 V at 1 A—an approximately 3 W design.

After running the simulation of the circuit in Figure 7, it is possible to probe the currents of L1 and R1. The current in L1 has a triangle shape as it charges and discharges due to the switching of M1 according to the timing of T_{ON} , the time M1 is on, and T_{OFF} , the time M1 is off.

The L1 current switches at a 500 kHz switching frequency. We can see that the inductor current is an ac + dc waveform. It transitions from a minimum value of 0.866 A (end of $T_{\rm OFF}$) to a maximum value of 1.144 A (end of $T_{\rm ON}$). As ac signals look for the path of least impedance, the ac portion of the current flows through the ESR of output capacitor C2. This alternating current, along with the charging and discharging of C2, results in output voltage ripple, while the direct current flows via R2.

Comparing the triangular shapes of the inductor current formed above and below the load current, we can see they are equal, and simple algebraic calculation shows that:

$$\frac{I_{L(MAX)} + I_{L(MIN)}}{2} = \frac{1.144 \text{ A} + 0.866 \text{ A}}{2} = 1.005 \text{ A}$$
(1)

The average inductor current is equal to the load current.



Figure 8. Buck topology-inductor current and load current simulation example.

When searching for a buck regulator IC, it is safe to assume the data sheet shows the maximum allowed output current, as $I_{IN} \approx I_{OUT}$, but this is not the case for the boost topology.

Let's look at Figure 9, which shows an open-loop boost design for a 3.3 V input to a 12 V output at 0.275 A, or about 3.3 W. What is the average inductor current in this case?

In Figure 10, the output current is the dc trace at 291 mA, I(R2)-close to what was computed. While the simulated load current is 291 mA, the simulation shows that the inductor current has an average value of 945 mA and a peak value of more than 1 A. This is more than 3.6 times the output current. During T_{nn} —the time in which M2 is conducting, and there is a voltage of V3 across L2-the inductor charges from its minimum value to its maximum value. During T_{on} , D2 is off and the load current is provided by the output capacitors.

During T_{0N} , the inductor is in series with the MOSFET, so any current flowing through the input inductor flows through the switch. Because of this, the data sheet specifies the maximum current that can flow through the switch, Isw. One should know the expected maximum current through the switch (and the inductor) when selecting a boost IC for a new design.

For example, take a boost regulator for the following application:

- ► V_{IN} = 12 V
- ► V_{OUT} = 48 V
- ► I_{OUT} = 0.15 A

Choosing the correct boost regulator requires one to find the average input current, as this is the current that flows through the inductor and MOSFET during T_{on} . To find this current, work backward from output to input according to output power and efficiency:

- Pout = Vout × Iout = 48 V × 0.15 A = 7.2 W
- Assume an efficiency of 0.85 (or use the data sheet if there is an efficiency curve with similar input and output parameters to the desired design).
- P_{IN} = P_{OUT}/efficiency = 7.2 W/0.85 = 8.47 W
- I_{IN} -AV = the average input current. This is the same average current that flows in the inductor and switch during the on-time, which is calculated by $P_{IN}/V_{IN} = 8.47 \text{ W}/12 \text{ V} = 0.7 \text{ A}.$
- \blacktriangleright Again, I_{IN} is the average inductor current, the maximum peak current will be 1.15 to 1.20 higher than $I_{\mbox{\tiny NV}}$ allowing for 30% to 40% of ripple current. So, $I_{PFAK} = I_{IN} \times 1.2 = 0.7 \text{ A} \times 1.2 = 0.847 \text{ A}.$





Figure 9. Boost topology: 3.3 V to 12 V, approximately 3.3 W.



Figure 10. LTspice simulation result for open-loop boost from 3.3 V to 12 V at 0.275 A.



Figure 11. Schematic during T_m: M2 is on, V3 is in parallel to L2, and D2 is off.

$V_{\mbox{\scriptsize sw}}$ the Transistor Maximum Allowable Voltage and Duty Cycle Limitation

Usually the V_{IN} range of an IC is specified in the data sheet—both a recommended range and absolute maximum values. The highest output voltage possible from a boost regulator with an internal power switch is stated in the data sheet as its maximum V_{SW} rating. If you use a boost controller with an external MOSFET as the power switch, the MOSFET's data sheet-stated V_{DS} rating is what limits the maximum output voltage.

For example, the LT8330 boost regulator has an input voltage range of 3 V to 40 V, an absolute maximum switch voltage of 60 V, and a fixed switching frequency of 2 MHz. Although the absolute maximum 60 V switch voltage rating makes it possible for the part to generate a boost output to 60 V, it is best practice to remain below this by at least 2 V.

The output voltage is also limited by the duty cycle. The maximum and minimum duty cycle might be in the data sheet, or it can be calculated. Using the LT8330 to convert 12 V to 48 V, for CCM omitting the diode voltage drop for a high conversion ratio, the duty cycle is computed from the input and output voltage:

- $D = (V_0 V_{IN})/V_0 = (48 \text{ V} 12 \text{ V})/48 \text{ V} = 0.75 \text{ or } 75\%$
- Check to see if the IC is able to work at the duty cycle required.
- ► The IC minimum duty cycle is given by:
 - **D**_{MIN} = minimum $T_{ON(MAX)} \times f_{SW(MAX)}$
- ▶ And the IC maximum duty cycle is given by:
 - D_{MAX} = 1 (minimum $T_{OFF(MAX)} \times f_{SW(MAX)}$)

Minimum $T_{\rm ON}$ and Minimum $T_{\rm OFF}$ can be found in the Electrical Characteristics table in the data sheet. Use the max values from the table's min, typ, and max columns. Using the published values of the LT8330 and in the $D_{\rm HIN}$ and $D_{\rm HAX}$ equations result in $D_{\rm HIN}=0.225$ and $D_{\rm HAX}=0.86.$ From the result, we can see that the LT8330 should be able to convert 12 V to 48 V, as the design calls for a duty cycle of 0.75.

Understanding Peripheral Stresses Using LTspice

The schematic shown in Figure 12 realizes the design concept previously introduced featuring the LT8330 in a 12 V input to 48 V output converter supporting 150 mA loads.



Figure 12. The LT8330 used in a 12 V to 48 V converter for 150 mA load current.

From the LTspice simulation we can plot and measure a number of parameters. Those that can help you choose an IC are described in Figure 13.

V_{sw} and Duty Cycle

After running the simulation, you can view the SW node behavior as a waveform to understand what voltages are present on the power switch during a switching period. To do so, hover over the SW node so that the crosshair cursor changes to a red voltage probe. Click to plot the switch node behavior on the waveform viewer. The resulting graph corresponds to the drain of the internal power MOSFET.

As expected, when the MOSFET conducts, the voltage potential is close to ground, but more importantly, during T_{OFF} , the MOSFET is off and the drain voltage is subject to the output voltage plus a diode drop. Now we know what stress is on the V_{DS} of the MOSFET. If we chose a controller design that uses an external MOSFET as the power switch, we should have chosen a MOSFET that has a V_{DS} rating of 60 V.

In the LTspice waveform viewer, one can use cursors to make horizontal and vertical measurements, similar to the cursors on an oscilloscope. To invoke the cursors, click the **V(sw)** label in the LTspice waveform viewer. This attaches the first cursor to the trace, and another click attaches a second cursor to the same trace. Alternatively, right-click the label and choose the desired cursors to a given probed trace. Using these cursors, you can measure T_{0N} and calculate the duty cycle, given by T_{0N} /Period.

 $T_{\text{PENIOD}} = T_{\text{ON}} + T_{\text{OFF}} = 1/f_{\text{SW}}.$ Earlier, we calculated this to be 75% or 0.75. Using LTspice we get approximately 373 ns. The LT8330 uses a fixed switching frequency of 2 MHz, so $T_{\text{P}} = 1/2e6 = 500$ ns, so the duty cycle is 373 ns/500 ns = 0.746.



Figure 13. Switch node plot on the graphical viewer in LTspice.



Figure 14. Measuring T_{ov} to verify the estimated duty cycle.

Peak Current Through and Voltage Across the Inductor

To choose an inductor for your boost application, you need to know if the inductor can handle the currents and voltages it will face—namely the peak inductor current, and the T_{ON} and T_{OFF} voltages. This can also be estimated in LTspice using differential probes. To probe differentially across the inductor, hover over the IN node, and the crosshair cursor will change to a red probe. Click and drag the mouse to the SW node. The cursor color changes to black. Release when over the second node.

In Figure 15, the voltage between nodes IN and SW are probed differentially across the inductor. During $T_{_{ON'}}$ the MOSFET conducts, so the right side of the inductor is near ground, while the left side is at $V_{_{IN'}}$ making the voltage across the inductor 12 V during $T_{_{ON'}}$. During $T_{_{OFF}}$ the MOSFET is off, placing the right side of the inductor at 48 V, while the left side is at $V_{_{IN'}}$ as during $T_{_{ON'}}$. Because the differential probe subtracts $V_{_{SW}}$ from $V_{_{IN'}}$ the result is -36 V, but the sign is irrelevant (for now). What is important is that the inductor changes between 12 V and 36 V.

During T_{ON} , the voltage across the inductor draws a positive di/dt, the slope of the blue I(L1) graph. The maximum point of this trace is I_{PEAK} , calculated as 0.847 A. Using LTspice, we can see that the peak current is about 866 mA.

The peak current is important to know in order to properly choose an inductor with sufficient rated current (IR) and saturation current (I_{SAT}). IR is more about how much heat is generated at the stated current, and I_{SAT} applies to events invoking short-circuit protection. If a regulator with internal MOSFETs is used, (I_{SAT} > regulator current limit), and if a controller is used with external MOSFETs, then (I_{SAT} > the peak inductor value) when the current limit is triggered.

It is important to note that the boost topology as described here has no current limit for the inductor or diode. If the switch is not used, or the IC is off, there is a direct path between input to output. There are ICs that provide additional protection features, such as output disconnection in shutdown, inrush current limiting, and other features to address this direct input to output connection—for example, the LTC3122 and LTC3539.

To improve efficiency, inductors featuring low DCR (dc resistance) and low core losses should be used. DCR is noted in the inductor data sheet at a particular temperature—it rises with temperature and has a tolerance. The dc losses can be easily computed from $P_{INDUCTOR_LOSS} = I_{NL,W}^2 \times DCR$, while the ac losses and core losses can be found in manufacturers' simulation or other documentation. LTspice can integrate power to calculate associated power loss. Providing LTspice with an inductor's documented DCR and other known parasitic parameters improves LTspice simulation accuracy.



Figure 15. Voltage and current through the inductor at steady state.



Figure 16. Measuring the inductor peak current.

Current and Voltage Through the Diode

Figure 17 shows the simulated differential voltage across the diode $V_{SW,OUT}$, the diode forward current I(D1), and the inductor current I(L1). When the switch is on (during T_{oN}), the anode is close to ground and the cathode is at the output voltage, so the diode is reverse biased and exposed to its maximum voltage, namely V_{oUT} . Selecting a diode that has V_{RRH} (maximum peak repetitive reverse voltage) higher than V_{oUT} is the first criteria.

The inductor's peak current flows through the diode once the MOSFET is turned off, at the commencement of the $T_{\rm OFF}$ period, so the diode peak current is the same as the inductor peak current. The diode data sheet includes a parameter called $I_{\rm FRM}$, the repetitive peak forward current, specified at a time duration and duty cycle. This parameter is usually higher than the average current the diode can provide.

After simulation is completed, LTspice can integrate any waveform in the waveform viewer to produce rms and average values and, by the same measure, the average current the diode will face. First, zoom in on the part of the waveform you want to integrate—zooming effectively sets the integration bounds. In this case, you want to zoom to cover a significant number of steady state cycles (not startup or shutdown). To set the integration bounds, drag over a steady state time period and hover over the graph name. For instance, the integration result shown in Figure 18 covers 0.75 ms, or over a thousand cycles. The cursor changes to a hand icon. Press the CTRL key and click to invoke the integration window of the waveform viewer.

The integration dialog box shown in Figure 18 displays the average current through the diode, which is 150 mA. This should be less than the IF(AV), maximum average forward current, specification in a diode data sheet, usually stated at a specific case temperature.

Diode Power Dissipation

The power dissipation of the diode can also be computed from the simulation. A diode data sheet specifies P_{T0T} (total power), the total power dissipation at 25°C, and R_{TH} , the junction-to-ambient thermal resistance. In LTspice, the power dissipation can be displayed on the waveform viewer by hovering over the diode; when you hover over a body of a discrete component or a voltage source, the mouse cursor changes to a current probe. Press the ALT key to change the cursor to a thermometer, and click to show the simulated power dissipation over the diode. Zoom in on steady state operation to integrate the waveform using the same procedure as previously described for the integration of the diode









Figure 19. Integration of power dissipated by the diode to yield average power dissipation.



(b)

Figure 20. Reverse recovery spike cause at the diode discharge. A lower value means lower power loss. This capacitance changes with voltage. (a) Diode reverse recovery current spike. (b) Zooming in on the diode reverse recovery current spike.

current. Diode power handling comprises the voltage across the diode and the current that flows through it.

The diode has some capacitance that is charged during its conduction period. The accumulated charge must be discharged when the diode no longer conducts. This damped charge movement results in loss of power, so selecting a low capacitance value is recommended. This capacitance value changes with the diode's reverse voltage, and a diode data sheet should include a graph displaying this effect. This internal capacitance is typically shown in diode data sheets as C_d and in the LTspice database as C_{ip} .

Using a low capacitance diode relaxes the requirements of the maximum reverse recovery current, improving efficiency. Figure 20 shows what to look for regarding recovery current. The power dissipation inherent in the reverse recovery is left as an exercise to the reader.

Conclusion

When selecting a boost IC, start at the output. Work backward from the desired output voltage and load current to find input power, taking efficiency into account. From this, determine the average and peak input current values. In a boost, the average current flowing in the inductor is higher than the load current, making the IC selection process different from that of a buck. Choosing properly rated components for a boost converter requires knowledge of the regulator peak and average voltages and currents, which can be determined using LTspice.

About the Author

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