

How to Prioritize Efficiency and Cost with the Lattice CertusPro-NX FPGA Evaluation Board

James R. Staley, Applications Engineer, and Matthias Bust, Principal Engineer

Abstract

Modern field programmable gate array (FPGA) families such as the Lattice Semiconductor CertusPro[™]-NX are suitable for a wide range of applications, but the power requirements are tailored to specific market-driven demands. Choosing the optimum approach to power these devices can be challenging without understanding how to carefully balance the triad of cost, performance, and size. This article provides a look at solutions for the CertusPro-NX Evaluation Board but also gives insight as to the how and why of what each solution offers for optimizing the solution to a particular need. While µModule[®] power solutions provide a very compelling design approach to FPGA systems because of their small size and design simplicity, there are additional options a power systems architect might consider.

Introduction

The Lattice Semiconductor CertusPro-NX Evaluation Board is designed to allow users to investigate and experiment with the features of the CertusPro-NX FPGA. Its features can assist users with the rapid prototyping and testing of their specific design. Included in this evaluation system are the on-board regulators for the power supply options of the FPGA. Most of the power supply rails are selectable for the user's preference.

The goal of this paper is to provide an updated power recommendation for each power supply option of the Lattice Semiconductor CertusPro-NX FPGA Evaluation Board. Considering the design complexity, efficiency, solution size, and cost, this power solution must include state-of-the-art and best performing power products. It is often the case that evaluation boards are designed with a power architecture to show off the full feature set of the FPGA. This approach is necessary for evaluation but may not lend itself well to adoption into systems that do not require full performance. It may be too large for scaled down implementations that are optimized for small physical board size. Which solution works best for a given CertusPro-NX application will depend on which priorities the system architect finds most compelling for a particular project. The discrete solution—a dedicated power IC with external power components prioritizes efficiency performance and cost over physical layout size. In systems where the most compact form factor is the priority, the µModule solution from Analog Devices offers unrivaled energy density that cannot be achieved by a conventional layout, while still giving a performance edge over the existing CertusPro-NX reference design. This reference design is unique in this regard because it allows system architects to choose which version of the power solution they wish to incorporate into their platform based on their intimate knowledge of their own desired platform design goals and constraints. By carefully studying the data from both versions, a deliberate choice can be made about which design will be a better fit with the size, performance, and cost trade-offs to maximize alignment with the project engineering specifications.

CertusPro-NX Evaluation Board Power Architecture

The CertusPro-NX Evaluation Board has most of the on-board regulators powered by an external 12 V power source. Each VCCIO pin of the FPGA has its default and selectable supply options for the users' preference according to their applications. Figure 1 shows the usable voltage rails that are linked to the specific VCCIO pins of the FPGA. Voltage options available for the VCCIO pins are summarized in Table 1.



Figure 1. CertusPro-NX FPGA VCCIO pins voltage options.

Table 1. VCCIO Supply Options

VCCIO Bank	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V	V-ADJ
VCCIOO	Selectable		Default			
VCCI01	Fixed					
VCCI02	Default	Selectable	Selectable			
VCCI03						
VCCI04			Selectable		Selectable	Default
VCCI05						
VCCI06	Default	Selectable	Selectable			
VCCI07	Fixed					

Each of the voltage rails used by the VCCIO pins of the FPGA is produced by various on-board voltage regulators. The main supply is powered via an external 12 V DC source, which is discussed in Section 1.4 of the CertusPro-NX Evaluation Board User Guide. Figure 2 shows the different voltage output rails produced by the on-board regulators powered via a 12 V DC external voltage supply. LDO regulators are also used for postregulation to produce a lower voltage while reducing noise at the output.



Figure 2. CertusPro-NX Evaluation Board power scheme.

Recommended Power Solution Architectures

As input voltage to the evaluation board, a regulated 12 V wall adapter is used. Given this input source and the required voltage levels on the board, a single stepdown approach can be used to generate all the necessary voltage rails directly from 12 V. If the user needs a wider input voltage range, or uses a higher input voltage (for example, 24 V), one may consider switching to a 2-step approach, generating first an intermediate voltage rail of, for example, 5.0 V or 3.3 V that can then be used to supply the following regulators generating the lower voltages, as shown in Figure 3.



Figure 3. Two step-down vs. single step-down approach.

The decision about which topology is selected has an impact on various parameters like efficiency, the switching frequency of each converter, and total solution footprint. These need to be carefully considered in every new implementation to optimize the power architecture for every new product design. Also, proper input protection and a filter circuit might be necessary.

Two power solution variants for the CertusPro-NX Evaluation Board were designed with different priorities in mind, both using the single step-down approach described. The first one is a discrete solution that uses monolithic DC-to-DC regulators with provisions for external circuitry that allows the user to optimize components for the best performance for each rail individually. The second one is a fully integrated solution using ADI's µModule technology, which gives the application the most compact and simplest layout solution possible while still providing excellent power solution performance.

The updated power solution architectures for the CertusPro-NX Evaluation Board are available in LTPowerPlanner[®], a tool that allows the optimization of systemlevel power trees. LTpowerCAD[®] is then used to provide a detailed circuit proposal per the selected DC-to-DC IC including the calculation of estimated circuit performance based on the entries for the IC usage and the surrounding passive components. These programs are part of a tool suite for Windows that can be downloaded from the LTpowerCAD webpage. This webpage also provides documentation, training material, and videos to get started.

The Discrete Power Solution

The discrete power solution offers the best individual DC-to-DC regulator performance for each rail by allowing the designer to optimize the external circuit components for a particular solution. The updated discrete power solution recommendation offers significant performance improvements over the existing power solution. All DC-to-DC regulators use synchronous internal switches to maximize efficiency while still maintaining a compact design and outstanding EMI performance. Figure 4 shows the discrete solution power tree for the CertusPro-NX Evaluation Board.

Switching Regulators

LT8653S

The LT8653S features second-generation Silent Switcher[®] architecture to minimize EMI emissions while delivering high efficiency at high switching frequencies. With a wide V_{IN} range and dual 2 A outputs, this is an ideal selection candidate.

ADP2387

Two of the rails that have voltages of 1.8 V and 3.3 V are required to deliver output currents that are higher than the LT8653S can deliver. They are 4 A and 3 A, respectively. With these requirements, the ADP2387 was identified to be an ideal candidate for the application.

Linear Regulators

MAX38903C

Used as a postregulator with a high noise rejection on a 1 V rail of the CertusPro-NX Evaluation Board, the MAX38903C is a low noise linear regulator that delivers up to 1 A of output current with only 5.5 µV rms of output noise from 10 Hz to 100 kHz. This low output noise and high noise rejection property of the MAX38903C makes it a smart choice to use in the power solution for the CertusPro-NX Evaluation Board.

ADP1707

The ADP1707-1.8 is a CMOS, low dropout linear regulator that has an output voltage of 1.8 V and provides up to 1 A of output current available in a 3 mm × 3 mm exposed paddle LFCSP. This makes it a very compact solution and also one that provides excellent thermal performance for applications requiring up to 1 A of output current in a small, low profile footprint suitable for the power solution of CertusPro-NX Evaluation Board.

The µModule Power Solution

Without sacrificing the quality of performance, the module solution on the other hand offers the smallest and simplest solution by utilizing ADI's µModule technology. Analog Devices' µModule regulators and DC-to-DC power products are complete system-in-a-package (SiP) power management solutions with integrated DC-to-DC controllers, power transistors, input and output capacitors, compensation components, and inductors within a compact, surface-mount BGA or LGA package. µModule power products support functions such as step down, step down and step up, battery charger, isolated converter, and LED drivers.

Figure 5 shows the power solution tree for the CertusPro-NX Evaluation Board using μ Module parts. The first stage after the external 12 V input supply is the μ Module DC-to-DC regulator array. The next stage is comprised of linear regulators. The linear regulators chosen are the same in both the μ Module design (Figure 5) or the discrete solution (Figure 4).



Power Tree for CertusPro-NX Evaluation Board : General Purpose FPGA - Discrete Solution

Figure 4. A discrete solution power tree modeled by the LTPowerPlanner tool.



Power Tree for CertusPro-NX Evaluation Board : General Purpose FPGA - uModule Solution

Figure 5. µModule solution power tree.



Figure 6. The VDD_1V8 and VCC_3V3 rail schematic diagram for discrete solution.

Switching Regulator Modules

LTM8078

The LTM8078 is a 40 V_{IN} dual 1.4 A/single 2.8 A step-down Silent Switcher µModule regulator. Its Silent Switcher architecture minimizes EMI while delivering high efficiency at frequencies that can be up to 3 MHz. Included in the package are the controllers, power switches, inductors, and support components. Operating over a wide input voltage range and a switching frequency range of 300 kHz to 3 MHz, each set by a single resistor, only the bulk input and output filter capacitors are needed to finish the design—making it an ideal power solution option for the CertusPro-NX Evaluation Board.

LTM4625

The LTM4625 is a complete 5 A step-down switching mode µModule regulator in a tiny 6.25 mm × 6.25 mm × 5.01 mm BGA package. Its high efficiency design delivers up to 5 A continuous output current. Only bulk input and output capacitors are needed. High switching frequency and current mode control enable a very fast transient response to line and load changes without sacrificing stability.

The LTM8078 and LTM4625 μ Module switching regulators provide the simplest quality solution, eliminating the complexity and avoiding space constraints.

Power Solution Design Detailed Description for CertusPro-NX Evaluation Board

Discrete Solution Design

From the recommended operating conditions stated in the CertusPro-NX FPGA data sheet, the supply voltages should be within ±5% of the typical value. In the design, the DC output error brought by the tolerances of the feedback resistor and the V_{REF} voltage of the regulators, the output voltage ripple and the load transient response are already considered in the 5%. With those errors present, it will still fall within the 5% allowable value for recommended operating conditions of the FPGA.

Complete data for all rails are available from ADI's Customer Office Solutions Group, but Table 2 includes selected rails to show typical representative performance for the 1.35 A LT8653S and 3 A/4 A ADP2387 outputs.

Table 2. Discrete Design Efficiency and RipplePerformance Data

Rail	Device	V _{ουτ} (γ)	Load (A)	Efficiency (%)	Ripple p-p (%)
VDD_1V8	LT8653S	1.8	1.35	86.20	0.91
VCC_3V3	LT8653S	3.3	1.35	90.65	0.42
VCC_ADJ	ADP2387	1.8	4.00	90.92	0.67
VDD_3V3	ADP2387	3.3	3.00	94.31	0.72

Rail 1: VDD_1V8

This voltage rail requires a 1.8 V output voltage and should be capable of delivering up to 1.35 A output current. This requirement is met by using one channel of the LT8653S. The $\pm 5\%$ total output voltage error at the application's output load current is carefully observed in the design to ensure that the recommended operating condition is met.

To achieve high DC accuracy, the internal reference feature is utilized. The channel of this part is configured to 1.8 V feedback reference voltage eliminating the error caused by the resistor values and tolerance. Figure 6 shows the LTPowerCAD-generated schematic for the VDD_1V8 and VCC_3V3.

During the evaluation of the rail to ensure that the output is within the recommended operating condition, the load transient response was evaluated with a very fast and high load step as the stimulus. The step load is set to 0 A to 1 A step with a 10 A/ μ s slew rate and 150 μ s pulse duration. Figure 7 shows the transient load response of the VDD_1V8 rail. The top waveform CH2 shows the output response while the bottom waveform CH4 shows the output load current.



Figure 7. VDD_1V8 transient load response.

Table 3. VDD_1V8 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.057	3.2	4.0
Undershoot	0.055	3.2	4.0

From the result, considering the overshoot and undershoot during the load transient and including the output ripple, the voltage is within the recommended operating condition of $\pm 5\%$.

Rail 2: VCC_3V3

The VCC_3V3 rail utilizes the second channel of the LT8653S together with the VDD_1V8. Just like the VDD_1V8, the VCC_3V3 rail must be capable of delivering 1.35 A output current as a supply on VCCI0 pins of the CertusPro-NX FPGA. There is also an IC option for a fixed 3.3 V output that comes with an internal trimmed feedback divider and therefore will lead to high DC accuracy. The schematic and circuit component values are also shown in Figure 6 while the transient response is shown in Figure 8. The top waveform CH2 shows the output response while the bottom waveform CH4 shows the output load current. Table 4 shows the transient load response result, where both the overshoot and undershoot, including the output ripple, maintain a voltage within the recommended operating condition of $\pm 5\%$.



Figure 8. Load transient response of the VCC_3V3 rail.

Table 4. VCC_3V3 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.054	1.6	4.0
Undershoot	0.052	1.6	4.0

Rail 7: VCC_ADJ

The VCC_ADJ voltage rail requires a 1.8 V output voltage and should be capable of delivering up to 4 A output current to the VCCIO and FMC connector. The $\pm 3\%$ total output voltage error at the application's output load current is carefully observed in the design to ensure that the recommended operating condition is met.

To achieve high DC accuracy, the internal reference feature is utilized. The error amplifier of this part is configured to 1.8 V feedback reference voltage to compensate for resistor values and tolerance.

The rail transient response was evaluated with a high slew rate current step to ensure the output voltage always remains within tolerance limits during operation. The step load is set to 0 A to 1 A step with a 10 A/ μ s slew rate and 150 μ s pulse duration. Figure 9 shows the transient load response of the VDD_1V8 rail. The top waveform CH2 shows the output response while the bottom waveform CH4 shows the output load current.



Figure 9. VCC_ADJ transient load response.

Table 5. VDD_1V8 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.048	2.7	3.0
Undershoot	0.048	2.7	3.0

From the result, considering the overshoot and undershoot during the load transient and including the output ripple, the voltage is within the recommended operating condition of $\pm 5\%$, and better than the target value of 3%.

Rail 8: VDD_3V3

The VDD_3V3 rail must be capable of delivering 3 A output current as a supply for the FMC connector pins of the CertusPro-NX FPGA board. The transient response is shown in Figure 11. The top waveform CH2 shows the output response while the bottom waveform CH4 shows the output load current. Table 6 shows the transient load response result, where both the overshoot and undershoot, including the output ripple, maintain a voltage within the recommended operating condition of $\pm 3\%$.





Table 6. VDD_3V3 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.09	2.7	3.0
Undershoot	0.082	2.5	3.0

µModule Solution Design

The same specifications as the previous section for the discrete design apply to the μ Module recommendations, so these will not be discussed in detail here. The μ Module solution trades off some performance for a much smaller footprint in layout. The same sample points will be shown as a comparison.

Complete data for all rails are available from ADI's Customer Office Solutions Group, but Table 7 includes selected rails to show typical representative performance for the 1.35 A LTM8078 and 3 A, 4 A LTM4625 outputs.

Table 7. µModule Design Efficiency and Ripple Performance Data

Rail	Device	V _{OUT} (V)	Load (A)	Efficiency (%)	Ripple p-p (%)
VDD_1V8	LTM8078	1.8	1.35	83.38	0.25
VCC_3V3	LTM8078	3.3	1.35	88.88	0.19
VCC_ADJ	LTM4625	1.8	4.00	83.02	0.11
VDD_3V3	LTM4625	3.3	3.00	89.60	0.11

Rail 1: VDD_1V8

Channel 1 voltage rail utilizes 0.1% resistors to ensure compliance with the DC + transient total tolerance margin requirements of the application. Figure 11 shows the captured waveform data for the worst-case load step, and Table 8 shows a summary of the captured cursor data.



Figure 11. VDD_1V8 transient load response.

Table 8. VDD_1V8 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.0708	3.9	4.0
Undershoot	0.0682	3.8	4.0

Rail 2: VCC_3V3

The VCC_3V3 rail (Channel 2 of the LTM8078) also utilizes 0.1% resistors to ensure compliance with the voltage margin requirements of the application. Figure 12 shows the captured waveform data for the worst-case load step, and Table 9 shows a summary of the captured cursor data.



Figure 12. VCC_3V3 transient load response.

Table 9. VCC_3V3 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.109	3.3	4.0
Undershoot	0.107	3.2	4.0

Rail 7: VCC_ADJ



Figure 13. VCC_ADJ transient load response.

The LTM4625 Channel 1 voltage rail utilizes standard 1% resistors to ensure compliance with the DC + transient total tolerance margin requirements of the application. Figure 13 shows the captured waveform data for the worst-case load step, and Table 10 shows a summary of the captured cursor data.

Table 10. VCC_ADJ Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.019	1.1	3.0
Undershoot	0.024	1.3	3.0

Rail 8: VDD_3V3

The VDD_3V3 rail (Channel 2 of the LTM3625) also utilizes 1% resistors to ensure compliance with the voltage margin requirements of the application. Figure 14 shows the captured waveform data for the worst-case load step, and Table 11 shows a summary of the captured cursor data.



Figure 14. 1VDD_3V3 transient load response.

Table 11. VDD_3V3 Rail Transient Load Data

Parameter	Voltage (V)	Percentage (%)	Target Limit (%)
Overshoot	0.03	1.7	3.0
Undershoot	0.036	2.0	3.0

Conclusion

Sound power architecting requires carefully balancing the trade-offs associated with size, performance, and cost. One of the two designs will be a better fit for any CertusPro-NX platform. As mentioned previously, complete efficiency, ripple, and transient data for all rails of both designs are available upon request. The results show that either discrete or module design approaches are capable of meeting the CertusPro-NX performance parameters with a margin to spare. Any future designs should incorporate whichever approach is best suited to the target market. The authors hope that careful analysis of the dataset and design philosophy presented in this article enables Lattice FPGA power incorporation with confidence. The design engineer, system architect, and project manager alike can all share a common understanding of the trade-offs associated with power part and topology selection. Whatever priorities an individual design specification calls for, ADI power solutions can then be tailored to more closely fit the particular criteria.

About the Authors

James R. Staley is an industrial power systems engineering manager for Analog Devices. He graduated Eta Kappa Nu from North Carolina State University with a B.S.E.E. concentration in nanotechnology and has over 20 years of semiconductor industry experience. He has held positions with applications engineering, sales applications engineering, and systems engineering at Linear Technology and Analog Devices. His current focus is on industrial and precision instrumentation power systems. James and his family reside in the Raleigh, North Carolina area.

Matthias Bust joined Analog Devices in 2007 and currently works in the Customer Office Solutions Team as an expert for power products. In his previous roles in ADI, Matthias worked as a systems manager for automotive power products and as a field applications engineer serving customers in all market areas. He has over 30 years of industry experience and has held positions in hardware/software design, systems engineering, and supply chain management in the telecommunication and laser industry. Matthias graduated with a diploma in electronic engineering and information technology from the Technical University of Ilmenau, Germany.

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