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How to Get the Best Results Using LTspice for EMC Simulation—Part 1

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Abstract

As technological innovations such as IoT connected devices and 5G connectivity become part of our everyday lives, so too does the need to regulate the electromagnetic emissions from these devices and quantify their immunity to EMI. Meeting EMC compliance targets is often a complex task. This article provides open-source LTspice® simulation circuits to answer key questions: (a) will my system pass EMC testing, or do I need to add mitigation techniques? and (b) how immune is my design to noise from the external environment?

Why Should I Use LTspice for EMC Simulation?

Design for EMC should follow the product release schedule as closely as possible, but this is often not the case, as EMC problems and lab testing can delay product release for months.

Usually, simulation focuses on the functional aspects of an electronic device; however, a simple and open-source tool such as LTspice can also be used to simulate the EMC behavior of any device. With many of us working from home, and EMC lab costs at a premium (up to $2000 daily), accurate EMC simulation tools are even more useful. Spending a few hours simulating EMC failures and circuit fixes helps to avoid multiple lab test iterations and expensive hardware redesigns.

To be useful, an EMC simulation tool needs to be as accurate as possible. This article series provides some guidelines and LTspice EMC circuit models that are simulated and well matched to real lab measurements.

This is Part 1 of a series of three articles that provide EMC simulation models for an example sensor signal chain, with a MEMS vibration sensor at its core. However, many of the components and EMC simulation techniques are not unique to MEMS solutions and can be used across a broad range of applications.

- Part 1: power supply components and conducted emissions and immunity.
- Part 2: signal integrity and transient robustness on cable drive transceiver links.
- Part 3: signal conditioning components and boosting immunity to external noise.

Solving Emissions and Immunity Problems Using LTspice

After reading this article you should be able to answer the following key questions:

(a) Is my system likely to pass EMC testing? Shall I keep an extra footprint for a common-mode inductor, a filter inductor, or a capacitor? After reading this article you should be able to use LTspice to plot differential and common-mode noise in your buck converter power design and show how the circuit passes or fails conducted emissions standard limits, as shown in Figure 1.

(b) Is a linear regulator needed to provide stable voltage to my sensitive load? After reading this article you should be able to use LTspice to understand if an LDO regulator is required on the output of your buck converter based on the buck output ripple voltage level tolerable in your design. In addition, this article provides a configurable power supply noise immunity, or PSRR, test circuit.

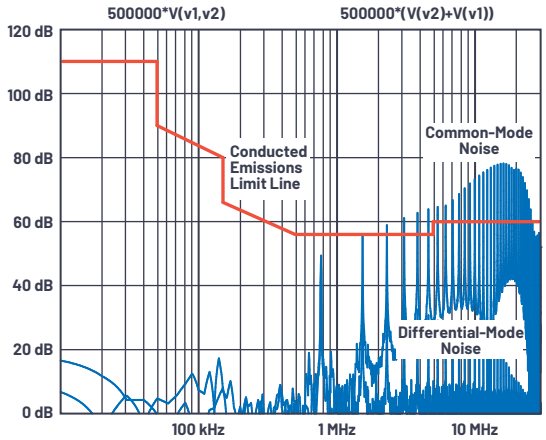

Figure 1. LTspice plot of differential and common-mode noise, with conducted emissions limit line.

Buck Converter for Sensors

MEMS vibration sensors are typically housed in small metallic enclosures, usually 20 mm to 30 mm in diameter and 50 mm to 60 mm in height. Sensors with digital signal chains are typically supplied with 9 V_{DC} to 30 V_{DC} over long cables and consume less than 300 mW. Tiny power solutions are required to fit inside this small enclosure, with high efficiency and wide input range.

The LT8618, LT8618-3.3, and LT8604 are compact, high speed step-down switching regulators ideally suited to MEMS sensor applications. LTspice models are already available for LT8618 and LT8618-3.3. The regulation of the LT8618 provides very low output ripple with less than 10 mV p-p. However, parasitic resistance and inductance of the output capacitor bank can increase this ripple, resulting in unwanted conducted emissions from the buck circuit. Parasitics can occur due to capacitive load, buck regulator output switching parasitics, and coupling capacitance between the PCB design and the sensor enclosure.

Extracting and Using Parasitic Values

The next sections describe how an engineer can extract the ESL and ESR parasitic values from real capacitors using Würth REDEXPERT and simulate the circuit using LTspice. At the input and output of many systems, capacitor and inductor parasitics play a major role in EMI performance. Splitting the individual parasitic contributions helps the user to make the best choice when it comes to reducing the system output ripple.

Conducted emissions simulation for a buck converter is discussed with an LTspice and Würth REDEXPERT process flow, as shown in Figure 2. Usually for a buck, output ripple is associated with signal-to-noise ratio (SNR), while input ripple is tightly linked to EMC performance.

After the Figure 2 simulation approach is outlined, this article then provides real lab measurements and simulation correlation using the DC2822A LT8618 demo board.

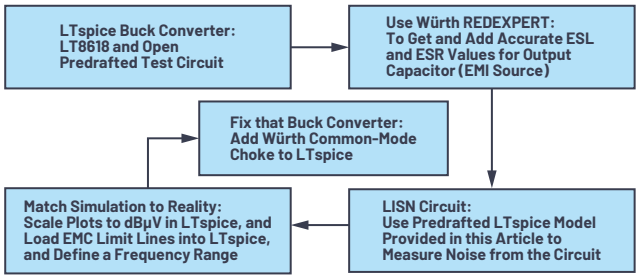

Figure 2. Process flow for simulating conducted emissions using LTspice.

LTspice Test Circuit with Würth REDEXPERT Data

The output ripple voltage of a buck converter is a function of the capacitor impedance and the inductor current. For better simulation accuracy, Würth REDEXPERT can be used to choose a 4.7 µF output capacitor (885012208040) and extract the ESR and ESL over frequency. The ESL and ESR are sometimes loaded into the LTspice capacitor model, but a quick check will demonstrate that ESL is often omitted in LTspice capacitor data. Figures 3a and 3b show two equivalent circuits: (a) with the 4.7 µF output capacitor, and discrete ESL and ESR values, and (b) with the Würth capacitor that includes ESR and ESL parameters.

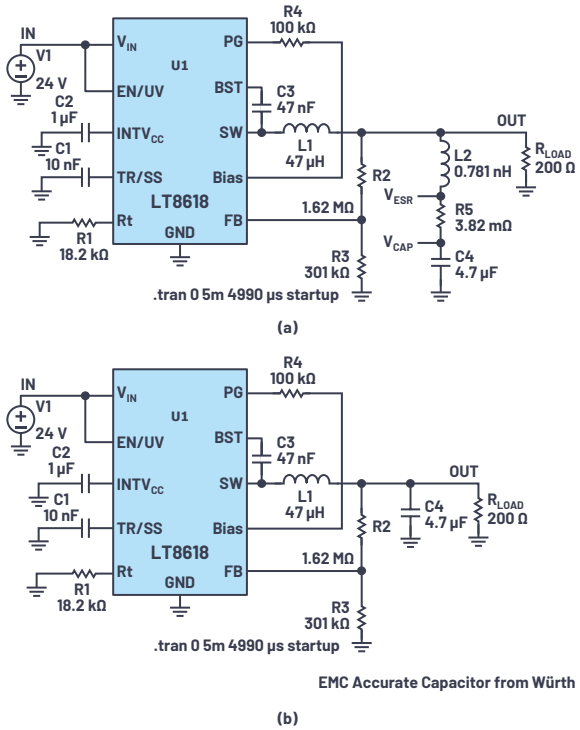

Figure 3. LTspice test circuits, (a) with the 4.7 µF output capacitor, and discrete ESL and ESR values and (b) with the Würth capacitor that includes ESR and ESL parameters.

REDEXPERT displays the impedance over frequency of many components, enabling determination of the key parasitics of each passive device. These parasitic values can later be implemented in LTspice models, enabling individual evaluation of contribution to total voltage ripple.

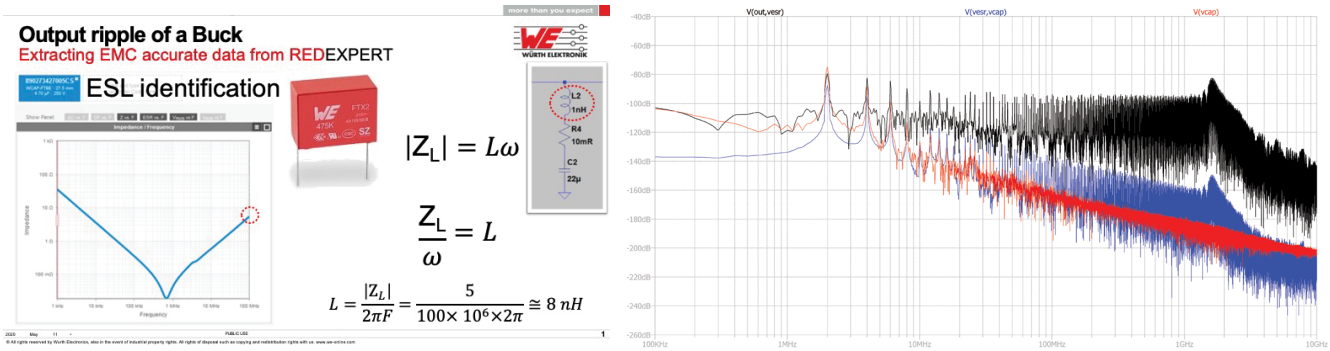

Figure 4. An FFT plot showing individual contribution to frequency spectrum due to pure capacitance, ESL and ESR of a 4.7 µF capacitor.

As mentioned previously, the LT8618 provides very low output ripple with less than 10 mV p-p. However, when simulating the effects of capacitive load and ESL, the output ripple voltage is 44 mV p-p. The capacitor ESL contributes significantly to noise over frequency, as is shown in the Figure 4 FFT plot.

Assessing EMI Compliance at Buck Input Using an LTspice LISN Circuit

To evaluate EMC compliance in conducted setups, most standards rely on a line impedance stabilization network (LISN) or artificial mains network (AMN). These devices have a similar function and are placed between the circuit power supply and device under test (DUT), here the buck converter. The LISN/AMN consists of low-pass and high-pass filters. The low-pass filters provide a path for low frequency power (DC to a few hundred Hz) to the DUT. The high-pass filters are used to measure supply and return supply line noise. These voltages are measured across 50 Ω resistors, as illustrated in Figure 5 and Figure 6.[1] In a real lab, this voltage is measured using an EMI receiver. LTspice can be used to probe the noise voltages and plot over the conducted emissions test frequency spectrum.

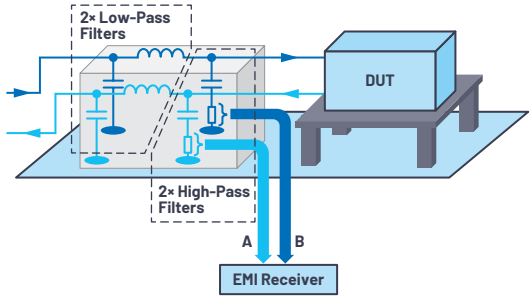

Figure 5. LISN placed between power supply and device under test (DUT).

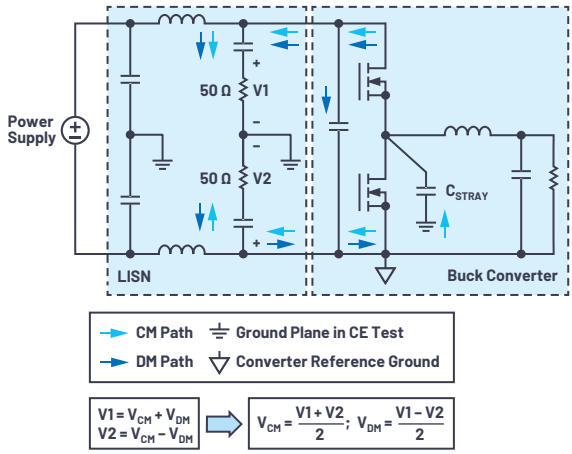

Figure 6. Representation of common- and differential-mode interference inside an LISN.[1]

Conducted emissions can be classified as common-mode (CM) noise and differential-mode (DM) noise. It is important to distinguish between CM and DM noise, as EMI mitigation techniques may be effective for CM but not for DM noise and vice versa. As both V1 and V2 voltages are outputted at the same time, an LISN can be used to separate out CM and DM noise in conducted emissions testing, as shown in Figure 6.[1]

DM noise is produced between the supply line and the return line, while CM noise is produced between the supply lines and the ground reference plane (such as a copper test table) via stray capacitance, C_{STRAY}. C_{STRAY} in effect models the switching noise parasitics at the buck converter output.

The LTspice LISN circuit corresponding to Figure 6 is shown in Figure 7. For greater simulation accuracy the L5 and L6 inductors are used to model the inductance of LISN supply leads to the test circuit. Resistor R10 models the impedance of the test board's slotted ground plane. Figure 7 also includes the capacitor C10 used to model C_{STRAY}. Capacitor C11 models parasitic capacitance between the sensor PCB and the sensor mechanical enclosure.

When running simulations, LTspice should be set up to help your LISN circuit reach steady state faster, as the wrong selection of start-up conditions can lead to long lasting oscillations.

Make sure that you untick **Start External DC Supply Voltages at Zero** and specify an **Initial Condition** (of voltage and current) of circuit elements if needed.

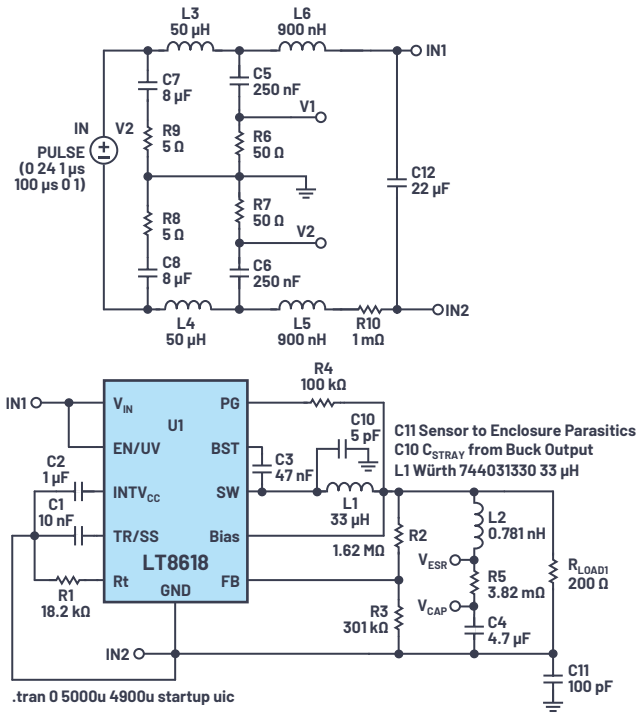

Figure 7. LTspice LISN circuit, LT8618 buck converter, and parasitic modeling.

Figure 8 shows the CM and DM noise using an LTspice FTT plot measured from the LISN terminals V1 and V2. To reproduce the arithmetic operations shown in Figure 6, the V1 and V2 are subtracted and multiplied by 0.5 for the DM noise, and V1 is added to V2 with the result multiplied by 0.5 for the CM noise.

Typically conducted emissions in a lab are measured in dBµV, while the default LTspice unit is 1 dbV. The relationship between the two is 1 dbV = 120 dBµV.

The LTspice expression for DM noise in dBµV is thus

$$V(v1,v2)\times 0.5\times 1000000 \quad (1)$$

and the expression for CM noise is

$$(V(v2)+V(v1))\times 0.5\times 1000000 \quad (2)$$

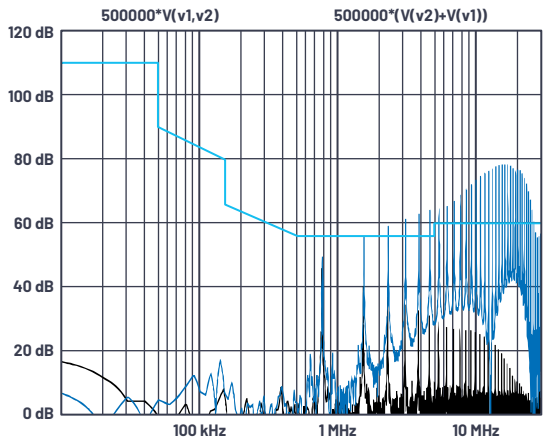

Figure 8. LTspice FFT plot for DM noise (black) and CM noise (blue).

Adding Conducted Emissions Limit Lines

The LTspice FFT waveform viewing parameters can be edited using the plot settings file. Using the LTspice FFT menu, navigate to **Save Plot Settings** and hit save. The plot settings file can be opened using a text editor and manipulated to add the EN 55022 conducted emissions limit line as well as the relevant EMC frequency range (10 kHz to 30 MHz) and amplitude (0 dBµV to 120 dBµV).

The EN 55022 conducted emissions standard frequency and amplitude limits can be manipulated using Excel to provide the correct syntax to copy and paste to the LTspice plot settings file, as shown in Figure 9. The line definition can be pasted to the plot setting parameters as shown in Figure 10. Figure 10 also shows the X frequency and Y amplitude parameters.

Start Freq, Hz	End Freq, Hz	Amp dBµV start	Amp dBµV stop	Line def for LTSPICE plot settings file	
9000	50000	110	110	Line: "dB" 4 0	(9000,316227.766016838) (50000,316227.766016838)
50000	50000	110	90	Line: "dB" 4 0	(50000,316227.766016838) (50000,31622.7766016838)
50000	2E+05	90	80	Line: "dB" 4 0	(50000,31622.7766016838) (150000,10000)
150000	2E+05	80	66	Line: "dB" 4 0	(150000,10000) (150000,1995.26231496888)
150000	5E+05	66	56	Line: "dB" 4 0	(150000,1995.26231496888) (500000,630.957344480193)
500000	5E+06	56	56	Line: "dB" 4 0	(500000,630.957344480193) (5000000,630.957344480193)
5E+06	5E+06	56	60	Line: "dB" 4 0	(5000000,630.957344480193) (5000000,1000)
5E+06	3E+07	60	60	Line: "dB" 4 0	(5000000,1000) (30000000,1000)

Figure 9. Generating the right syntax to copy and paste to the LTspice plot settings file.

```
[FFT of time domain data]
{
  Npanes: 1
  {
    traces: 2 {524290,0,"V(v1,v2)*500000"} {524291,0,"(V(v2)+V(v1))*500000"}
    X: ('M',0,10000,0,3e+007)
    Y[0]: (' ',0,1,20,1e+006)
    Log: 1 2 0
    GridStyle: 1
    PltMag: 1
    Line: "dB" 4 0 (9000,316227.766016838) (50000,316227.766016838)
    Line: "dB" 4 0 (50000,316227.766016838) (50000,31622.7766016838)
    Line: "dB" 4 0 (50000,31622.7766016838) (150000,10000)
    Line: "dB" 4 0 (150000,10000) (150000,1995.26231496888)
    Line: "dB" 4 0 (150000,1995.26231496888) (500000,630.957344480193)
    Line: "dB" 4 0 (500000,630.957344480193) (5000000,630.957344480193)
    Line: "dB" 4 0 (5000000,630.957344480193) (5000000,1000)
    Line: "dB" 4 0 (5000000,1000) (30000000,1000)

  }
}
```

Figure 10. Adding the conducted emissions pass/fail line definition and frequency/ magnitude scales.

Figure 11 shows the conducted emissions limit line, and the DM and CM conducted emissions from the buck circuit. The circuit fails emissions testing in the 2.3 MHz to 30 MHz frequency band.

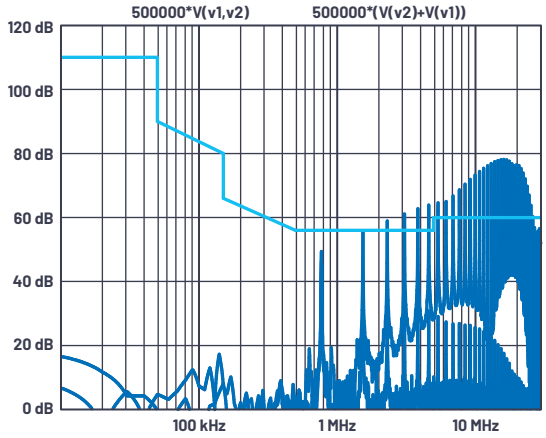

Figure 11. LTspice FFT plot and EN 55022 conducted emissions limit line.

Fixing the Buck Converter EMI

To reduce the DM noise from the circuit, a very low ESL and ESR capacitor can be placed at the input rail, such as the C12 22 µF Würth 885012209006, as shown in Figure 12.

To reduce CM noise, a Würth common-mode choke, such as the 250 µH 744235251 (WE-CNSW series), can be chosen from the LTspice library. The package size of 4.5 mm × 3.2 mm × 2.8 mm is ideal for space constrained MEMS sensor enclosures. Figure 13 shows the FFT plot of the fixed buck.

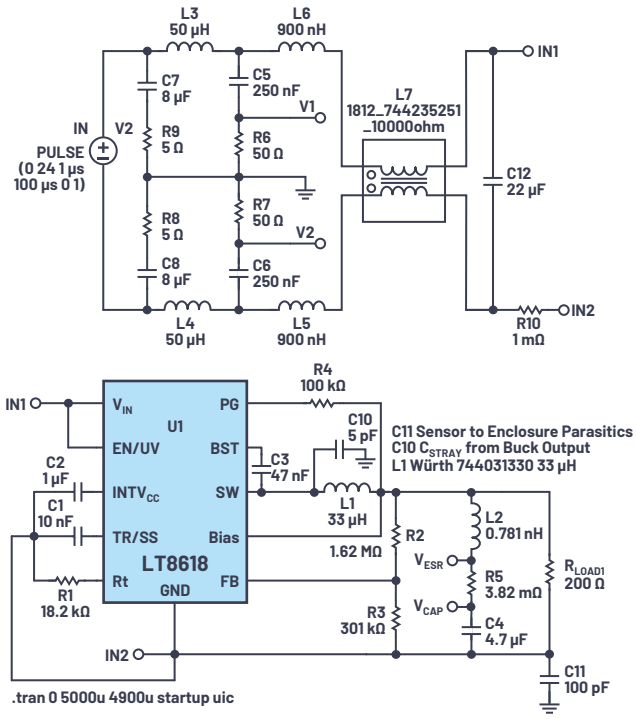

Figure 12. Fixing the buck converter emissions.

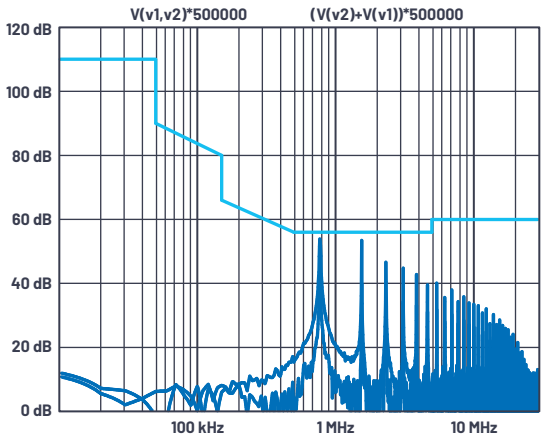

Figure 13. An FFT plot with buck converter fixed.

Real Lab Measurements and Simulation Correlation Using the DC2822A LT8618 Demo Board

This article has provided guidance for using LTspice for conducted emissions simulation. The methods can be used for any buck converter circuit. Now we turn our attention to simulation and EMC lab correlation using the DC2822A LT8618 demo board, shown in Figure 14. The DC2822A demo board includes several input and output capacitors, which were not included in previous simulation models (for example, Figure 7 and Figure 12). The LTspice model shown in Figure 15 includes these capacitors and the capacitor ESL and ESR values obtained using Würth REDEXPERT.

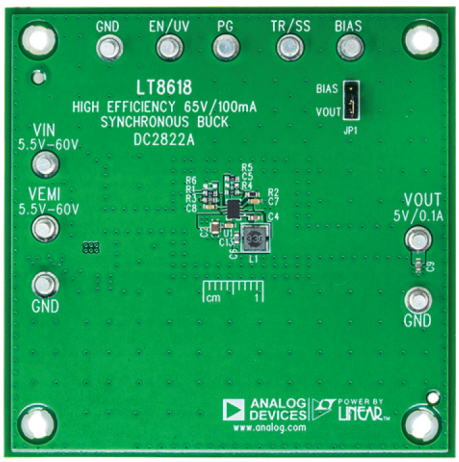

Figure 14. DC2822A LT8618 demo board.

The DC2822A demo board includes two power inputs, VIN and VEMI. The VIN input power rail bypasses the ferrite bead used on the PCB. The Figure 15 LTspice model corresponds to the demo board VIN configuration. Figure 16 shows the FFT of the LTspice simulation, with common-mode emissions narrowly failing the conducted emissions limit line at 2 MHz.

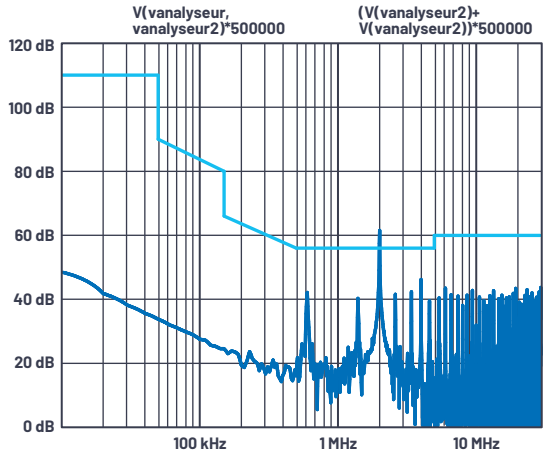

Figure 16. LTspice FFT plot corresponding to the DC2822A VIN configuration.

To reduce simulation time and to optimize matching the LTspice simulation to the DC2822A demo board lab measurements, the following changes were made to Figure 15 compared to previous models (Figure 7 and Figure 12):

- No need to model 100 pF capacitance between enclosure casing and PCB. We are just modeling a DC2822A demo board.
- Assuming from the outset that the switching noise is negligible on this well-designed PCB. Previously we estimated 5 pF for switching noise in Figure 7 and Figure 12.
- Ignoring the very small inductance of the wire leads between the LISN and the DC2822A demo board.
- Adding 1 kΩ resistors in parallel with the 50 µH LISN inductors to reduce simulation time (the LISN settling time is reduced).

With these changes in the Figure 15 circuit, Figure 17 shows a comparison of the LTspice simulation and actual measurement of the DC2822A demo board in an EMC lab. The LTspice simulation model predicts the actual lab emissions' major peaks with excellent accuracy.

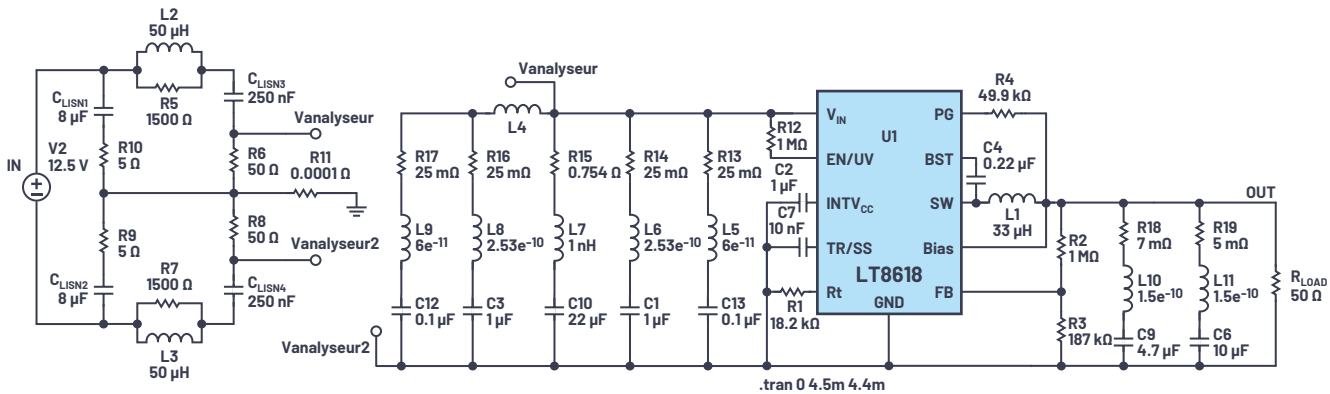

Figure 15. LTspice model corresponding to the DC2822A demo board VIN configuration.

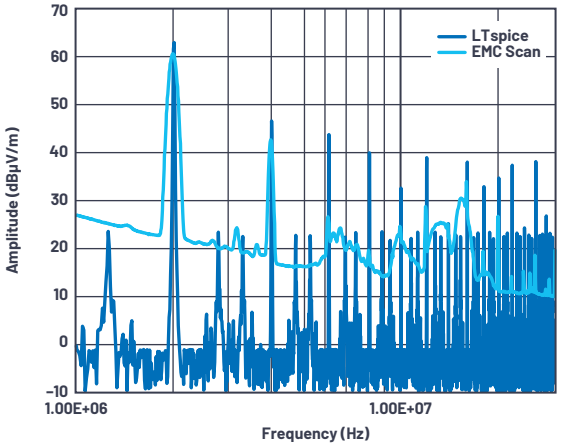

Figure 17. DC2822A VIN configuration, comparison of LTspice and actual EMC lab emissions.

With the ferrite bead (EMI filter) VEMI rail measurement, the DC2822A demo board easily passes the conducted emissions limit line of 60 dBµV. In fact, at lower frequencies the DC2822A demo board only has 30 dBµV to 35 dBµV of emissions.

Conducted Immunity

Wired condition monitoring sensors have stringent noise immunity requirements. For CbM of railway, automation, and heavy industry (for example, pulp and paper processing), vibration sensor solutions need to output less than 1 mV of noise to avoid triggering a false vibration level at the data acquisition/controller. This means that the power supply design needs to output very little noise (low output ripple) into the measurement circuit (MEMS signal chain). The power supply design must also be immune to noise coupled to the power supply cable (high PSRR).

As shown previously, the LT8618 can have tens of millivolts of output ripple due to nonideal capacitive loads and burst operation. For MEMS sensor applications, the LT8618 requires an ultralow noise and high PSRR LDO regulator at its output, such as the LT3042.

Flexible Simulation Circuit for Noise Immunity (PSRR)

The LTspice circuit shown in Figure 18 can be used to simulate the PSRR of the LT3042. The time domain transient model shown in Figure 18 is an alternative to the AC sweep method. This time domain model is more flexible than an AC method, and even allows the user to simulate the PSRR of a switching regulator. The simulation circuit frequency sweeps changes in the voltage input rail and simulates the corresponding change in output voltage. In other words, the simulation evaluates the equation: $PSRR_{LT3042}$ = (change in V_{IN})/(change in V_{OUT}) over frequency.

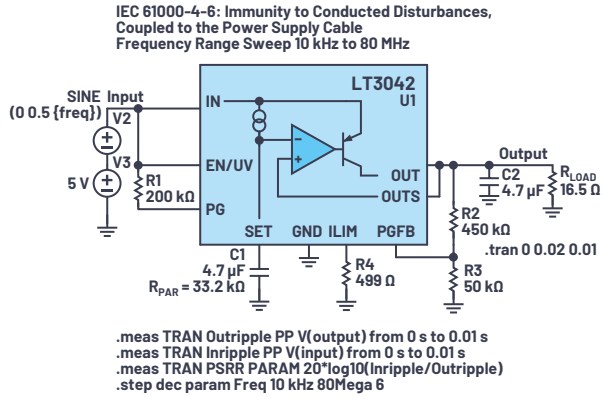

Figure 18. Simulating the PSRR of the LT3042 LDO regulator over 10 kHz to 80 MHz.

Figure 18 contains several powerful statements. The combination of .meas and .step statements enables the user to add a voltage noise source at the LDO input, and measure the LDO PSRR over a stepped change in voltage input over frequency.

.meas Statements

This allows the user to measure the peak-to-peak value of a signal over a time frame and output it to the SPICE Error Log. Figure 18 measures both input and output ripple, and calculates the PSRR of the measured data. All of this is outputted to the SPICE Error Log.

.step Statements

The .step command is useful for sweeping a variable across a range of values in a single simulation run. The .step statement in Figure 18 steps the V2 voltage source sine wave across a 50 Hz to 10 MHz range.

The C2 output capacitor initial voltage can be set to 3.3 V to speed up settling (and simulation) time. This is done by editing the capacitor properties, and it can be made even faster by disabling the **Start External DC Supply Voltage at 0 V** option in LTspice.

Using the SPICE Error Log

Once the simulation completes, right-click one of the windows, select view and select SPICE Error Log (or use the Ctrl+L hotkey). The **SPICE Error Log** contains data points for the .meas statements.

To plot the .meas data, right-click the error log and select the plot step'ed .meas data, right-click on the blank screen to select **Add Trace** (or use Ctrl+A) and select PSRR. Right-click the x-axis and check the radio button to display with logarithmic scale. This will display the PSRR over frequency, as shown in Figure 19.

Some artifacts from the original LT3042 data sheet curve are not visible (about 2 MHz), but the global shape and values are close to the data sheet.

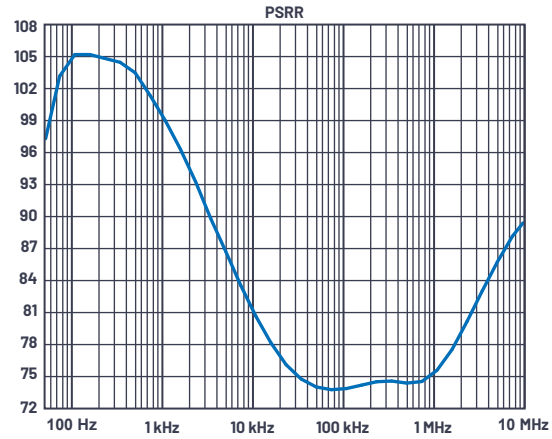

Figure 19. Plotting the simulated PSRR of the LT3042 LDO regulator.

Figure 20 shows the output voltage ripple over frequency. This is less than 200 µV over the 50 Hz to 10 MHz range. The input voltage ripple is 1 V p-p over the same frequency range. The LT3042 provides an excellent PSRR and low noise supply for noise sensitive MEMS solutions.

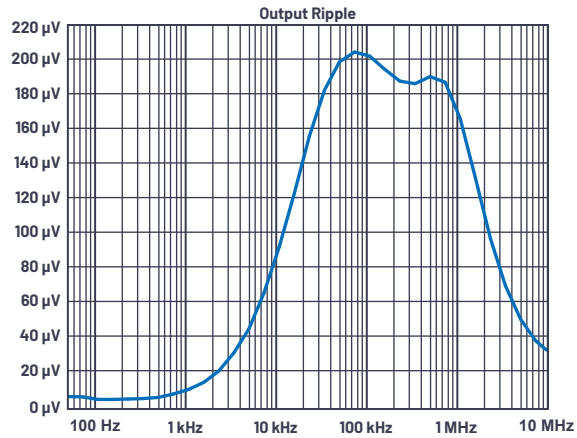

Figure 20. Plotting the LT3042 simulated output voltage ripple over frequency.

The .meas approach using the SPICE Error Log can be used to simulate many other parameters, including:

- PSRR of a switching regulator
- PSRR vs. dropout voltage vs. frequency
- PSRR vs. bypass network
- RMS output ripple vs. DC input
- Efficiency vs. component value

Summary

This article provides LTspice simulation circuits and methods to plot differential and common-mode noise in your buck converter power design. This article enables the user to plot conducted emissions limit lines and helps to predict EMC lab failures. The simulation approach is validated with lab measurements, with close correlation to the LT8618 DC2822A demo board.

Using the LT3042 LDO regulator at the output of the LT8618 buck converter provides an ultralow noise, high PSRR solution for MEMS sensor applications. A flexible simulation circuit for PSRR shows good agreement with the LT3042 data sheet. The LT3042 simulates with less than 200 µV output ripple over the 50 Hz to 10 MHz range, even in the presence of a large 1 V p-p input voltage noise.

Acknowledgements

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