Keywords: LED backlight, boost converter, high brightness, step-by-step, dc-dc converter

APPLICATION NOTE 6818

HOW TO DESIGN AN LED BACKLIGHT DRIVING SYSTEM USING THE MAX20446

Abstract: This application note details a step-by-step design process for the MAX20446 6-Channel Backlight High Brightness LED driver and highlights the calculations needed to speed up the selection of critical components. The trade-offs of component selection are also discussed. This application note focuses on the boost converter topology, and the same design process can be extended to other LED driver products.

Introduction

The MAX20446 is a peak current-mode-controlled LED driver, capable of driving up to six LED strings in several different configurations: boost, buck-boost, SEPIC, and flyback topologies. This application note focuses on the boost topology in which the LED string forward voltage is always higher than the input supply voltage range.

The MAX20446 offers the following features:

- Six integrated current outputs that can sink up to 120mA LED current each
- Integrated spread-spectrum and phase shifting
- I^2C-controlled pulse-width modulation (PWM) dimming and hybrid dimming
- Programmable switching frequency between 400kHz and 2.2MHz.

For this LED backlight driving system design example, six 7-LED strings are driven with a constant current of 100mA each. Assume that each LED has a maximum expected forward-voltage drop of 3.3V and minimum expected forward-voltage drop of 2.7V. Also assume that the LED driver circuit is directly fed by the car battery, which has a typical V_{IN} of 12V but can vary from 5V to 16V.

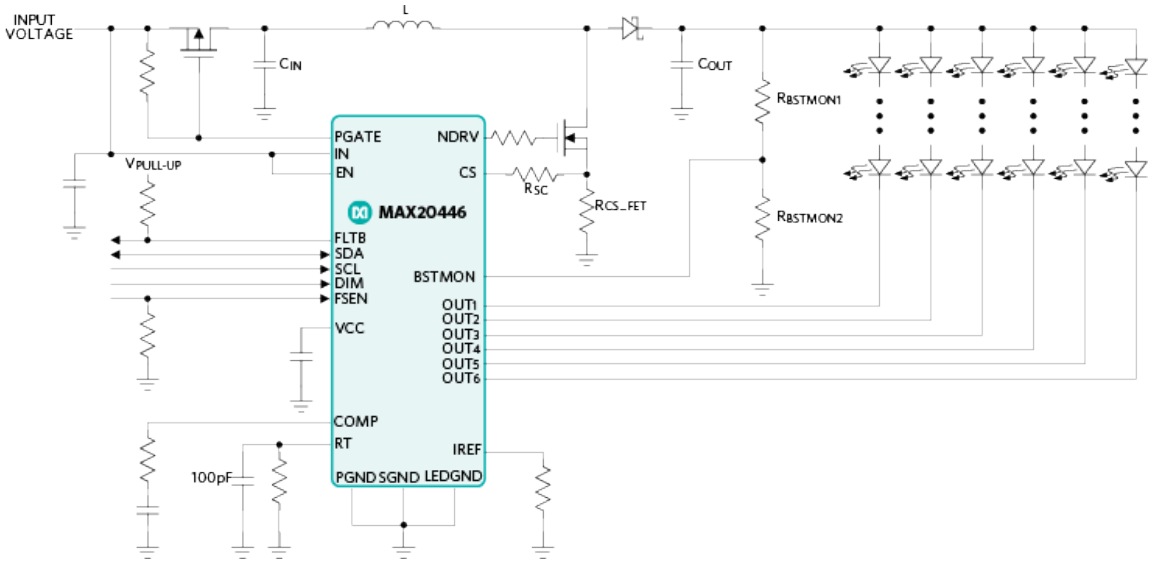

Figure 1. Typical MAX20446 operating circuit.

Inductor Selection

To select the right inductor value, calculate the required total output current (I_{LED}) to drive the LED using the following equation:

$$I_{LED} = I_{STRING} \times N_{STRING}$$

(Eq. 1)

where I_{STRING} is the current per string, and N_{STRING} is the number of strings used.

The maximum voltage (V_{LED_MAX}) to drive the LED strings is given by the following equation:

$$V_{LED\_MAX} = V_{F\_MAX} \times N_{LED} + V_{OUT\_MAX}$$

(Eq. 2)

where V_{OUT_MAX} is the maximum OUT_ regulation voltage (1.1V from the MAX20446 data sheet's Electrical Characteristics), V_{F_MAX} is the maximum expected forward drop on each LED, and N_{LED} is the number of LEDs that form each string.

The maximum duty cycle (DMAX) is given by the following equation:

$$D_{MAX} = \frac{V_{LED\_MAX} + V_D - V_{IN\_MIN}}{V_{LED\_MAX} + V_D - V_{CS} - V_{FET}}$$

(Eq. 3)

where V_{LED_MAX} is the forward voltage of the LED string in volts, V_D is the forward drop of the rectifying diode (approximately 0.6V), V_{IN_MIN} is the minimum input-supply voltage in volts, V_{CS} is the peak current sense voltage in volts (90% of the available limit should be considered), and V_{FET} is the average drain-to-source voltage of the switching MOSFET in volts when it is on

(assume 0.1V initially).

The maximum duty cycle and LED current determine the average inductor current (IL_{AVG}), which is expressed by the following equation:

$$IL_{AVG} = \frac{I_{LED}}{(1 - D_{MAX})}$$

(Eq. 4)

Knowing the average inductor current, the peak inductor current (IL_P) is expressed as follows:

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

(Eq. 5)

where ΔI_L is the peak-to-peak inductor current ripple in amperes. A lower ripple current requires a larger (and typically more expensive) inductor. A higher ripple current not only leads to higher switching losses but also requires more slope compensation and increased input capacitance. If the maximum peak-to-peak ripple is the recommended ±30% of the average inductor current, ΔI_L is given by the following equation:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

(Eq. 6)

From Equation 4, the average inductor current is proportional to the output current, and because the inductor ripple current, ΔI_L, is independent of output load current, the minimum and the maximum values of the inductor current track the average inductor current exactly. Based on this, Equation 5 can be rewritten as follows:

$$IL_P = IL_{AVG} + IL_{AVG} \times 0.3 = IL_{AVG} \times 1.3$$

(Eq. 7)

Finally, the minimum inductance value (L_{MIN}) in Henrys is expressed by the following equation:

$$L_{MIN} = \frac{(V_{IN\_MIN} - V_{FET} - V_{CS}) \times D_{MAX}}{f_{SW} \times \Delta I_L \times (1 - L_{TOL})}$$

(Eq. 8)

where f_{SW} is the desired switching frequency in hertz and L_{TOL} is the tolerance parameter applied on the inductance's nominal value.

As an example, if f_{SW} = 2.2MHz, L_{TOL} = 30% and V_{CS} = 0.378V, the values are calculated as follows:

$$I_{LED} = 6 \times 0.1A = 0.6A$$

(Eq. 9)

$$V_{LED\_MAX} = 3.3V \times 7 + 1.1V = 24.2V$$

(Eq. 10)

$$D_{MAX} = \frac{24.2V + 0.6V - 5V}{24.2V + 0.6V - 0.378V - 0.1V} = \frac{19.8V}{24.322V} = 0.81$$

(Eq. 11)

$$IL_{AVG} = \frac{0.6A}{1 - 0.81} = 3.158A$$

(Eq. 12)

$$IL_P = 3.158A \times 1.3 = 4.1A$$

(Eq. 13)

$$\Delta I_L = 3.158A \times 0.3 \times 2 = 1.895A$$

(Eq. 14)

$$L_{MIN} = \frac{(5V - 0.378V - 0.1V) \times 0.81}{2.2{\times}10^6 Hz \times 1.895A \times 0.7} = \frac{3.663V}{2.918{\times}10^6 A/s} = 1.255\mu H$$

(Eq. 15)

When the minimum inductor value is determined, a real inductor value must be chosen that is as close as possible to L_{MIN} without going under. Recalculate the peak inductor current and ripple using the chosen inductor value. These numbers are necessary for additional calculations going forward.

$$L_{ACTUAL} = 4.7\mu H$$

(Eq. 16)

$$\Delta I_L = \frac{(5V - 0.378V - 0.1V) \times 0.81}{2.2{\times}10^6 Hz \times 4.7{\times}10^{-6} H \times 0.7} = \frac{3.663V}{7.238H/s} = 0.506A$$

(Eq. 17)

$$IL_P = 3.158A + \frac{\Delta I_L}{2} = 3.411A$$

(Eq. 18)

Ensure that the chosen inductor has a current rating higher than IL_P. Typically, 20% headroom is used for the inductor peak current.

Input Capacitor Selection

In a boost converter, the input current is continuous, so the input capacitor's RMS ripple current is low. Both bulk capacitance and ESR contribute to the input ripple. Assume equal ripple contributions from bulk capacitance and ESR if aluminum electrolytic and ceramic capacitors are both used in parallel. If only ceramic capacitors are used, most of the input ripple comes from the bulk capacitance (since ceramic capacitors have very low ESR). Use Equation 19 and Equation 20 to calculate the minimum input bulk capacitance and maximum ESR.

$$C_{IN\_MIN} = \frac{\Delta I_L \times D_{MAX}}{4 \times f_{SW} \times \Delta V_{Q\_IN}}$$

(Eq. 19)

$$ESR_{CIN\_MAX} = \frac{\Delta V_{ESR\_IN}}{\Delta I_L}$$

(Eq. 20)

where ΔV_{Q_IN} and ΔV_{ESR_IN} are the input voltage ripple contributions due to capacitor discharge and ESR respectively.

Assume that a maximum input ripple of 50mV can be tolerated (1% of V_{IN_MIN}) where 95% of this input ripple comes from the bulk capacitance, and calculate the input capacitor as follows:

$$C_{IN\_MIN} = \frac{0.506A \times 0.81}{4 \times 0.0475V \times 2.2{\times}10^6 Hz} = \frac{0.41A}{0.418 \times 10^6 V/s} = 0.98\mu F$$

(Eq. 21)

$$ESR_{CIN\_MAX} = \frac{0.0025V}{0.506A} = 4.94m\Omega$$

(Eq. 22)

Considering a 20% tolerance on the capacitor's nominal value, use a 4.7µF capacitor to achieve the 0.98µF minimum bulk capacitance. Ensure that the chosen capacitors meet the minimum bulk capacitance requirement at the operating DC voltage (capacitance can decrease substantially with a change in voltage in ceramic capacitors).

The dielectric material should be X7R or better. Otherwise, the capacitor can lose much of its capacitance due to DC bias or temperature. The total capacitance value can also be increased if the input voltage is noisy or to meet electromagnetic interference (EMI) requirements.

Output Capacitor Selection

In the boost converter topology, the output capacitor supplies the load current when the switching MOSFET is on. The function of the output capacitor is to reduce the converter output ripple to acceptable levels. The entire output-voltage ripple appears across the constant-current sink outputs because the LED-string voltages are stable due to the constant current.

The ESR, ESL, and the bulk capacitance of the output capacitors contribute to the total output voltage ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and ESL effects. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To attenuate audible noise during PWM dimming, the number of ceramic capacitors on the output is usually minimized.

In this case, an additional electrolytic or aluminum organic polymer capacitor provides most of the bulk capacitance. Alternatively, low acoustic noise ceramic capacitors can be used.

Determine the minimum bulk capacitance at the boost output by using the following equation:

$$C_{OUT\_MIN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta V_{Q\_OUT}}$$

(Eq. 23)

where ΔV_{Q_OUT} is the output voltage ripple contribution due to capacitor discharge.

An additional output voltage ripple contribution (ΔV_{ESR_OUT}) comes from the output capacitor ESR, which is given by the following equation:

$$ESR_{COUT\_MAX} = \frac{\Delta V_{ESR\_OUT}}{IL_P}$$

(Eq. 24)

Limit the peak-to-peak output voltage ripple to 50mV to get a stable output current. Assume that the bulk capacitance is responsible for 95% of the ripple contribution, and calculate the following values using Equation 23 and Equation 24.

$$C_{OUT\_MIN} = \frac{0.6A \times 0.81}{2.2{\times}10^6 Hz \times 0.0475V} = \frac{0.486A}{0.1045 \times 10^6 V/s} = 4.65\mu F$$

(Eq. 25)

$$ESR_{COUT\_MAX} = \frac{0.0025V}{3.411A} = 0.73m\Omega$$

(Eq. 26)

Use three 4.7µF ceramic capacitors in parallel to exceed the minimum output capacitance of 4.65µF because the chosen capacitors must meet the minimum bulk capacitance requirement at the operating voltage.

Overvoltage Protection

If any LED string is open, the DC-DC converter output voltage increases to achieve the desired LED current. The overvoltage-protection threshold limits the output voltage through a voltage-divider network connected between the converter output, the BSTMON input, and GND. If the BSTMON voltage exceeds 1.23V, NDRV is forced low, which turns off the switching MOSFET and prevents the boost output voltage from increasing.

The overvoltage-protection threshold at the DC-DC converter output is determined using the following equation:

$$V_{BSTMON} = 1.23V \times \left(1 + \frac{R_{BSTMON1}}{R_{BSTMON2}}\right)$$

(Eq. 27)

where 1.23V (typ) is the overvoltage threshold on BSTMON.

V_{BSTMON} is the maximum voltage the boost converter can produce and should be greater than the maximum expected LED string voltage (V_{LED_MAX}) according to the following inequality:

$$V_{BSTMON} > 1.1 \times V_{LED\_MAX}$$

(Eq. 28)

where the factor 1.1 takes into account a 10% margin.

The minimum expected LED string voltage (V_{LED_MIN}) is expressed by the following equation:

$$V_{LED\_MIN} = V_{F\_MIN} \times N_{LED} + V_{OUT\_MIN}$$

(Eq. 29)

where V_{OUT_MIN} = 0.7V.

If undervoltage occurs during startup, the boost converter latches off. To avoid the boost converter from latching off, the voltage on the BSTMON pin must always be greater than 0.6V. This results in the following relation between V_{BSTMON} and V_{LED_MIN}:

$$0.6 \times \left(1 + \frac{R_{BSTMON1}}{R_{BSTMON2}}\right) \cong \frac{V_{BSTMON}}{2} < V_{LED\_MIN}$$

(Eq. 30)

The inequalities from Equation 28 and Equation 30 can be combined to yield the following:

$$1.1 \times V_{LED\_MAX} < V_{BSTMON} < 2 \times V_{LED\_MIN}$$

(Eq. 31)

Select values for $R_{BSTMON1}$ and $R_{BSTMON2}$ so that the output voltage does not exceed its absolute maximum rating (52V) while respecting Eq. 31. By selecting $RR_{BSTMON1}$ = 226kΩ and $R_{BSTMON2}$ = 10kΩ, the following value for VBSTMON is obtained:

$$V_{BSTMON} = 1.23V \times 23.6 = 29V$$

(Eq. 32)

Slope Compensation and Current-Sense Resistors Selection

The MAX20446 is a current-mode-controlled LED driver, which means that information about the inductor current is fed back into the loop.

At duty cycles greater than 50% and with continuous (i.e., always greater than zero) inductor current, a load transient can cause subharmonic oscillation and loop instability without slope compensation. To keep the loop stable, a resistor (R_{SC}) must be added from CS to the source of the switching MOSFET. Internal to the MAX20446, there is a current source that feeds a small ramped current through R_{SC} to create a voltage on the slope-compensation resistor (V_{SC}). This voltage is added to the voltage across the FET current-sense resistor, R_{CS_FET}, and the result is compared to a reference voltage, namely the voltage on the COMP pin.

Because R_{CS_FET} has both the switching MOSFET current and the slope compensation current flowing through it, the total voltage on the CS pin is expressed by the following equation:

$$V_{CS} = V_{SC} + V_{CS\_FET}$$

(Eq. 33)

The slope compensation voltage is defined as follows:

$$\frac{dV_{SC}}{dt} = R_{SC} \times 50\mu A \times f_{SW}$$

(Eq. 34)

To maintain stability, the minimum amount of slope-compensation voltage rate needed is expressed by the following equation:

$$\frac{dV_{SC}}{dt}_{MIN} = \frac{(I_{L\_downslope} - I_{L\_upslope}) \times R_{CS\_FET}}{2}$$

(Eq. 35)

where $I_{L\_UPSLOPE}$ and $I_{L\_DOWNSLOPE}$ are expressed as follows:

$$I_{L\_upslope} = \frac{V_{IN\_MIN}}{L_{MIN}}$$

(Eq. 34)

$$I_{L\_downslope} = \frac{V_{LED\_MAX} - V_{IN\_MIN}}{L_{MIN}}$$

(Eq. 36)

Therefore, V_{SC_MIN} and R_{SC_MIN} are defined by the following equations:

$$V_{SC\_MIN} = \frac{(V_{LED\_MAX} - 2 \times V_{IN\_MIN}) \times R_{CS\_FET} \times 1.5}{2 \times L_{MIN} \times f_{SW}} = \frac{(V_{LED\_MAX} - 2 \times V_{IN\_MIN}) \times R_{CS\_FET} \times 3}{4 \times L_{MIN} \times f_{SW}}$$

(Eq. 37)

$$R_{SC\_MIN} = \frac{(V_{LED\_MAX} - 2 \times V_{IN\_MIN}) \times R_{CS\_FET} \times 3}{4 \times L_{MIN} \times 50\mu A \times f_{SW}}$$

(Eq. 38)

This includes a 1.5 factor to provide adequate margin.

Recalling Equation 33, the minimum value of the R_{CS_FET} resistor is obtained by solving the following equation:

$$0.39V \times 0.9 = \frac{(V_{LED\_MAX} - 2 \times V_{IN\_MIN}) \times R_{CS\_FET} \times 3}{4 \times L_{MIN} \times f_{SW}} + IL_P \times R_{CS\_FET}$$

(Eq. 39)

where 0.39V is the minimum value of the peak current-sense threshold voltage. The current-sense threshold also includes the slope-compensation component. The minimum current-sense threshold of 0.39V is multiplied by 0.9 to take tolerances into account.

R_{CS_FET} is then expressed by the following equation:

$$R_{CS\_FET} = \frac{1.404V \times L_{MIN} \times f_{SW}}{3 \times (V_{LED\_MAX} - 2 \times V_{IN\_MIN}) + 4 \times L_{MIN} \times f_{SW} \times IL_P}$$

(Eq. 40)

Based on the stated design specifications, the values of R_{CS_FET} and R_{SC} are calculated as follows:

$$R_{CS\_FET} = \frac{1.404V \times 4.7{\times}10^{-6}H \times 2.2{\times}10^{6}Hz}{3 \times (24.2V - 10V) + 4 \times 4.7{\times}10^{-6}H \times 2.2{\times}10^{6}Hz \times 3.411A} = \frac{14.517V{\times}\Omega}{183.68V} = 79m\Omega$$

(Eq. 41)

$$R_{SC} = \frac{14.2V \times 0.075\Omega \times 3}{4 \times 4.7{\times}10^{-6}H \times 50{\times}10^{-6}A \times 2.2{\times}10^{6}Hz} = \frac{3.195V{\times}\Omega}{2068{\times}10^{-6}V} \cong 1.6k\Omega$$

(Eq. 42)

R_{CS_FET} = 75mΩ is selected, which is the closest lower-value standard resistor.
R_{SC} = 2.7kΩ is selected for this application.

Switching MOSFET Selection

The external switching MOSFET's voltage rating should be sufficient to withstand the sum of the maximum output voltage and the rectifier diode forward drop as stated in the following equation:

$$V_{DS\_FET\_ABS\_MAX} \geq (V_{LED_{MAX}} + V_D) \times 1.3$$

(Eq. 43)

The switching MOSFET should also be rated to handle the maximum RMS current:

$$I_{DRMS} \geq 1.3 \times \sqrt{IL_{AVG}^2 \times D_{MAX}}$$

(Eq. 44)

where I_{DRMS} is the switching MOSFET's drain RMS current in amperes, and the factor 1.3 is included to consider a 30% margin.

For this example application, the required $V_{DS\_FET\_ABS\_MAX}$ and I_{DRMS} are calculated as follows:

$$V_{DS\ FET\ ABS\ MAX} \geq (24.2V + 0.6V) \times 1.3 = 32.24V$$

(Eq. 45)

$$I_{DRMS} \geq 1.3 \times \sqrt{9.973A^2 \times 0.81} = 3.695A$$

(Eq. 46)

The MOSFET's on resistance (R_{DSON}) is related to the current rating and affects the boost converter's efficiency because it determines the resistive power loss of the device. The higher it is, the lower the overall efficiency of the converter is. Calculate the resistive power loss by using the following equation:

$$P_{LOSS\_RDSON} = IL_{AVG}^2 \times R_{DSON\_MAX} \times D_{MAX}$$

(Eq. 47)

Given the total output power (P_{OUT}) and an estimated overall LED driver's efficiency (η) of 90%, the P_{LOSS_TOT} value can be obtained as follows:

$$P_{OUT} = V_{LED\_MAX} \times I_{LED} = 24.2V \times 0.6A = 14.52W$$

(Eq. 48)

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS\_TOT}} = 0.9$$

(Eq. 49)

$$P_{LOSS\_TOT} = P_{OUT} \times \frac{0.1}{0.9} = 14.52W \times \frac{0.1}{0.9} \cong 1.613W$$

(Eq. 50)

The R_{DSON_MAX} value, which limits the P_{LOSS_RDSON} impact on overall efficiency to 1%, can be determined by using the following equation:

$$\frac{P_{OUT}}{P_{OUT} + P_{LOSS\_TOT} - P_{LOSS\_RDSON}} \leq 0.91$$

(Eq. 51)

$$P_{LOSS\_RDSON} \leq 176mW \Rightarrow R_{DSON\_MAX} \leq 21m\Omega$$

(Eq. 52)

Another consideration concerns the gate charge because the gate driver must provide that charge to turn the MOSFET on and off. A smaller charge is better, and the switching speed is also important, but it does not show significant variations between MOSFETs of similar current, on resistance, and voltage ratings.

The ON Semiconductor® NVTFS5C471NL N-channel MOSFET's characteristics are suitable for this application.

Rectifier Diode Selection

The rectifier diode can be a major contributor to overall power loss. Choose a Schottky diode with low forward-voltage drop that is rated to handle the average LED current. Use the following equation to determine the required current rating for the rectifier diode:

$$I_D \geq IL_{AVG} \times (1 - D_{MAX}) \times 1.2$$

(Eq. 53)

where the factor of 1.2 is included for margin.

With the previously calculated values of IL_{AVG} = 3.158A and D_{MAX} = 0.81, the rectifier diode is required to handle a forward current of 0.72A, as shown in Equation 54.

$$I_D \geq 3.158A \times (1 - 0.81) \times 1.2 = 0.72A$$

(Eq. 54)

Also ensure that the Schottky diode has a reverse voltage rating 20% higher than

V_{LED_MAX}, the maximum expected reverse voltage across the diode.

The most evident limitations of Schottky diodes are their relatively low reverse voltage ratings and their relatively high reverse leakage current. For silicon-metal Schottky diodes, the reverse voltage is typically 50V or less. Reverse leakage current increases with temperature, which leads to a thermal instability issue that often limits the useful reverse voltage to well below the actual rating.

The ON Semiconductor NRVBS260T3G Schottky diode is selected based on the calculated results.

Error Amplifier Compensation

Figure 2 shows the generic open loop configuration of a current-mode boost converter operating with continuous inductor current.

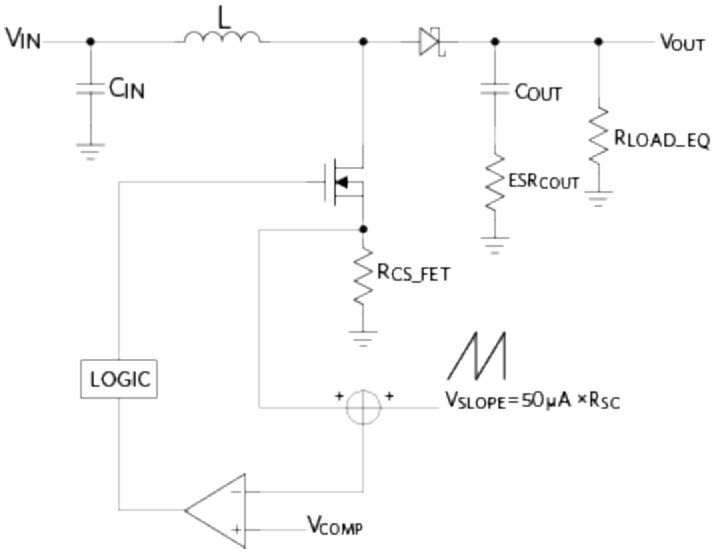

Figure 2. Generic current-mode boost converter open loop configuration.

In the MAX20446 LED driver, R_{LOAD_EQ} is replaced by

$$\frac{V_{LED\_MAX}}{I_{LED}}$$

.The transfer function, A(s), is given by the following equation:

$$A(s) = \frac{V_{LED\_MAX} \times (1-D)}{2 \times I_{LED} \times R_{CS\_FET}} \times \frac{\left(1+\frac{s}{f_{z1}}\right)}{\left(1+\frac{s}{f_{p1}}\right)} \times \frac{\left(1-\frac{s}{f_{ZRHP}}\right)}{1+\frac{s\left[\left(1+\frac{S_a}{S_n}\right)\times(1-D)-\frac{1}{2}\right]}{f_{SW}}+\frac{s^2}{(\pi \times f_{SW})^2}} \quad \text{(Eq. 55)}$$

where the artificial compensation ramp slope (S_A), the inductor on-slope (S_N), f_{Z1}, f_{RHPZ}, and f are expressed in the following equations:

P1

$$S_a = (R_{SC} + R_{CS\_FET}) \times 50\mu A \times f_{SW}$$

$$S_n = \frac{V_{IN\_MIN}}{L} \times R_{CS\_FET}$$

$$f_{z1} = \frac{1}{2\pi \times ESR_{C_{OUT}} \times C_{OUT}}$$

$$f_{RHPZ} = \frac{V_{LED\_MAX} \times (1 - D_{MAX})^2}{2\pi \times I_{LED} \times L}$$

$$f_{p1} = \frac{I_{LED}}{\pi \times V_{LED\_MAX} \times C_{OUT}}$$

f_{RHPZ} is the worst-case frequency at which the right-half-plane (RHP) zero is located. The RHP zero differs from the traditional left-half-plane (LHP) zero. Instead of boosting the phase, the RHP zero lags the phase further down, which reduces the phase margin and causes the loop to be unstable.

If ceramic capacitors with almost zero ESR are used at the converter's output, f_{Z1} can be neglected because it shifts toward high frequencies and most likely falls out of the converter's bandwidth.

The dominant pole's f_{P1} frequency is twice a common pole frequency due to the effect of boosting. Loop compensation is guaranteed by a so-called Type II transconductance amplifier, which characterizes the closed-loop response ($B(_s)$). **Figure 3** shows the basic Type II transconductance amplifier circuit with external compensation components.

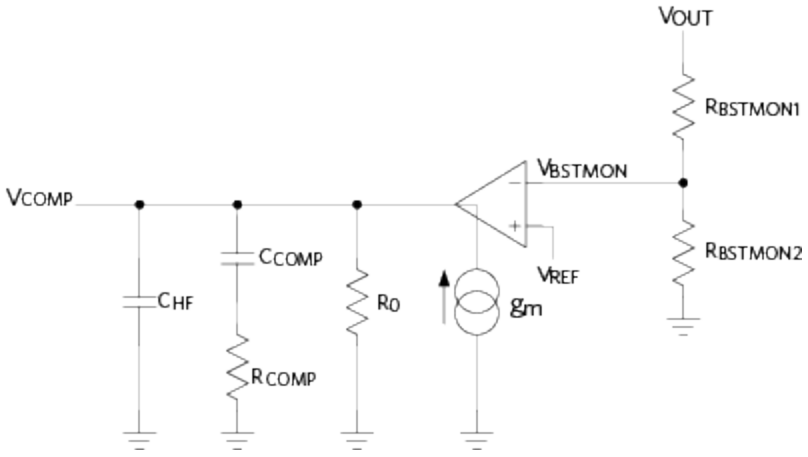

Figure 3. Type II transconductance amplifier for loop compensation.

Assuming R_0 >> R_{COMP} and C_{COMP} >> C_{HF}, the B(s) transfer function of Figure 3 can be written as follows:

$$B(s) \approx g_m \times R_{COMP} \times \frac{R_{BSTMON2}}{R_{BSTMON1} + R_{BSTMON2}} \times \frac{1}{sC_{COMP}R_{COMP}} \times \frac{\left(1 + \frac{s}{f_{zEA}}\right)}{\left(1 + \frac{s}{f_{pEA}}\right)} \quad \text{(Eq. 56)}$$

where A_{VM} is the mid-band voltage gain and g_M is the transconductance of the error amplifier. AVM is are expressed as follows:

$$A_{VM} = g_m \times R_{COMP} \times \frac{R_{BSTMON2}}{R_{BSTMON1} + R_{BSTMON2}}$$

f_{ZEA} and f_{PEA} are expressed as follows:

$$f_{zEA} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}}$$

$$f_{pEA} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}}$$

The closed loop response of the LED driver is A(s) × B(s)

The goal of loop compensation is to ensure that there is less than 180 degrees of phase shift for loop gains greater than 0dB (and an adequate phase margin). The error amplifier adds a zero-frequency pole due to the integrating effect of C_{COMP}, which allows rolling off the loop gain to 0dB with a -20dB/decade slope (after the dominant pole and well before the effects of the RHP zero).

It is recommended that the closed loop gain crossover frequency, f_C, is limited to at least one fifth of f_{RHPZ} to obtain an acceptable phase margin that is higher than 45 degrees. The compensation zero, f_{ZEA}, should be placed at least one fifth of the target crossover frequency, which is approximately 1/25 f_{RHPZ}.

To fix the total loop gain at f_{p1} so that the total loop gain crosses 0dB with -20dB/decade slope at 1/5 f_{RHPZ}, the optimum value of R_{COMP} is given by the following expression:

$$R_{COMP} = \frac{f_{RHPZ} \times R_{CS\_FET} \times I_{LED} \times \left(1 + \frac{R_{BSTMON1}}{R_{BSTMON2}}\right)}{5 \times f_{p1} \times g_m \times V_{LED\_MAX} \times (1 - D_{MAX})}$$

(Eq. 57)

The value of C_{COMP} can then be obtained from the definition of f_{ZEA}.

$$C_{COMP} = \frac{1}{2\pi \times R_{COMP} \times f_{zEA}} = \frac{25}{2\pi \times R_{COMP} \times f_{RHPZ}}$$

(Eq. 58)

The higher the frequency that the loop gain stays above zero before crossing 0dB, the faster the loop response is and, therefore, the lower the output voltage drops during a load step. Lowering R_{COMP} while keeping $f_{ZEA} \approx f_C/5$, increases the phase margin without significantly changing the gain and increases the time it takes for the output voltage to settle following a load step.

If the total output capacitance's ESR is significant, the output zero effect at f_{z1} is not negligible and can be counter-balanced by placing the error amplifier's main pole frequency, f_{PEA}, at f_{z1}. Consequently, the optional C_{HF} capacitor value is expressed as follows:

$$C_{HF} = \frac{1}{2\pi \times R_{COMP} \times f_{z1}} = \frac{ESR_{C_{OUT}} \times C_{OUT}}{R_{COMP}}$$

(Eq. 59)

The f_{PEA} pole might also be necessary to ensure that the gain continues to roll off after the crossover frequency.

Based on the previously calculated values for this design example, the values of f_{RHPZ}, f_{P1}, R_{LOAD_EQ}, R_{COMP}, and C_{COMP} are calculated as follows:

$$f_{RHPZ} = \frac{24.2V \times (1-0.81)^2}{2\pi \times 0.6A \times 4.7\times10^{-6}H} = \frac{0.873V}{17.71\times10^{-6}V \times s} = 49.295kHz$$

(Eq. 60)

$$f_{p1} = \frac{0.6A}{\pi \times 24.2V \times 14.1\times10^{-6}F} = \frac{0.6}{1071.43\times10^{-6}s} = 560Hz$$

(Eq. 61)

$$R_{LOAD\_EQ} = \frac{V_{LED\_MAX}}{I_{LED}} = \frac{24.2V}{0.6A} = 40.33\Omega$$

(Eq. 62)

$$R_{COMP} = \frac{49.295\times10^{3}Hz \times 75\times10^{-3}\Omega \times 0.6A \times 23.6}{5 \times 0.56 \times 10^{3}Hz \times 700 \times 10^{-6}S \times 24.2V \times (1-0.81)} = \frac{52.35\times10^{3}\Omega}{9.012} \cong 5.8k\Omega$$

(Eq. 63)

$$C_{COMP} = \frac{1}{2\pi \times 5800\Omega \times 1.972\times10^{3}Hz} \cong 14nF$$

(Eq. 64)

Select the standard commercial values of R_{COMP} = 4.7kΩ and C_{COMP} = 18nF for this numerical example to calculate F as follows:

ZEA

$$f_{zEA} = \frac{1}{2\pi \times 4700\Omega \times 18{\times}10^{-9}F} = \frac{1}{2.391 \times 10^{-4}s} = 1.882kHz$$

(Eq. 65)

Figure 4 and **Figure 5** illustrate the Bode plots of the LED driver closed loop response. A 0-dB crossing frequency (f_C) of 10kHz and a phase margin (PM) of 70 degrees are obtained.

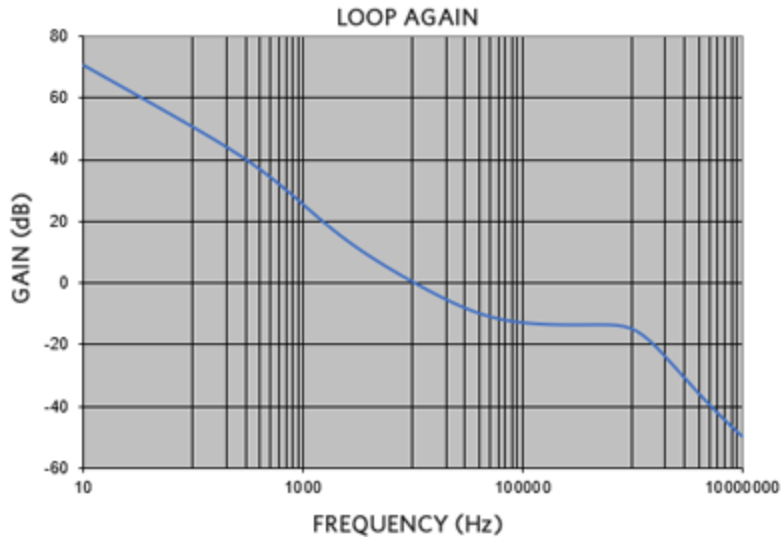

Figure 4. Loop gain.

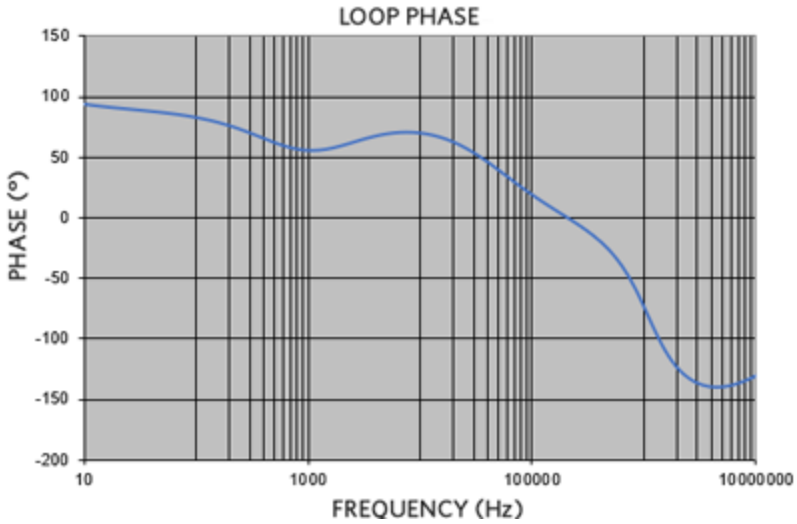

Figure 5. Loop phase.

Conclusion

Figure 6 shows the complete boost LED driver schematic with the selected component values from the design example. The step-by-step design process outlined in this application note can be used as a reference during the debug and test phase.

For additional details, refer to the MAX20446 data sheet and the MAX20446 Evaluation Kit data sheet.

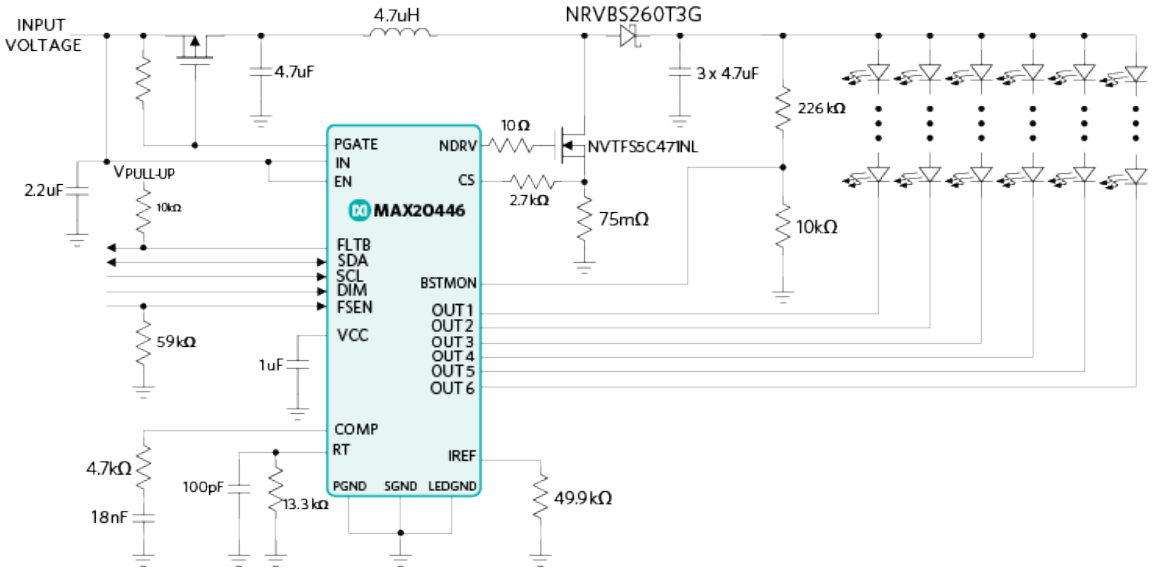

Figure 6. Typical MAX20446 operating circuit based on example calculations (optional P-MOS and relevant bias resistor not included).

Trademarks

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Related Parts		
MAX20446	Automotive 6-Channel Backlight Driver with Boost/SEPIC Controller and I^2C Interface	Samples

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