

GPS Data Converters to the Rescue for Electronics Surveillance and Warfare Systems!

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Spectral congestion, higher operating frequencies, and more complex waveforms continue to cause increased problems for electronic surveillance and warfare systems, with greater bandwidths to be surveyed and ever greater levels of detection sensitivity needed. With ever more functionality of these systems being implemented in the digital domain, both of these elements, in addition to cost, push directly on the performance limits of high speed analog-to-digital converters (ADCs), with the ADC often being the system limitation. However, the next high speed generation ADCs push to higher levels of performance and offer some system level solutions to these challenges.

The basic architecture of modern day surveillance systems, as shown in Figure 1, consists of three basic functions:

- RF/microwave tuner
- Digitizer—the ADC with associated amplifier and buffer
- Fast Fourier transform and digital signal processing

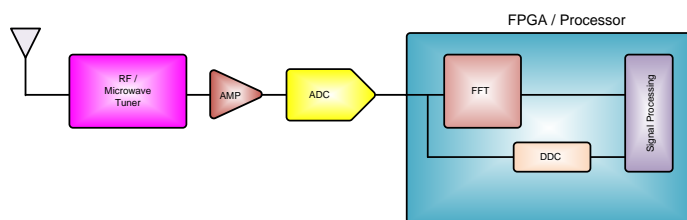


Figure 1. Basic Surveillance System Architecture

In many instances, when the system architect is often faced with a conundrum, the high speed ADC performance—the transition from the analog to the digital domain—is the limiting factor of the system. While minimizing cost and system size is always paramount, the system designer must focus on how to best balance the need to increase instantaneous surveillance bandwidth (to maximize the probability of intercept) and how to minimize the effects of in-band high power signals desensitizing the system.

The sampling rate and spurious-free dynamic range (SFDR) are generally the two key factors of the ADC that influence the decision of how to meet the system criteria and identified trade-offs. The sampling rate of the converter determines the Nyquist band, which in turn determines the maximum observable bandwidth of the individual converter while the SFDR determines the signal levels that are detectable. Although the noise spectral density may also need to be considered, in most cases the noise floor of the ADC is far below the spur level, and from the operational system perspective, spurs created from the digitization process are difficult to distinguish from low power signals in the spectrum that are being digitized. Hence the sensitivity of the system is directly related to the SFDR, to minimize the detection of false targets.

For example, consider digitizing two continuous waveform (CW) signals, with Signal A being a full-scale input and Signal B a signal of much lower power—Signal B may be difficult to distinguish as being a signal of interest compared to a spur, as the spurs generated through digitizing Signal A can be at similar levels. Thus, Signal B would be below the detection level of the system and would not be flagged as a signal of interest.

Limitations such as these make it clear that the best detection levels can be achieved with ADCs with very high linearity. However, higher linearity historically has been at the expense of the ADC sample rate, meaning high linearity GPS converters have not been available. For the purposes of this discussion, a general electronic surveillance system will be considered, but similar system architectural trade-offs apply to electronic intelligence (ELINT), signals intelligence (SIGINT), and communications intelligence (COMINT). Three different system architectures (shown in Figure 2) are often considered for these systems.

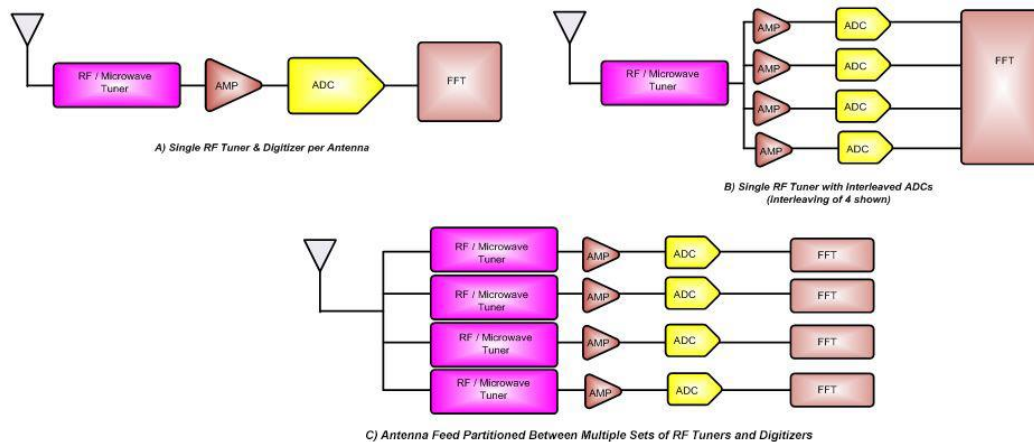


Figure 2. Architecture Options for Surveillance Systems

Figure 2A illustrates the simplest system. Using a highly linear ADC such as the Analog Devices [AD9265](#)—which has an SFDR of 93 dBc and a signal-to-noise ratio (SNR) of 79 dBFS at 70 MHz IF—this architecture provides excellent sensitivity and detection, but with a max sample rate of 125 MSPS. This is at the expense of instantaneous BW, which is limited to 62.5 MHz before antialiasing filters are considered, typically reducing the maximum BW to 40 MHz or lower. With only a single converter in the system, the system cost is low but the RF tuner is forced to sweep the entire RF bandwidth in steps of 40 MHz, reducing the probability of intercept of certain signals.

An obvious way to increase the BW is to interleave multiple high linearity, lower sampling rate converters, connected to a single wideband RF tuner (Figure 2B), increasing the effective sample rate and instantaneous bandwidth. For example, if eight AD9265 ADCs are interleaved, this will provide an aggregate effective sampling rate of 1 GSPS supporting an instantaneous bandwidth of almost 500 MHz. As the RF tuner only needs to sweep in steps of 500 MHz, the RF spectrum can be surveyed much faster, increasing the probability of intercept of signals of interest—particularly of agile signals—and the system relies on a single RF tuner, limiting the cost increase compared to Figure 2A.

While this does impose some further challenges for the RF tuner (a wider bandwidth provides challenges for maintaining similar IP3 and noise performance as the previous architecture), the main drawbacks of this approach can be with the challenges of interleaving ADCs. Mismatches between converters in terms of gain, dc offset, and phase need to either be calibrated out of the system or managed using digital signal processing, but even so, there will typically be some degradation in terms of SFDR, noise floor, or possibly bandwidth that will reduce the

performance of this architecture. The susceptibility of desensitization to a very high power signal within the surveillance band further exacerbates this problem. Such a signal anywhere within the 500 MHz band requires that the RF and IF gain is reduced, limiting the probability of intercept of lower power signals.

The highest performance architecture, though, is that shown in Figure 2C. Multiple parallel RF and digitizer subsystems are implemented, and if the AD9265 is again considered, multiple adjacent 40 MHz bands are observed instantaneously. By offsetting each subsystem by almost 40 MHz (some overlap is required) the instantaneous BW can be increased, but clearly this is at the expense of system cost, as the cost of the system is scaled directly with instantaneous bandwidth. Compared to an interleaved approach, the architecture has the benefit of not needing calibration or digital signal processing to remove spurs created by interleaving. Additionally, the system is more resistant to high power blocking or jamming, as the RF/IF gain for each 40 MHz band can be set independently.

The system architectures above are currently employed in a range of systems to date, but as shown, each has its limitations in performance, cost, and potentially size. However, the status quo may soon be challenged by new gigasample per second ADCs that offer higher linearity and embedded digital signal processing features. New ADCs, such as the [AD9625](#) and [AD9680](#) offer sampling rates in between 1.25 GSPS and 2.5 GSPS, with SFDRs as high as 85 dBc. Table 1 provides an overview of the performance of the AD9265 as well as typical current and new ADI gigasample ADCs.

Table 1. Overview of High Linearity Lower Speed ADCs Compared to Past and Present GSPS ADCs

	Analog Devices AD9265 (125 MSPS)	Typical Previous Generations >2 GSPS ADC	Analog Devices AD9680 (1.0 GSPS)	Analog Devices AD9625 (2.5 GSPS)
Sample Rate (MSPS)	125	>2000	1000	2500
Analog BW (MHz)	650	>3000	2000	3000
SFDR (dBc)	93	58	85	79
SNR (dBFS)	79	50	65.3	58.3
ENOB (bits)	12.8	8.0	10.8	9.2
IMD3 (dBc)	95	64	81	81.2

The linearity of a gigasample per second ADC will not match that of a lower sampling rate device, but it can be seen that the gap is certainly narrowing. Using a single gigasample ADC enables the architecture of Figure 2B to be implemented, but without the drawbacks of interleaving. Furthermore, the higher linearity of the device increases the detection sensitivity and minimizes the susceptibility to jamming and blocking, closing the performance gap between this and the system shown in Figure 2C, but with reduced cost and size.

However, while this aspect certainly opens up new options to the system architect, the more exciting aspect of these new devices is that they are also able to implement digital signal processing within the converter, immediately after the conversion to digital. 65 nm CMOS processes enable higher speed digital signal processing to be implemented within the converter. For example, digital downconversion (DDC) functionality is implemented in both the AD9625 and AD9680 to enable the high speed ADC to dynamically change from providing full bandwidth to a selectable frequency subband within the digitized Nyquist band of >1000 MHz. Consider the architecture shown in Figure 3, which illustrates the AD9625 2.5 GSPS, 12-bit ADC with embedded DSP options.

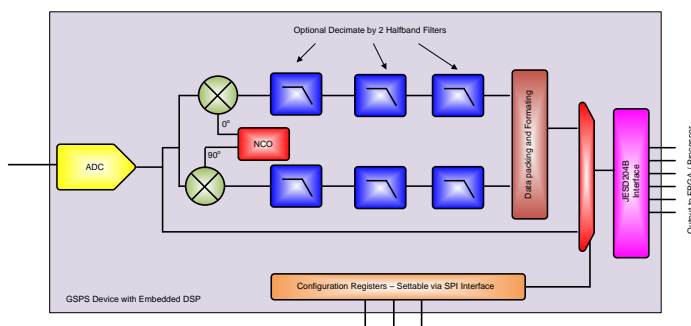


Figure 3. 2.5 GSPS ADC with Optional and Bypassable Embedded Digital Downconverters

In a wideband mode, the ADC will support surveillance of the RF spectrum in 1 GHz steps, enabling a rapid evaluation of the RF landscape. Once signals of interest are identified it is feasible to direct this data through the DDC. The DDC, using a digital numerically controlled oscillator (NCO) and filtering stages can select a band from anywhere within the Nyquist band of the converter and employ digital decimation by factors of 8 and 16, suppressing the noise floor further. Although this functionality could easily be employed in the digital signal processing stages in devices after the converter, performing this in the ADC itself helps reduce the output data rate of the ADC, and more importantly, the power dissipated in the transmission, significantly reducing the system power when the DDC is utilized.

With the continued emphasis on reducing size, weight, and power (SWaP) in aerospace and defense systems, new options for the system architect begin to open up as high speed converters continue to see improved linearity in the GSPS region. With the inclusion of digital signal processing features within the high speed converter, a wide range of options and system optimizations begin to unfold making this an exciting period for next generation surveillance systems.

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