

Greatly Increase the Efficiency of the Regulated 48 V to 12 V First Stage

Alexandr Ikriannikov, Fellow, and Laszlo Lipcsei, Director, Product Applications

Abstract

48 V distribution is popular in data center and communication applications, with many different solutions for the step down from 48 V to the intermediate rail. The simplest approach could be a buck topology, which can provide a high performance but often falls short in power density. Upgrading the multiphase buck with coupled inductors enables a dramatic power density improvement that matches the state-of-the-art alternatives while keeping the massive performance advantage. The multiphase coupled inductors have inverse coupling between windings that enables current ripple cancellation in each phase current. This benefit can be traded either for efficiency or, for example, size reduction and improvement of the power density. This article illustrates an example with 4× reduction in magnetics volume and weight, allowing an industry standard size of 1/8 of the brick for a 1.2 kW solution with peak efficiency above 98%. This article also focuses on how to optimize the 48 V topology based on the figure of merit (FOM) of the coupled inductors. It will be of interest to engineers focusing on the DC-to-DC conversion area.

Introduction

The 48 V distribution rail is typically stepped down to some intermediate voltage, often 12 V or lower, and then the different local point-of-load regulators deliver a variety of different voltages directly to different loads. One of the first choices to consider for the step-down voltage regulator 48 V to 12 V is a multiphase buck converter (Figure 1). This is a solution with regulated V_0 and fast transient, which is simple and inexpensive to implement. For a power range of a few hundred watts to >1 kW, four parallel phases can be considered. However, as high efficiency is often a priority: switching frequency is often relatively low for the 48 V kind of converters to keep the switching losses down, as compared to the lower voltage applications with 12 V or even 5 V input. This hurts magnetics twice in terms of volt × seconds, as the already noticeable voltage is also applied for a relatively longer time. As a result, magnetics for 48 V are typically bulky, with multiturn windings to withstand the significantly increased volt × seconds as compared to lower voltage applications. High efficiency can still be achieved in 48 V buck converter, but typically with a significant overall size, where inductors occupy most of the volume.

The basic 48 V to 12 V ~1 kW buck converter has four phases with discrete inductors 6.8 μ H and switches at 200 kHz. These four inductors are by far the biggest and tallest components, representing a majority of the solution volume. The objective of the article is to keep or improve the achieved high efficiency of this initial design but reduce the size of the magnetics significantly.

The current ripple in each phase of the conventional buck can be found as Equation 1, where the duty cycle is $D = V_0/V_{IN}$, V_0 is the output voltage, V_{IN} is the input voltage, L is inductance value, and Fs is the switching frequency.



Figure 1. Four-phase buck converter with discrete inductors.

Replacing the discrete inductors (DL) with the coupled inductor¹⁻⁷ that has a leakage inductance L_k and the mutual inductance L_m, the current ripple in CL (coupled inductor) can be shown as Equation 2.⁶ The FOM is expressed as Equation 3, where N_{ph} is the number of coupled phases, ρ is a coupling coefficient (Equation 4), and j is a running index, which just defines an applicable interval of the duty cycle (Equation 5).

$$dIL_{CL} = \frac{V_{IN} - V_O}{L_k} \times \frac{D}{F_S} \times \frac{1}{FOM(D, N_{ph}, \rho, k)}$$
(2)

$$FOM = \frac{\left(1 + \frac{\rho}{\rho + 1} \times \frac{1}{N_{ph} - 1}\right)}{1 - \left[\frac{(N_{ph} - 2 \times j - 2) + \frac{j \times (j + 1)}{N_{ph} \times D} + \frac{\rho}{N_{ph} \times D + (N_{ph} - 2 \times j - 1) + j \times (j + 1)}{N_{ph} \times (1 - D)}\right] \times \frac{\frac{\rho}{\rho + 1}}{N_{ph} - 1} \qquad (3)$$

$$\rho = \frac{L_m}{L_k} \qquad (4)$$

$$j = floor \left(D \times Nph\right) \tag{5}$$

CL Considerations

The first step for the improvement would be to plot a FOM for the $N_{ph} = 4$, for several practically reasonable values of the coupling coefficient L_m/L_k (Figure 2). The red curve $L_m/L_k = 0$ represents FOM = 1 baseline for the discrete inductor. It was shown that the notch CL (NCL) structures with very low leakage can generally achieve very high L_m/L_k and therefore high values of FOM.^{8,9} However, while the duty cycle of interest is ideally right in the first notch D = 12 V/48 V=0.25: it is necessary to consider some range for the V_{IN} and also V_0 . Sometimes the nominal V_{IN} can be 48 V or 54 V plus some tolerance, V_0 can be adjusted away from 12 V, and so on. In order for the current ripple to remain contained if the duty cycle changes around D = 0.25 in some range, a typical CL design with significant leakage is chosen instead of NCL, still with a significant FOM value. Assuming $L_m/L_k > 4$, a benefit of ~6× could be considered from FOM in Figure 2 to decrease the inductance value in CL, compared to the DL baseline. Decreasing the energy storage should directly affect the required volume of the magnetics. Reducing DL = 6.8 µH value to CL = 1.1 µH should therefore be beneficial for the size reduction.



Figure 2. FOM for a 4-phase CL for some different L_m/L_k values as a function of the duty cycle D. The region of interest is highlighted.



Figure 3. Current ripple for DL = 6.8 μ H and CL = 4 × 1.1 μ H for V_M = 48 V and F_s = 200 kHz as a function of V_o. The region of interest is highlighted.

The corresponding current ripple is plotted in Figure 3, comparing baseline design DL = 6.8 μ H with proposed 4-phase CL = 4 × 1.1 μ H (L_m = 4.9 μ H) at V_{IN} = 4.8 V and F_s = 200 kHz conditions. In the region of interest, the current ripple of CL is similar to or smaller than that of DL. This implies that rms of all circuit waveforms is similar and so are the conduction losses. Same ripple at the same F_s also implies the same switching losses, gate drive losses, etc., which means that the efficiency between the two solutions should be very similar (assuming a similar contribution from DL and CL inductor losses, as the only difference).



Figure 4. Four DL = 6.8 μ H inductors (top) are replaced with CL = 4 × 1.1 μ H (bottom), achieving 4× volume reduction.



Figure 5. 48 V to 12 V regulated first stage. Components are placed on the top PCB side inside the 1/4-brick outline. Moving all ~1 mm components to the bottom: 1/8-brick.

Designed CL = 4 × 1.1 μ H is shown in Figure 4, replacing four DL = 6.8 μ H inductors.⁵ Each DL is 28 mm × 28 mm × 16 mm, assuming that they are spaced 0.5 mm from each other: 4-phase CL with 56.5 mm × 18 mm × 12.6 mm dimensions achieves 4× volume reduction for magnetics. A complete 1.2 kW 48 V to 12 V regulated solution is shown in Figure 5, components on a single PCB side are inside 1/4-brick outline. The CL dimensions and footprint are purposefully designed to fit two CL parts inside an industry standard quarter-brick size. Placing all ~1 mm components (FETs, controller ICs, ceramic capacitors, etc.) on the bottom side of the PCB enables 1/8-brick size for the 1.2 kW solution.

Performance Gain

When the DL = $6.8 \,\mu$ H inductors were changed to CL = $4 \times 1.1 \,\mu$ H—the current slew rate limit in the inductor also improved by $6\times$, which is always helpful for the transient improvement. On top of this, the inductor saturation rating improved by $\sim 2\times$ at 100°C, even though the total magnetics volume decreased by $4\times$.

The transient performance of the proposed $V_{IN} = 48$ V solution with the $V_0 = 12$ V output is illustrated in Figure 6. As expected, feedback regulates the output voltage to a preset value for the changing load current, also compensating for any changes in the input voltage.



Figure 6. Transient at the V_0 = 12 V output (CL = 4× 1.1 µH) for the 75 A load steps.

Probably the most important performance parameter, achieved efficiency is shown in Figure 7. It is compared to the state-of-the-art industry solution: 48 V to 12 V (fixed 4:1 step down) LLC with matrix transformer and GaN FETs on both primary and secondary sides.¹⁰ Compare the achieved full load efficiency of 97.6% and the benchmark of 96.3%. This implies that 16.6 W less losses are dissipated at full power, achieving 1.6× improvement in the proposed solution. Such loss reduction is typically very hard to achieve when the efficiency is already so high.

A trade-off between size and efficiency is certainly possible. Figure 8 compares the efficiency of the CL = 4 × 1.1 µH (4× reduction in magnetics size compared to DL) to a larger CL = 4 × 3 µH with only 2× reduction in inductor volume. The physically larger CL = 4 × 3 µH has a higher $L_k = 3$ µH value for leakage and a larger mutual inductance $L_m = 10$ µH. This allows a comfortable F_s reduction to 110 kHz, pushing the efficiency significantly higher in a whole load range.



Figure 7. Efficiency comparison of the state-of-the-art 48 V to 12 V solutions in 1/8-brick form factor.



Figure 8. Efficiency vs. size trade-off for the proposed 48 V to 12 V solution with coupled inductors.

Conclusion

Utilizing the coupled inductor benefits, the 48 V to 12 V solution reduces the total magnetics size by 4× from the base discrete inductors, achieving 1.2 kW in the industry standard 1/8 brick form factor. This 4× magnetics size reduction is achieved while preserving the excellent efficiency performance, increasing inductor current slew rate in transient by 6×, and increasing inductor I_{sat} rating by 2×.

Compared to the industry state-of-the-art 48 V to 12 V solution in the same form factor: \sim 1.6× loss reduction is achieved at full power. Efficiency is also shown to improve further if a smaller reduction in magnetics size is acceptable.

At the same time, the proposed solution is fully regulated, placed directly on the customer motherboard, and utilizes standard silicon FETs to optimize the cost further. This is compared to unregulated 4:1 LLC with all GaN FETs, manufactured as a separate module with a specialized PCB that has many layers, a sensitive layout, and an embedded matrix transformer.

The overall performance gain illustrates the advantages of ADI's patented IP on coupled inductors, which we are delighted to provide to our many customers with DC-to-DC applications.

References

- ¹ Aaron M. Schultz and Charles R. Sullivan. "Voltage Converter with Coupled Inductive Windings, and Associated Methods." U.S. Patent 6,362,986, March 2001.
- ² Jieli Li. "Coupled Inductor Design in DC-DC Converters." MS Thesis, 2001, Dartmouth College.
- ³ Pit-Leong Wong, Peng Xu, P. Yang, and F. C. Lee. "Performance Improvements of Interleaving VRMs with Coupling Inductors." *IEEE Transactions on Power Electronics*, Vol. 16, No. 4, July 2001.
- ⁴ Yan Dong. "Investigation of Multiphase Coupled-Inductor Buck Converters in Point-of-Load Applications." Ph.D. Thesis, 2009, Virginia Polytechnic Institute and State University, USA.
- ⁵ Alexandr Ikriannikov. "Coupled Inductor with Improved Leakage Inductance Control." U.S. Patent 8,102.233, January 2009.
- ⁶ Alexandr Ikriannikov and Di Yao. "Addressing Core Loss in Coupled Inductors." Electronic Design News, December 2016,
- ⁷ Alexandr Ikriannikov. "Coupled Inductor Basics and Benefits." Analog Devices, Inc., 2021.
- ⁸ Alexandr Ikriannikov. "Evolution and Comparison of Magnetics for the Multiphase DC-DC Applications." *IEEE Applied Power Electronics Conference*, March 2023.
- ⁹ Alexandr Ikriannikov and Di Yao. "Converters with Multiphase Magnetics: TLVR vs CL and the Novel Optimized Structure." PCIM Europe, May 2023.
- ¹⁰ "EPC9174-Evaluation Board." Efficient Power Conversion Corporation.

About the Authors

Alexandr Ikriannikov is a fellow for the Communications and Cloud Power Team at Analog Devices. He received his Ph.D. degree in electrical engineering from Caltech in 2000, where he studied power electronics from Dr. Cuk. His graduate school projects ranged from Power Factor Correction for AC-to-DC applications to 15 V to 400 V DC-to-DC for Mars rovers. After graduate school he joined Power Ten to redesign and optimize multi-KW AC-to-DC power supplies, then in 2001 joined Volterra Semiconductor concentrating on low voltage high current applications and coupled inductors. Volterra was acquired by Maxim Integrated in 2013, which is now part of Analog Devices. Currently, Alexandr is a senior member of IEEE. He holds more than 60 issued U.S. patents plus more pending and has authored multiple publications in the field of power electronics.

Laszlo Lipcsei is a director for the Communications and Cloud Power Team at Analog Devices. He received his M.S.E.E. degree in automation and computers from Bucharest Polytechnic University. In 2000, he joined 0₂Micro and focused on power conversion and battery management IC definition and development. In 2015, Laszlo joined Maxim Integrated AR&D team to lead the definition and system development of software-defined battery. His team also developed the wireless BMS proof of concept battery pack that was showcased at CES 2020. Since early 2020, he has been focusing on multiphase and 48 V power conversion architecture development. Laszlo holds over 50 patents with more pending.

Engage with the ADI technology experts in our online support community. Ask your tough design questions, browse FAQs, or join a conversation.

ADI EngineerZone

SUPPORT COMMUNITY

Visit ez.analog.com



For regional headquarters, sales, and distributors or to contact customer service and technical support, visit analog.com/contact.

Ask our ADI technology experts tough questions, browse FAQs, or join a conversation at the EngineerZone Online Support Community. Visit ez.analog.com.

©2023 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

TA24698-12/23(A)