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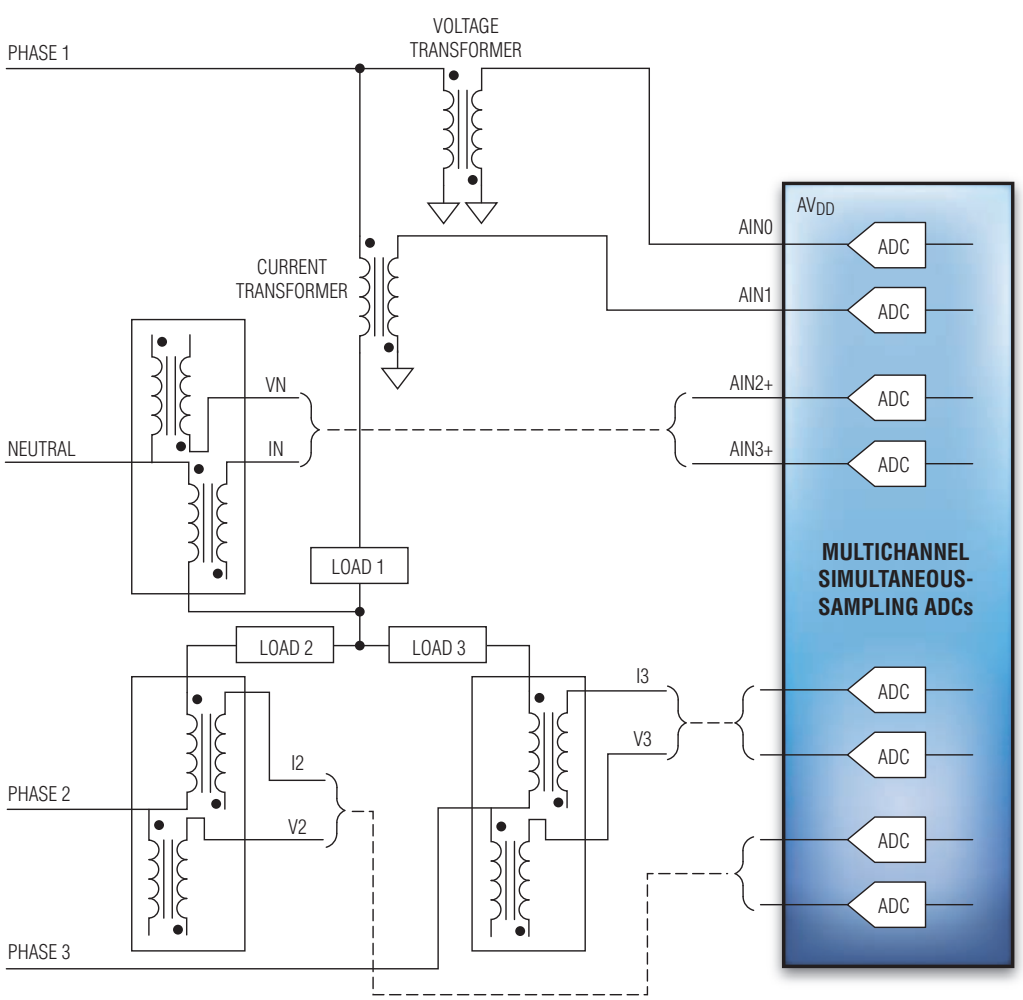

Typical power-grid monitoring application using simultaneous-sampling ADCs. (See article on page 3.)

Letter from the CEO

Weathering the Economic Storm

The last two years have been difficult for everyone. Corporate belt tightening, company closures, home mortgage foreclosures, and still other economic issues have garnered the headlines and been on everyone's mind. At the same time, developing new products and bringing them to market has never been more critical to ensure that your company has the best product for customers to purchase or to open new market opportunities.

Here at Maxim we see the same issues. We had to do our share of controlling costs, but we have done it very selectively so we don't impact your work. Thus, to the outside there has been very little visible change—our application staff is still readily accessible, samples of our products are just a phone call or web access away, and on-time delivery performance is better than ever.

One area inside Maxim that we barely touched during our belt-tightening was product research and development. We are maintaining our goal of releasing, on average, one new product every business day during 2009. Our forthcoming products will deliver even higher levels of circuit integration, lower power consumption, enhanced performance, and features that will help you design still greener and better performing systems that won't break the bank.

To ensure that you can get the help you need, when you need it, we also kept our applications engineering staff at close to full strength. We added new software that improves our internal communications. We want every technical question answered and no caller to be left without an answer. The reasoning is actually quite simple—it's our effort to make sure that you continue to develop your products on your schedule.

During the economic upheaval of the last 18 months we also revamped some of our manufacturing procedures so that all our products are available when you want them. Throughout our organization, we put a special focus on not becoming a bottleneck in your manufacturing flow. To do that, we added a fast-response capability—by keeping the right products in the manufacturing pipeline, we can deliver an uninterrupted flow to your production lines. On-time delivery performance is now over 95% and still improving.

As economic conditions improve, we will not stop our improvement process. We will continue to make additional investments to accelerate new product development. We will streamline our manufacturing to better deliver products that meet your needs and production deadlines.

Tunç Doluca
President and Chief Executive Officer

Reduce System Cost for Advanced Powerline Monitoring by Leveraging High-Performance, Simultaneous-Sampling ADCs

Martin Mason, Director, Precision ADCs
Maxim Integrated Products

Rising power demands and a focus on energy conservation are driving increased investment in the global power-delivery infrastructure. As a result, advanced powerline monitoring systems have become a critical element of the new "smart grids" for both single- and multiphase applications. With system performance requirements growing more stringent, designers are turning to simultaneous-sampling, multichannel, high-performance ADCs for their powerline monitoring or multichannel SCADA (supervisory control and data acquisition) systems.

Introduction

Advanced powerline monitoring systems combine power-supply monitoring, load balancing, protection, and metering functions in one system. This approach allows the power utilities to deliver, and the customers to consume, grid power more efficiently. Along with efficient delivery, the advanced powerline monitoring systems predict maintenance needs; detect and respond to fault conditions; record and allow for dynamic load balancing and energy conservation; monitor (and control) the quality of power delivery; and help protect equipment.

To implement these monitoring systems, ADCs (analog-to-digital converters) are needed to monitor the voltage and current on multiple phases. However, to meet the stringent requirements of the various standards and to measure and optimize power-factor losses, these converters must be synchronized to ensure that they sample the three phases (plus neutral) simultaneously. Synchronizing individual converters can be difficult, so vendors offer multiple simultaneous-sampling ADCs in a single package. If a more highly integrated solution is needed, another option is to integrate the simultaneous-sampling converters in a custom ASIC.

Performance Measurements—Local Standards and International Requirements

The development and widespread adoption of advanced powerline monitoring systems is complex due to varying international standards defining the precision of energy measurement. The measurement characteristics of the delivered energy must comply with local standards or international requirements. The EU (European Union) standards EN 50160, IEC 62053, and IEC 61850 dictate the minimum accuracy needed for a modern multichannel ADC system used in power-system monitoring and metering. Powerline monitoring is also impacted by the increasingly stringent accuracy requirements associated with real-time power-delivery monitoring, fault detection and protection, and dynamic load balancing. As an example, the EU standard IEC 62053 Class 0.2 (which is increasingly used as a common standard worldwide) requires meter precision to be 0.2% of nominal current and voltage. For power-factor accuracy measurement, phase matching should be 0.1% or better.

Not only is the minimum accuracy specified, but international and local standards also dictate the sample rate needed for a modern system used in powerline monitoring and metering. There is now a need for rigorous analysis of multiple high-order harmonics of the AC supply and for detection of high-speed fault conditions such as instantaneous spikes and brownouts. Consequently, these applications typically require accurate, simultaneous multichannel measurement over a wide dynamic range of up to 90dB with a sample rate of 16ksps or higher.

Many countries around the globe have adopted versions of the EU standards, so these standards serve as a good example of the measurement requirements which the system must meet. **Table 1** summarizes the EN 50160 requirements.

For the harmonic voltage, the EN 50160 mandates measurement up to the 25th-order harmonic of 50Hz/60Hz voltages. However, for various nonlinear loads, such as inductive motors and switching power-supply drives, measurements must be done for up to the 127th-order harmonic of 50Hz/60Hz voltage supply.

It is also important to note that emerging standards like IEC 61850 recommend the recording of power-system transient events with 256 samples per AC cycle or higher.

A Typical Power-Grid Monitoring Application

Standard throughout the world, 3-phase power is distributed using what is called a "wye connection." The term "wye" refers to three voltages that are offset in phase from each other by one-third of a cycle (120°). A fourth wire, or neutral line, is often used to accommodate unbalanced loads. If loads on each of the three phases

Table 1. EN 50160 Energy Specifications

Supply Voltage Phenomenon	Acceptable Limits	Measurement Interval	Monitor Period	Acceptance Percentage (%)
Grid Frequency	49.5Hz to 50.5Hz, 47Hz to 52Hz	10s	1 week	95, 100
Slow Voltage Changes	230V ±10%	10min	1 week	95
Voltage Sags or Dips (≤ 1min)	10 to 1000 times per year (under 85% of nominal)	10ms	1 year	100
Short Interruptions (≤ 3min)	10 to 100 times per year (under 1% of nominal)	10ms	1 year	100
Accidental, Long Interruptions (> 3min)	10 to 50 times per year (under 1% of nominal)	10ms	1 year	100
Temporary Overvoltage (Line-to-Ground)	Mostly < 1.5kV	10ms	–	100
Transient Overvoltages (Line-to-Ground)	Mostly < 6kV	–	–	100
Voltage Unbalance	Mostly 2%, but occasionally 3%	10min	1 week	95
Harmonic Voltages	8% THD	10min	1 week	95

are equal, the system is balanced and no current flows though the neutral line. A typical power-grid monitoring scheme is shown in **Figure 1**. Each phase's power (voltage and current) measurements are obtained by a current transformer (CT) and a voltage transformer (a potential transformer, PT, in power-distribution nomenclature). The complete system comprises four such pairs (one pair for each of the three phases plus neutral).

As Figure 1 illustrates, the ADCs simultaneously measure the three phases and neutral voltages and currents. By performing digital processing on the sampled and digitally converted data, the active-, reactive-, apparent-energy, and power-factor parameters can be found and the line loads can be dynamically adjusted to correct for power factor. The result is increased power efficiency. The execution of a FFT (fast Fourier transform) on the sampled data can allow frequency and harmonic distortion metering to be achieved, while highlighting information such as system losses and the effects of unwanted noise.

Power-Monitoring System Requirements

Power-monitoring equipment must measure instantaneous current and voltage values with sample rates up to 60Hz × 256 samples, or greater than 15,360sps (samples per second), to accommodate the standard's requirements. This requirement and the need for precision up to 90dB form the basis for selecting the ADC used in the system.

The ADC's dynamic range for voltage measurement can be calculated from the maximum and nominal voltages to be monitored, and from the required accuracy for power measurements. For example, if a design must measure a 1.5kV (1500V) temporary overvoltage (under a fault condition) with a nominal 220V voltage measurement and 0.2% specified accuracy, then the total dynamic range of the voltage-measurement subsystem will need to be at least:

$$20\log((1500 \div 220) \times 2000) = 83\text{dB}$$

Note: In all these calculations, the required design accuracy is assumed to be 0.05%, which is better than the standard's 0.2% accuracy requirements. This design margin is used to ensure compliance to the standard.

Current-sensing requirements also affect ADC specifications. If the design requirements for power monitoring are the typical 100A:10A (10A nominal and 100A maximum) and Class 0.2 (0.2%), then the total dynamic range of the current-measurement subsystem will need to be:

$$20\log((100 \div 10) \times 2000) = 86\text{dB}$$

These examples clearly demonstrate the need for higher performance in today's ADCs. To achieve an 86dB dynamic range, a 16-bit ADC with sampling rates of 16ksps or higher is essential. To ensure accurate 3-phase and neutral wye system current and voltage measurements, the ADC must sample up to eight channels simultaneously (four voltage and four current). Additionally, the ability to correct the current and voltage transformer-induced phase shift (or delays) is critical for systems trying to measure and correct power factor to maximize power efficiency.

ADC Alternatives

When selecting the right ADC for a power-grid monitoring application, designers must look beyond sample rates and standard requirements. Today they must also consider factors like effective input impedance (Z_{IN}), signal-phase

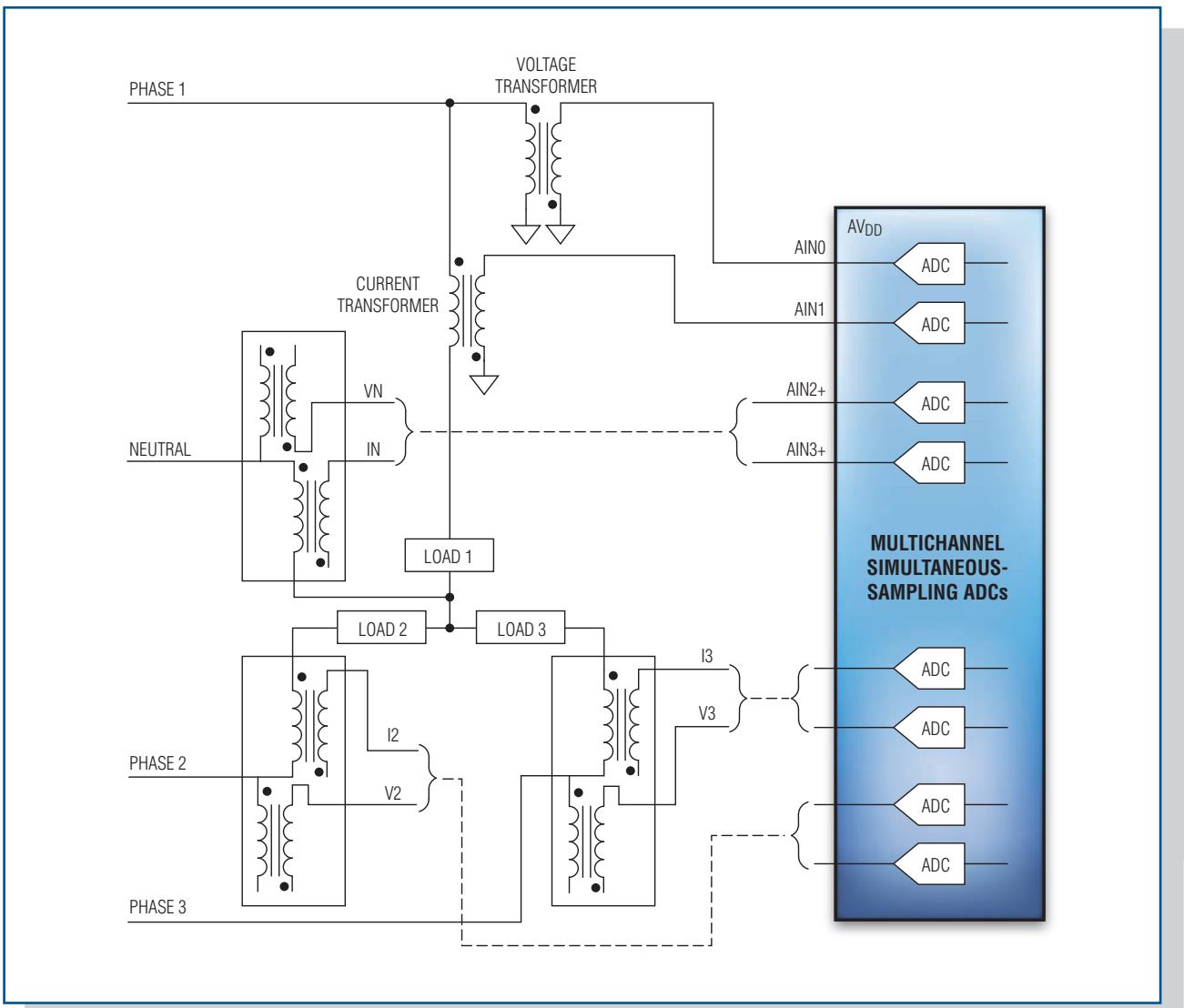

Figure 1. Typical power-grid monitoring application using simultaneous-sampling ADCs.

adjustment, and a small package size. Given these many system requirements, designers are turning to simultaneous-sampling, multichannel, high-performance ADCs for their powerline monitoring or multichannel SCADA (supervisory control and data acquisition) systems.

Several ADC solutions meet the rigorous standards of these power-grid monitoring applications. A majority of these targeted solutions are 6-channel, 16-bit simultaneous-sampling ADCs with sample rates up to 250ksps.

Several companies offer chips with up to six low-power, 250ksps SAR (successive approximation register)-type ADCs. Maxim offers the MAX11046*, which integrates eight high-precision, low-power, 16-bit, 250ksps SAR ADCs in a single package. The MAX11046 achieves greater than a 90dB signal-to-noise ratio.

Effective Input Impedance (Z_{IN})

Z_{IN} is dictated by the input capacitance and sampling frequency:

$$Z_{IN} = \frac{1}{(C_{IN} \times F_{SAMPLE})}$$

Where F_{SAMPLE} is the sampling frequency and C_{IN} = 15pF.

If the ADC has a high Z_{IN} like the MAX11046, it can interface directly with voltage and current-measurement transformers. That interface often eliminates the need for external precision instrumentation amplifiers, or buffers. The design therefore saves system cost, board area, and power. **Figure 2** shows an application example for a single-phase monitoring system based on the MAX11046 EV (evaluation) kit board connected to powerline monitor

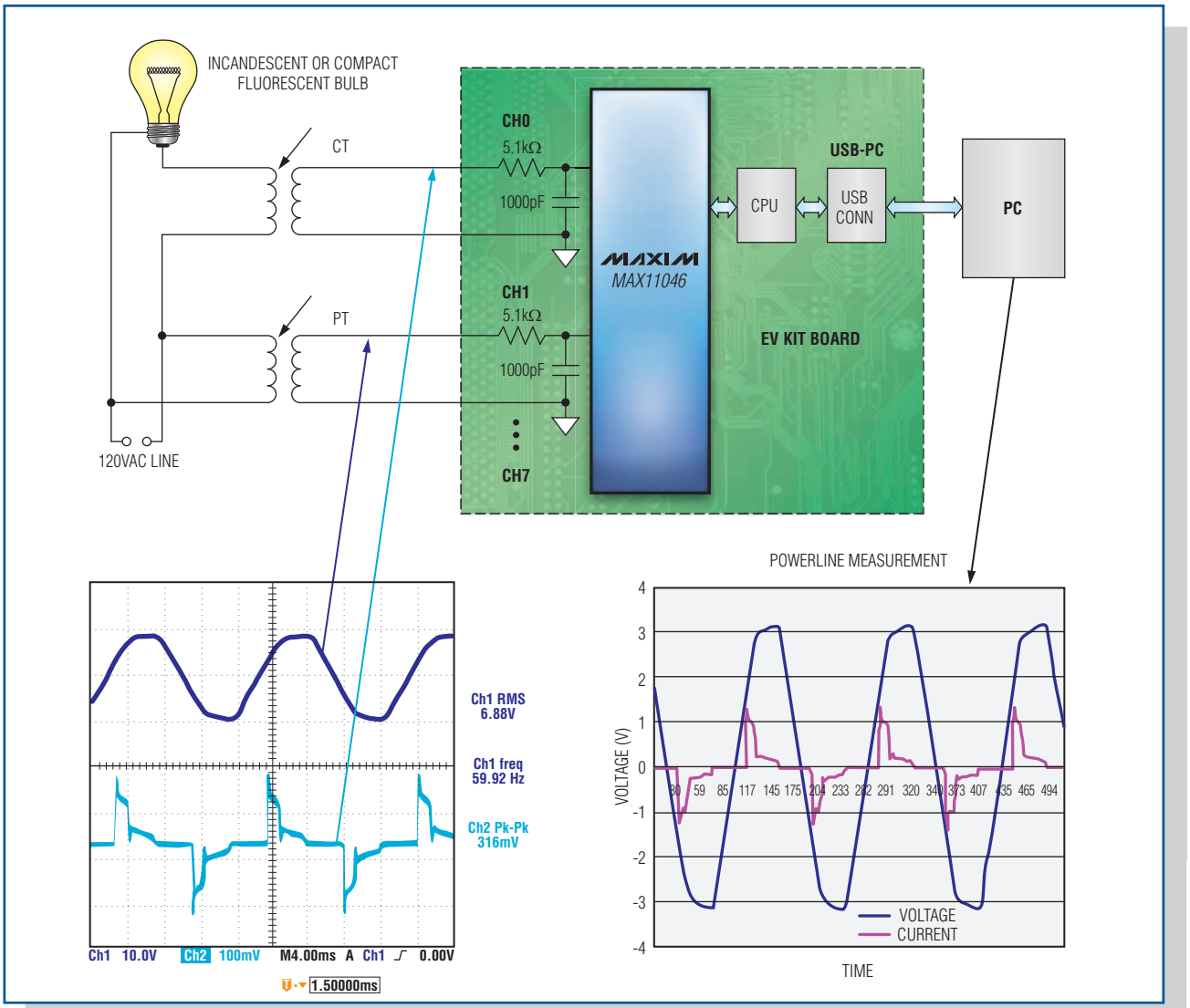

Figure 2. Multichannel simultaneous-sampling ADCs such as the Maxim MAX11046 simplify the design of advanced power-monitoring systems. A single-phase monitoring solution is shown in this example.

transformers. The schematic shows the simple cost and space-efficient interface between the powerline transformers and the simultaneous-sampling, multichannel data converter. For a three-phase power system, this circuitry is replicated for each phase and the neutral.

Signal-Phase Adjustment

As high voltage goes through the transformer and transitions to a lower voltage, a phase shift (or delay) occurs. This delay creates a significant problem for power-management or power-monitoring applications. To address this, designers can adjust phase in software at the backend or they can realign the signals inside the ADC upfront. Deskewing the voltage and current signals allows for true and accurate measurement of the power factor in the wye configuration. Shifts in phase from the 120° separation of the three phases represent lost power. Once the power factor is accurately measured, it can be corrected to make the grid exponentially more efficient.

Traditionally, signal-phase adjustment using simultaneous-sampling, multichannel 16-bit ADCs has been addressed digitally as a postprocessing step performed on the ADC's output data. Maxim's MAX11046 high-precision data converter handles phase adjustment in this manner. With such an ADC, continuous software overhead is required to address signal-phase adjustment.

Some of today's ADC solutions offer input-phase adjustments of 0 to 333µs with the delay independently settable per channel in 1.33µs steps. This design eliminates the software overhead mentioned above. One such device, the 24-bit, 4-channel MAX11040 sigma-delta ADC, provides this capability plus high-precision, simultaneous sampling of as many as 32 channels using a built-in cascade feature. Each channel includes an adjustable

sampling phase that permits internal compensation for phase shift due to external transformers or filters at the inputs. An active-low SYNC input allows periodic alignment of the conversion timing for up to eight devices with a remote timing source.

Small Package Size

In many power-grid monitoring applications, physical size matters. Often there is a need to monitor multiple polyphase supply lines, particularly in power-distribution centers. When examining the board area consumed by an ADC per-channel implementation, there are differences in the solutions available. For example, the MAX11040 solution uses 15.9mm^2 per channel, which is less than half the area of solutions offered by other vendors.

High packing density of the ADCs allows more channels to be physically loaded on a PCB. This helps minimize the overall size, power consumption, and cost of the measurement systems.

Overvoltage Protection

The optimal system design must also prevent system failures from overloads or other line disturbances. The MAX11040 and other devices in its family have built-in overvoltage protection (similar to ESD protection) through the use of clamp diodes set for 6V and an internal logic circuit that sets a fault bit if high voltage is detected. Other ADC vendors have their own approaches, but external diode protection is typically used.

Detecting power-grid shorts and opens is a primary function of many of these protection systems using ADCs. Detection is done by looking at the data coming from the ADC. Criteria for when to trip a relay are complex and highly proprietary to each monitoring system vendor. Nonetheless, it is generally agreed that it is as bad to trip in a false situation as it is not to trip in a fault situation.

Conclusion

Rising worldwide power demands are driving rapid investment in the power-delivery infrastructure or "smart grid." By integrating power-supply monitoring, dynamic load balancing, protection and metering functions, and advanced powerline monitoring systems, utility companies (and customers) can monitor, deliver, consume, and control grid power more efficiently.

Complicating the development and widespread adoption of these power-grid monitoring systems are the varying standards and agency requirements. Stringent specifications, such as the EN 50160, IEC 62053, and IEC 61850 standards, dictate the precision energy measurement, the minimum accuracy, and the sample rate needed for real-time power-delivery monitoring, fault-detection and protection, and dynamic load balancing. These standard requirements create clear criteria for the ADCs utilized in such a modern multichannel ADC system. Other factors, including effective input impedance (Z_{IN}), signal-phase adjustment, and small package size, also influence ADC selection.

Today's high-performance, simultaneous-sampling ADCs are optimized for three-phase power (plus neutral) monitoring and measurement systems. These devices are a natural choice for high-density designs that need to provide high performance while reducing total system cost and minimizing board area.

The author wishes to thank Joseph Shtargot for his advice and support in completing this article.
A similar article appeared on the *EDN Magazine* website on August 18, 2009.
*Future product—contact factory for availability.

Overcome the Challenges of Integrating HB LEDs in Automotive Systems

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HB LEDs provide a number of advantages over traditional lighting technologies in automotive applications. They are more environmentally friendly, improve safety, enhance the look and style of vehicles, and have longer life. But designing a highly efficient, low-cost, high-performance HB LED-based lighting solution presents many challenges. A new generation of multistring LED drivers makes it easier to meet all those challenges.

Introduction

Today's automobile manufacturers are converting more of their lighting systems from incandescent and CCFLs (cold-cathode fluorescents) to HB (high-brightness) LEDs. These HB LEDs are used for backlighting in navigation and entertainment displays, for internal cabin lights, and for external lighting such as daylight running lights and tail lights. New applications like heads-up displays are also expected to leverage HB LEDs.

First-generation HB LED drivers had some limitations. They did not allow designers to optimize efficiency, minimize external component count, minimize EMI, or achieve a very wide PWM dimming range. The latest generation of multistring HB LED drivers, such as the MAX16814, solves these design challenges in unique ways by allowing intercommunication between their switching and linear control sections. This article presents an example design for daylight running lights or heads-up displays.

Why HB LEDs?

HB LEDs are gaining popularity in the automotive world, quite simply because they offer automobile designers many advantages. HB LEDs are a more environmentally friendly technology than other lighting technologies—they have superior energy efficiency and do not contain mercury, thus they release fewer harmful chemicals when recycled. HB LEDs can also improve car safety. They turn on and off faster than incandescent lamps, which is why they are commonly adopted for brake lights.

HB LEDs allow car makers greater freedom in designing the style or "look" of their vehicles. The LEDs are small, directional sources of light that require almost no depth behind the panel. Designers can create light arrays of any shape thanks to the small size and directionality of the light emitter. As a small emitter of light, they are ideal for applications with light guides.

Finally, with lifetimes of 50,000 hours or more, HB LEDs have a much longer life than any other lighting technology. This makes them ideal for any application where the light remains on for an extensive amount of time. Daytime running lights are an ideal example.

HB LED technology is also important for advancing new applications like heads-up displays. The ability to dim LEDs over a very wide range, depending on the intensity of the ambient light, is particularly useful. Here is where PWM dimming becomes so important.

When you understand the "why" of HB LEDs, it is no surprise that their use is becoming prevalent in automobile design today. Their applications include brake lights and rear lights; front lights (daytime running lights, position lights in mid-to-high-end cars, and high- and low-beam lights in very high-end vehicles); and interior lights, where RGB LEDs allow control of light color, giving a unique style to the vehicle. The application of HB LEDs in navigation, entertainment, and cluster display backlights is also becoming mainstream (**Figure 1**).

Challenges of Designing with HB LEDs

Of course, the integration of HB LEDs into automotive applications presents challenges. Keeping cost as low as possible is an immediate concern. LED lamps are, in general, a more costly lighting solution than other technologies (e.g., incandescent, halogen, CCFLs) at the component level. For this reason, the cost of LED solutions at the system level must be minimized to improve the market penetration of this technology. To reduce the solution cost, the number of components required by the driver must be kept as low as possible. This approach also improves reliability, because each component on the PCB is a potential failure point in the system.

Another challenge is efficiency. High energy efficiency is increasingly important in cars, especially hybrid vehicles. Efficiency must be optimized to reduce power dissipation (heat). Automotive components work in a hot environment, with maximum ambient temperatures of +105°C for parts in the engine compartment or +85°C for many other applications. LEDs generate considerable conducted heat (they do not irradiate energy in IR or UV bands like other kinds of lights), and so their power dissipation also contributes to raising the ambient temperature. Thus, it is essential to minimize power dissipation from the LED driver to avoid overheating the IC or other components in the driver module.

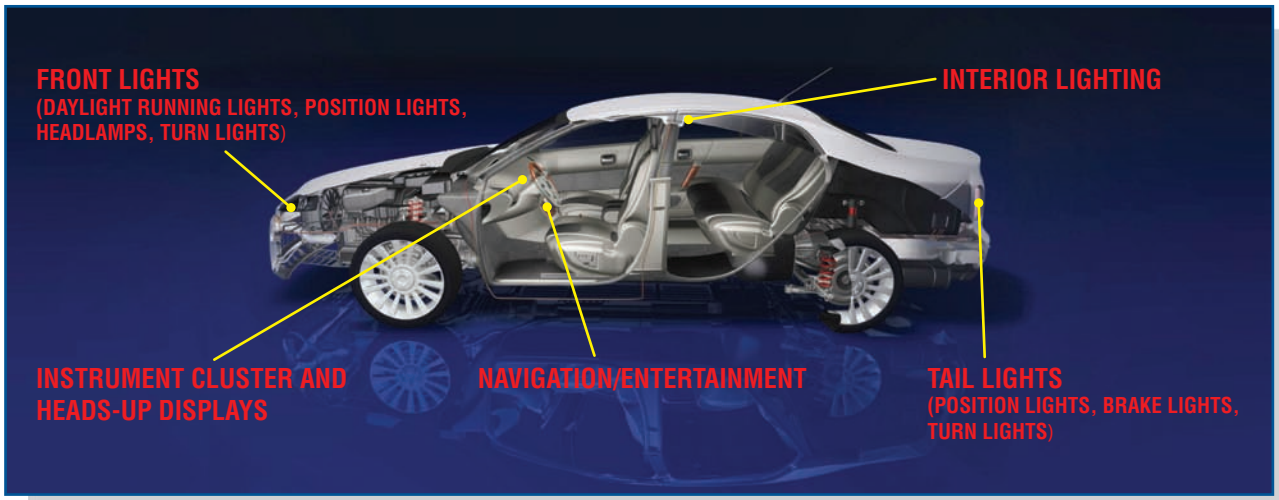

Figure 1. HB LEDs are making inroads into every automotive-lighting application, from headlamps to brake lights and everything in between.

To no surprise, automotive environments have challenging requirements for EMI. The lighting subsystem can interfere with other vehicle subsystems, of which the AM radio is usually the most sensitive. This can be an issue since LEDs require electronic switching or linear driver circuits that can cause EMI noise (especially switching circuits) or EMI susceptibility. The driver circuits can also cause unpleasant audible noise, for example from ceramic capacitors.

Benefits of Multistring LEDs

A number of automotive applications require LEDs to be placed on multiple strings. A string is a group of LEDs connected in series, therefore having the same current. The form factor of displays makes it easier to place LEDs on multiple strings for their backlights. Having multiple strings, moreover, improves fault tolerance. If one LED breaks, only the LEDs in that particular string fail to light, not all of the LEDs in all the strings. For safety reasons, multiple strings also limit the voltage of an individual LED string. As an example, a single LED string with 80V total voltage can be split into two strings of 40V each, thus reducing the risk of injury to someone who accidentally touches the LED contacts or wires.

Multistring drivers, therefore, offer an obvious, overriding advantage: just one IC is required for many strings. For example, a multistring configuration could include the LED strings; a single boost converter, which converts the input battery voltage into a higher voltage required by the LED strings; and multiple, linear current sinks that set the current of each string (**Figure 2**).

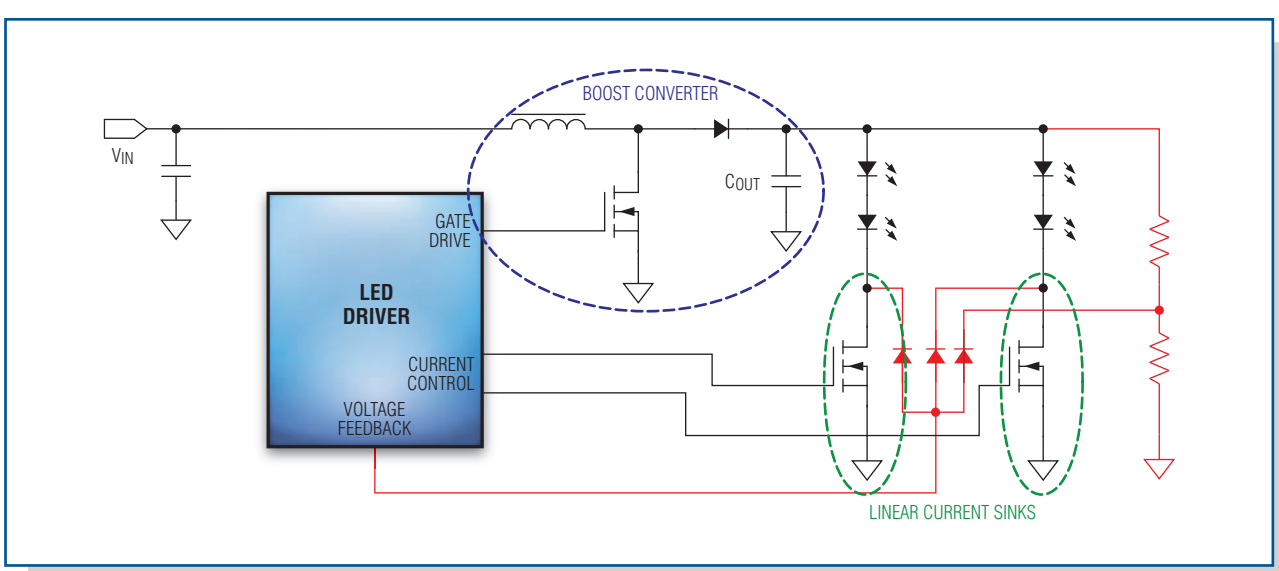

Figure 2. A basic multistring driver configuration uses a single chip to control the current to multiple LED strings. Components shown in red can be added to perform adaptive voltage optimization while the boost converter and linear current sinks work independently.

Compared to the solution with multiple switching converters, this solution has fewer components and lower cost (a single inductor and fewer shunt capacitors are needed). Compared to having a single-string driver and directly connecting the LED strings in parallel, there is an advantage in the current balancing among the strings. If multiple strings are directly connected in parallel, the current splits unevenly among them because some LEDs have higher forward voltage than others. Moreover, since the LED forward voltage decreases with increasing temperature, this current imbalance can cause thermal runaway. The string with more current is hotter, its forward voltage decreases, so it draws even more current, becomes even hotter, and so on. The current imbalance grows, and one or more strings carrying greater current can fail. Finally, if the LED strings are simply paralleled, the driver controls only the total current. When one string fails and opens, its current is transferred to the other strings, which can then fail because they are overdriven. None of these problems happens with the current-balancing solution in Figure 2.

There is, admittedly, a limitation of the topology of Figure 2: it uses linear MOSFETs to set the string currents. To keep the temperature of those MOSFETs low, the voltage drop across them must be as low as possible, but high enough to keep them in their saturation region. The boost output voltage must then ideally be:

$$V_{BOOST} = \max(V_{STRING,I}) + V_{SAT}$$

Where $V_{STRING,I}$ is the total forward voltage of string I, and V_{SAT} is the V_{DS} needed for the linear MOSFETs to remain in saturation. An LED driver that sets V_{BOOST} to its ideal value is said to perform AVO (adaptive voltage optimization).

AVO is further complicated because LEDs must be PWM-dimmed in most applications. They must be turned on and off with a certain duty cycle, and that is done by turning their linear current sinks on and off. But then, what should the boost converter do when all the LED strings are turned off? This is another design problem with many possible answers and some limitations, as we will discuss.

Problems with Traditional Multistring Drivers

Traditional multistring LED driver solutions using the topology of Figure 2 include a boost switching converter and multiple current sinks that work as separate entities. When those drivers are used, implementing AVO requires some external components which, in turn, can cause their own set of issues.

One problem is that an external circuit must detect which LED string has the highest forward voltage (or the lowest cathode voltage). This can be done with a few diodes, such as the structure marked red in Figure 2. This solution causes the board area and solution cost to increase.

Another concern is what happens when an LED fault occurs. If an LED fails and opens the circuit, the voltage at the cathode of that string falls to zero; the diode circuit detects that LED string as the one with the highest forward voltage. Consequently, it tries to provide enough voltage for that string and starts increasing V_{BOOST}. This results in multiple possible problems. An increase in the voltage is applied to the current-sink MOSFETs of the other strings, which can then cause them to fail. Or, the voltage increase can trigger the output OVP (overvoltage protection) of the boost converter (if present) which shuts it off, thus turning off all the strings.

A third issue is what this circuit should do when the LEDs are PWM-dimmed. When the LEDs are off, the diode circuit has no string voltage as a reference to set V_{BOOST}. A possible solution is to add another diode connected to the boost output through a divider, as done with the circuitry marked red in Figure 2. This diode turns on when the LEDs are off, and sets V_{BOOST} to a predetermined voltage. The obvious problem with this solution is that the output voltage of the boost converter has a high ripple at the PWM dimming frequency. (See **Figure 3**.) This voltage rippling can cause EMI noise which, as mentioned above, is a serious problem for automotive applications. Voltage ripple can also cause unpleasant audible noise from the output capacitor, C_{OUT}.

Advances in the New Generation of Multistring Drivers

New-generation multistring drivers have greatly improved performance. Instead of having the converter and current sinks work independently, they allow communication between the boost switching converter and the linear current-sink portions of the design. Thus, these new multistring drivers address the three design issues described above.

In these new-generation drivers, the IC internally senses the LED string voltages, i.e., the voltages at the drains of each current-sink MOSFET. The IC then selects the lowest string voltage with an internal diode- or analog-switch-based circuit (**Figure 4**). In this way, the number of external components and the solution cost are substantially decreased.

This intercommunication solves the disruptive problem when one LED in a string fails and opens the circuit. If an LED fault happens in this new design, the V_{BOOST} starts increasing. Once this voltage reaches an OVP threshold, the faulty string is identified, disabled, and removed from the AVO control loop. The other strings continue working normally. Most importantly for the user, the effect of the LED failure is merely reduced brightness of light instead of a complete turn-off.

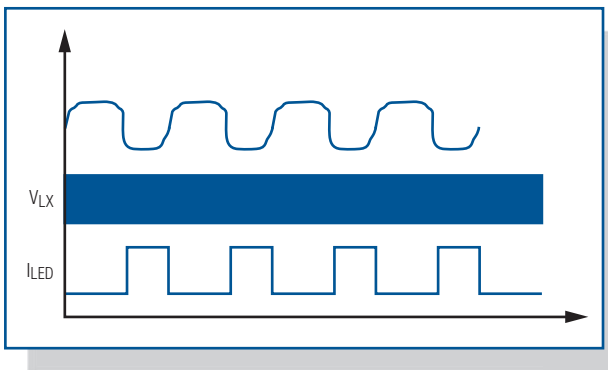

Figure 3a. With a traditional driver performing PWM dimming and utilizing the external circuitry of Figure 2, the V_{BOOST} changes between the on- and off-time of the LED current. The result is a noisy voltage rail.

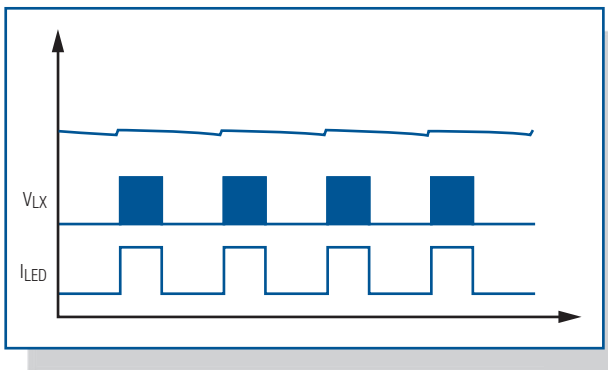

Figure 3b. With a new-generation driver, the boost converter stops switching during the off-time of the LED current. Thus, the converter's output is maintained by its output capacitor and the voltage only slightly decreases due to leakage currents.

There are some concerns regarding what the LED driver's switching converter should do when the LEDs are PWM dimmed. The integration of the switching and linear sections allows a different and quieter solution than the one described in Figure 2. Now the boost converter can be "frozen" when the LEDs are off, as in Figure 3b. While the converter stops switching, the switching power MOSFET is kept open and the compensation circuitry is opened as well. At this point, the compensation capacitor retains its charge, which is the state of the compensation loop. V_{BOOST} is then retained by C_{OUT}, which is not discharged because the LEDs are off. The only discharge current from C_{OUT} is leakage current. When the LEDs come back on, the converter restarts switching with minimal ripple. With this solution, V_{BOOST} remains almost constant throughout the PWM dimming cycle, thus considerably reducing both EMI noise and audible noise from the output capacitor.

The only limitation of this solution is that the PWM dimming on-time must be longer than a few (e.g., three or four) switching cycles. Longer on-time is needed so that the boost converter can recharge C_{OUT} with the charge that leaked off during the off-time. This limits the minimum duty cycle that can be achieved.

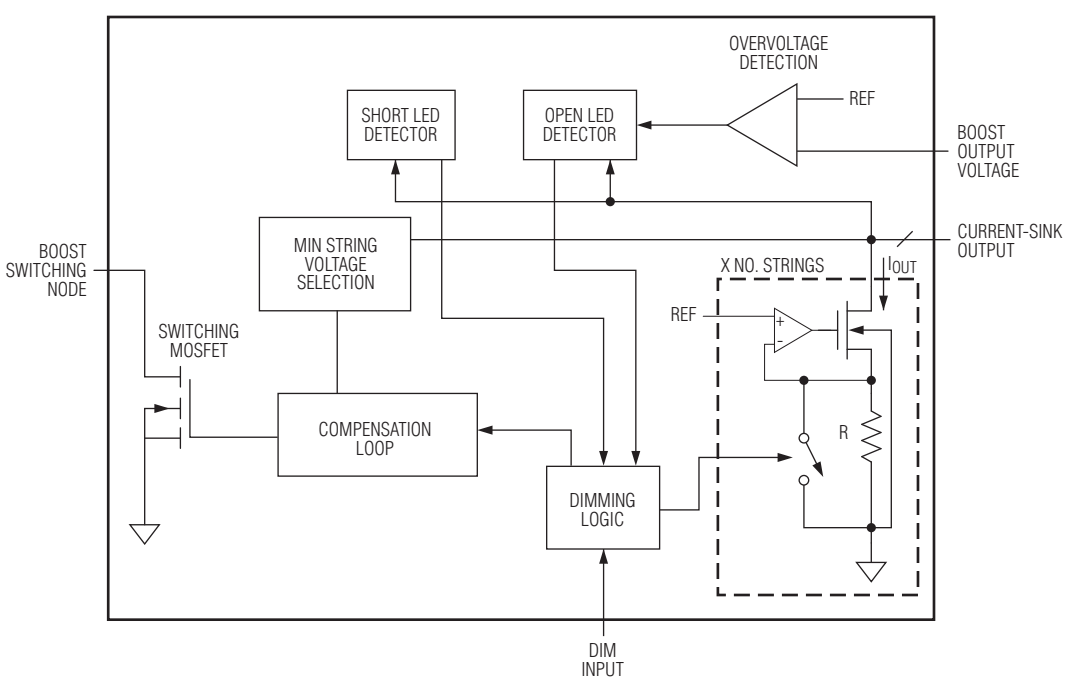

Figure 4. In a new-generation HB LED driver IC, internal communication between the LED sink drivers and the boost converter allows more effective control and eliminates many of the issues encountered by older drivers.

Applying the New-Generation Drivers

In a car, both the daytime running lights and heads-up displays have similar performance demands: they are on whenever the car is running, and need high reliability/redundancy to ensure that they are always available. By using a new-generation multistring driver such as the MAX16814, the required high reliability can be achieved while component count is minimized, thus improving reliability with fewer parts to fail and reducing system cost.

These life-critical applications are also similar in their system requirements: operation over a wide input voltage range; sustaining voltage peaks (load dump) of typically up to 40V from the car battery; and low EMI generation.

Fault tolerance is essential. It is critical that the LED light never shuts off completely in case of a fault. Using a multistring approach in combination with the MAX16814 assures that if one LED opens or shorts, only that string is shut down; other strings will continue to work normally. Additionally, because of its fault output, the MAX16814 can signal back to the driver that one LED failed (**Figure 5**).

Heads-up displays also need a very wide (1000:1 or more) PWM dimming range. The MAX16814 integrates a unique PWM dimming solution that eliminates ripple at V_{BOOST} (at the dimming frequency), thus minimizing EMI and audible noise. This MAX16814 solution is similar to the approach used in Figure 3b, but it also allows a very wide PWM dimming range of 5000:1 at 200Hz. This dimming range is wider than any similar product, and overcomes the minimum on-time limitation mentioned above.

The MAX16814 can drive 4 LED strings with up to 150mA per string, and provides the requisite intercommunication between the switching and linear control sections. This chip thus dramatically reduces external component count. Additionally, the MAX16814 includes a complete set of fault-protection and detection features. If any string has LED open or short failures, that string is disabled and the fault condition is signaled to the system. Finally, this IC is a full-featured automotive product, with a 40V maximum input voltage capability and a -40°C to +125°C operating temperature range.

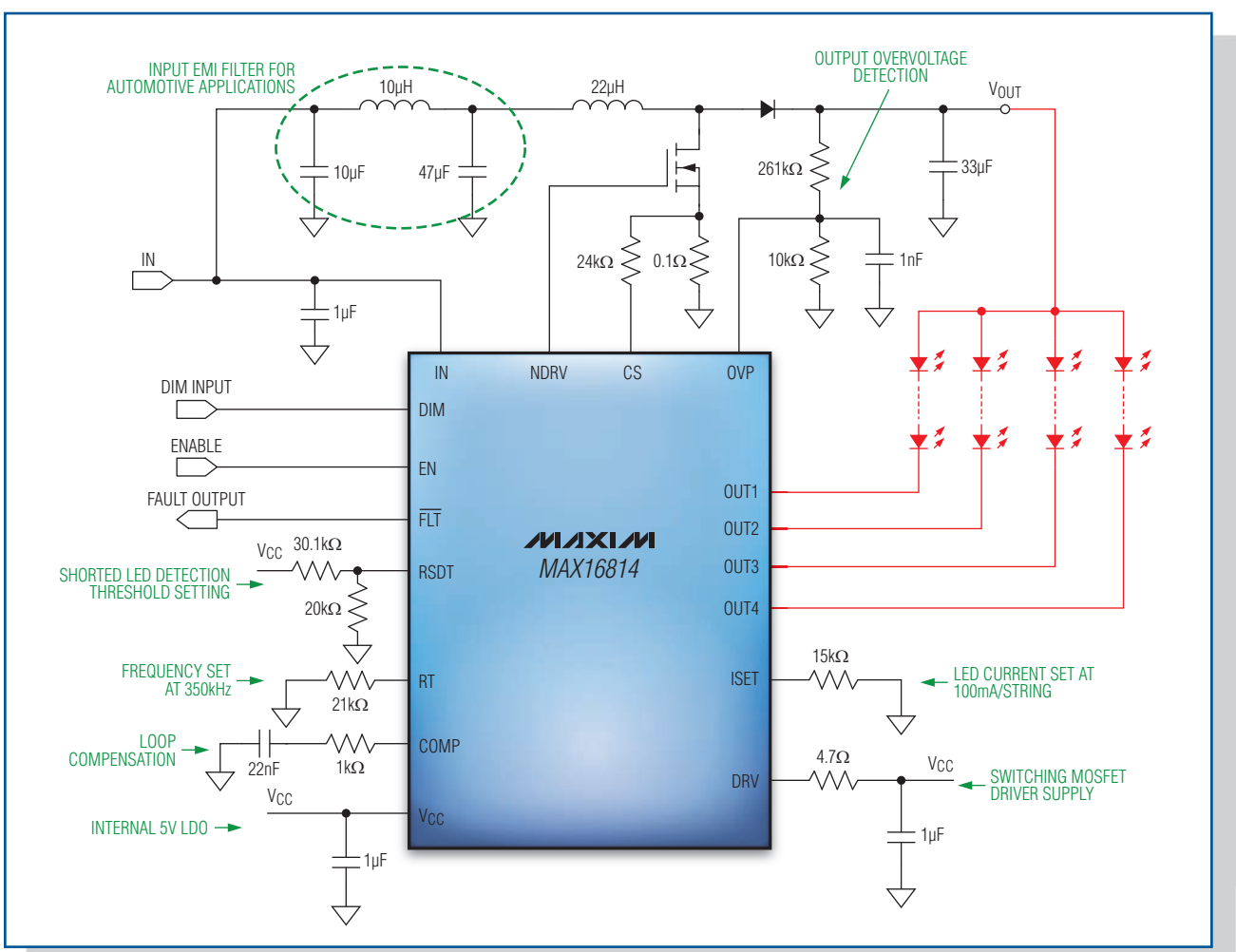

Figure 5. This is an example of a complete automotive design for a heads-up or running-light driver subsystem, including all the external components and an input EMI filter. Because of the low noise of the MAX16814, the EMI filter component value can be kept low.

Table 1. Summary of HB LED Driving Approaches

Solution	External Components	Efficiency	Current Balancing	Response of Other LED Strings if One Opens	EMI and Noise with PWM Dimming	PWM Dimming Range
Multiple Switching Converters	Many	High	Good	They continue to work	Low	Wide
LED Strings Paralleled, Single-String Driver	Very few	Medium	Bad	Their current increases; they can fail	Low	Wide
Independent Boost Converter and Linear Sinks, Without AVO	Few	Low	Good	They continue to work	Low	Wide
Independent Boost Converter and Linear Sinks, with AVO	Some	Medium	Good	They can turn off	Noise at dimming frequency	Wide
Internal Communication Between Boost Converter and Multiple Linear Sinks	Few	Medium	Good	They can continue to work	Low	Limited
MAXIM MAX16814	Few	Medium	Good	They continue to work	Low	Wide (5000:1 at 200Hz)

When designing an HB LED-based system, many tradeoffs are possible, such as component count, efficiency, and reliability. **Table 1** compares various multi-LED driver solutions to help designers select the best approach for their application.

Newer generation LED drivers lower component count. Moreover, by leveraging the intercommunication between switching and linear sections, they provide more cost-effective solutions, higher efficiency, and improved features including better fault protection and detection. The MAX16814 is a multistring driver that provides all of these advantages plus a wider PWM dimming range than any similar product available in the market.

A similar article appeared in the July/August, 2009, issue of *Power Systems Design* magazine.

Minimize Voltage Offsets in Precision Amplifiers

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Maxim Integrated Products

Voltage-offset errors in precision amplifiers are partly caused by input bias currents. This article analyzes the problem and proposes a solution based on resistor networks, both discrete and integrated. The analysis shows that integrated resistors can outperform the more costly discrete approach.

In precision electronics, amplifier stages must comply with precisely designed performance specifications. One problem encountered when designing these amplifiers is the voltage offset generated by currents flowing into the amplifier inputs. In this article, we first analyze the source of this offset, and then propose a solution based on integrated resistor networks.

Analyzing the Problem

Before attempting to solve a problem, we need to understand its source. For that purpose, consider the simplified schematic for an ideal op amp (**Figure 1**).

The analysis of this circuit should be well known to first-year students (we assume zero current at the amplifier inputs):

$$V^- = V_{OUT} \times \frac{R1}{R1 + R2} = V_{IN}$$

Rearranging:

$$A_V = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1}$$

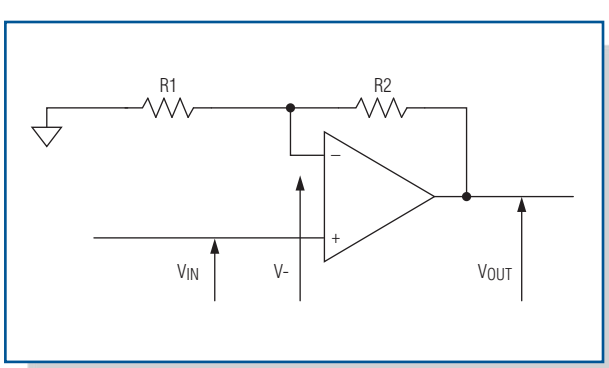

Figure 1. This simplified schematic depicts an ideal op-amp circuit.

You can make the analysis more realistic by introducing a finite input resistance, which gives the op amp a finite input bias current. We model this effect with a current source on each input of the ideal op amp (**Figure 2**).

To analyze the effect of each of these current sources, assume that V_{IN} = 0V. We assume that the impedance at V_{IN} is small in relation to other impedances, so I_{BIAS+} will be shunted to ground and have no effect. Because V_{IN} = 0V, V^- must also equal 0V. Moreover, because both ends of R1 are at the same 0V potential, it can be eliminated from the analysis. Thus, we immediately see an unwanted output offset (V_{OUT}), due to the input bias current (I_{BIAS-}) and feedback resistor (R2):

$$V_{OUT} = I_{BIAS-} \times R2$$

Solving the Problem

The circuit can be improved by adding one extra resistor (R3 in **Figure 3**). We need to examine the effect of this extra resistor, which causes the positive input to be offset negative by $I_{BIAS+} \times R3$. You can, therefore, adjust R3 to nullify the effect of bias current into the negative input. It is reasonable, however, to make the approximation that positive and negative input bias currents are the same.

With V_{IN} = 0, you can easily calculate V_{OUT} by noting that we have a voltage adder circuit, i.e., the output voltage is the voltage applied to the positive terminal times the voltage gain, plus an offset due to input current leakage into the negative terminal. Because V_{IN} = 0, any voltage applied to the positive terminal is due to leakage into that terminal, and R3:

$$V_{OUT} = -I_{BIAS-} \times R2 + I_{BIAS+} \times R3 \times A_V$$

$$V_{OUT} = -I_{BIAS-} \times R2 + I_{BIAS+} \times R3 \times \frac{R1 + R2}{R1}$$

$$I_{BIAS-} \times R2 = I_{BIAS+} \times R3 \times \frac{R1 + R2}{R1}$$

$$R2 = R3 \times \frac{R1 + R2}{R1}$$

$$R3 = \frac{R1 \times R2}{R1 + R2}$$

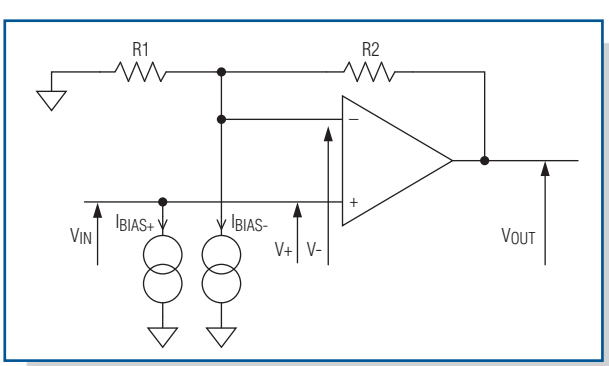

Figure 2. Current sources model input bias currents for the ideal op amp of Figure 1.

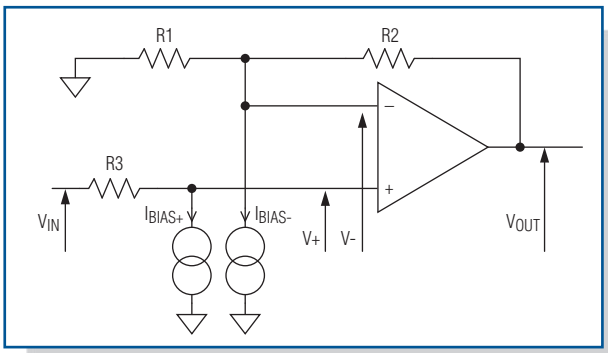

Figure 3. Adding a compensation resistor (R3) to the Figure 2 circuit cancels the effect of input bias currents.

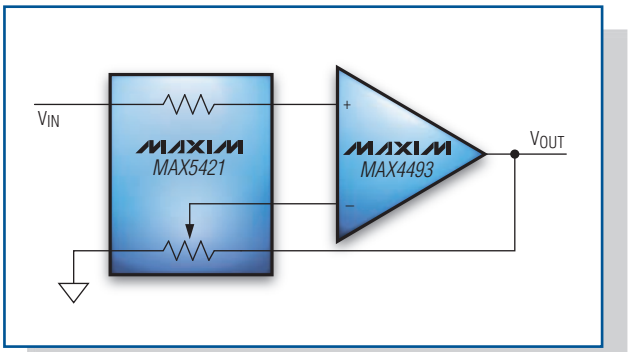

Figure 4. This precision amplifier combines precision resistors (MAX5421 ICs) with a general-purpose, rail-to-rail op amp (the MAX4493).

If R3 equals the parallel combination of R1 and R2, the voltages generated by input bias currents should cancel. For the high-precision applications in which this technique is generally used, the resistors should be specified as follows:

- The ratio R2/R1 must have high precision in order to set a precision gain.
- The match between R3 and the parallel combination of R1 and R2 must also be high precision so errors introduced by the input bias currents are compensated.
- These resistors must track with temperature.

You can use either integrated or discrete resistors in the precision op-amp circuit of Figure 3.

Integrated Resistors

The MAX5421 (as an example) includes 15kΩ resistors and operates with a supply voltage of +5V or -5V. A similar part, the MAX5431, includes 57kΩ resistors and operates with a supply voltage of +15V or -15V. These devices not only include precision integrated resistors, but they also switch between the resistors. When the resistors are used to set gain in an op-amp circuit, this capability allows you to choose among programmable gains of 1, 2, 4, and 8.

Data sheets for these devices show that they exhibit constant resistance at the resistor-pair node for resistor ratios of 2, 4, and 8. If the ratio is 1, you see only the low resistance of the node. For all ratios, therefore, the matching resistor should equal the wiper resistance (**Table 1**).

Resistor tolerances are shown in **Table 2**.

Note that these tolerances are guaranteed maximums over the full operating temperature range of -40°C to +85°C, which in turn guarantees the gain tolerance to a high level of precision. A typical integrated-resistor design (a precision amplifier) is shown in **Figure 4**.

The main technical advantages of integrated resistor chips like the MAX5421 or MAX5431 are matching and temperature tracking between the resistors. You can then select a desired system gain by electronically switching among the gain-setting resistors.

The absolute resistance of an integrated resistor has a large tolerance. That is not a problem in these circuits, however, because gain values are precisely set by resistor ratios to within ±0.025%. If the matching resistor is external, you will have difficulty choosing the correct value, but integrated matching resistors make the task easy. Integrated resistors can be factory trimmed, and they track the gain-setting resistors precisely with temperature. Any tolerance in R1 and R2 also affects R3, so R3 should match the parallel combination of R1 and R2.

If your system does not require R3, you may be able to reduce costs by using digitally programmable, precision voltage-dividers like the MAX5420 and MAX5430. These

Table 1. Matching Resistor Settings for MAX5421/ MAX5431 Dividers

		MAX5421 (V_{DD} = +5V, V_{SS} = -5V)	MAX5431 (V_{DD} = +15V, V_{SS} = -15V)
Wiper Resistance (kΩ, typ)	**Ratio: 1**	0.3	0.5
	Ratio: 2, 4, 8	8	14
Matching Resistance (kΩ, typ)	**Ratio: 1**	0.3	0.5
	Ratio: 2, 4, 8	8	14

Table 2. Resistor Tolerances for MAX5421/MAX5431 Dividers

Part	Divider Ratio Accuracy (±%, max)
MAX5421_A	0.025
MAX5421_B	0.09
MAX5421_C	0.5
MAX5431_A	0.025
MAX5431_B	0.09
MAX5431_C	0.5

devices have the same performance as the MAX5421 and MAX5431, but do not contain the matching resistor. For fixed-gain applications, consider the MAX5490, MAX5491, and MAX5492 resistor-dividers, which contain one fixed-ratio pair of resistors only and no matching resistor.

Discrete-Resistor Approach

Now, consider the gain-setting resistors for an alternate, discrete-component approach. The pair of discrete resistors must not only have a ratio tolerance of ±0.025%, but they must also track within this tolerance over the required temperature range. In practice, this means that each resistor must have a tolerance of 0.0125%. Resistor data sheets often specify an initial tolerance plus a temperature coefficient. We can therefore calculate the worst-case tolerance over the temperature range in question. The example below is based on specifications for an ultra-precision discrete resistor with a low temperature coefficient:

Initial tolerance: 0.005%

Temperature coefficient: 2ppm

Operating temperature range: -40°C to +85°C

The resistor tolerance over this range is, therefore:

$$R_{TOL} = \begin{matrix} -(0.005 + (40 + 25) \times 2 \times 10^{-6})\% \\ (0.005 + (85 - 25) \times 2 \times 10^{-6})\% \end{matrix}$$

$$R_{TOL} = \begin{matrix} -0.018\% \\ 0.017\% \end{matrix}$$

To match the gain tolerance of an op amp with integrated resistors, you must use ultra-high-precision resistors like those above. Such discrete resistors are available, but they cost several dollars each. The resistor for input-offset matching is less critical, but its cost is prohibitive for a discrete component that comes *even close* to the performance of an integrated resistor. A single pair of resistors costs far more than a MAX542x or MAX543x (for example), which integrate all the resistors required for four gain settings, plus a matching resistor and all the switches and logic necessary to implement gain switching.

Conclusion

We have analyzed the problem of voltage-offset error caused by input bias currents in a precision system. By examining the discrete- vs. integrated-resistor approaches, we conclude that integrated resistors outperform their more costly discrete counterparts.

Improve Two-Phase Buck Converter Performance with a Coupled-Choke Topology

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Interleaved multiphase converters or synchronous buck converters are usually employed to supply power to microprocessors. However, these designs typically have large ripple currents in their inductors, and thus the converters will have relatively high switching losses. One alternative that reduces switching losses is to use a coupled-choke topology in the multiphase converter. The coupled chokes improve supply efficiency by reducing the phase ripple without increasing the output ripple voltage. Furthermore, the combination of the coupled-choke topology and a lower leakage inductance will also improve the converter's transient response.

Introduction

Power supplies for today's high-performance microprocessors require high-current, low-voltage DC-DC converters with fast transient responses. Those supplies must deliver currents of more than 100A at voltages of 1V and below. Additionally, they must respond to load-current changes in nanoseconds. During the load changes, moreover, the supply's output voltage must remain within a narrow regulation boundary. However, a small amount of output-voltage "droop" is permitted such that the output voltage decreases slightly within the regulation boundary when the load current increases.

Synchronous buck converters are normally used to power microprocessors. These converters typically step down a 12V input from a bus converter to 1.0V or lower. However, buck converters require higher steady-state levels and a fast transient response to load changes. To achieve that performance, a small inductor allows quick current ramping and can reduce the size of the output capacitor. There is, however, a problem with this approach: small inductor values lead to large ripple current in the inductor and higher switching losses for the converter.

Interleaved multiphase converters substantially cancel the ripple current in the output capacitor. That allows designers to reduce the output capacitor's capacitance without affecting the ripple voltage. Alternatively, they can reduce the inductance per phase so that the power supply responds to load-current changes quicker. There is, nonetheless, still a problem with this design. As the inductance per phase in the uncoupled multiphase buck converter is reduced, phase ripple current increases. So again, the switching losses and the copper losses also increase.

An alternative approach uses a coupled-choke topology in a multiphase converter. This design prevents any increase in switching losses by reducing the phase ripple for the same output-ripple voltage. Additionally, if you use a coupled choke with lower leakage inductance, the converter's transient response can also be improved.

The Coupled-Choke Topology

There are many industry-standard multiphase buck controllers and converters available today. This article uses the MAX8686 controller to compare the performance of a coupled-choke vs. an uncoupled-choke topology in a multiphase converter. Two MAX8686 controllers will be used to form a two-phase buck converter.

The MAX8686 is a current-mode, synchronous PWM step-down regulator with integrated MOSFETs. The controller operates from a 4.5V to 20V input supply, and provides an adjustable output voltage from 0.7V to 5.5V while delivering up to 25A per phase. The controller can be configured for single-phase as well as multiphase operation. For multiphase operation, the MAX8686 can operate in master or slave mode.

Figure 1 illustrates the two approaches: two-phase converters with coupled-choke and uncoupled-choke topologies. $L_{OUT\_WINDING1}$ and $L_{OUT\_WINDING2}$ can be two windings of the coupled choke or two physically separate inductors. With coupled chokes, how the two windings are connected (i.e., in phase or out of phase) is very important.

A prototype board using the MAX8686 is shown in **Figure 2**. The converter is running at 400kHz; the input voltage is 12V and output voltage is 1.2V with a maximum-rated current of 50A. This converter delivers up to 40A at +70°C with as little as 200 LFM of airflow.

Issues Involving the Inductors

Inductor current waveforms and LX voltage waveforms using two inductors are shown in **Figure 3**. The two inductors are Vishay® model 0.56µH-IHLP-4040DZ-11.

Inductor currents are combined in the output capacitors. Figures 3b and 3c show the same waveforms for the converter using a coupled choke with two windings. The coupled choke used for this example is the BI Technologies HM00-07559LFTR which has a self-inductance of

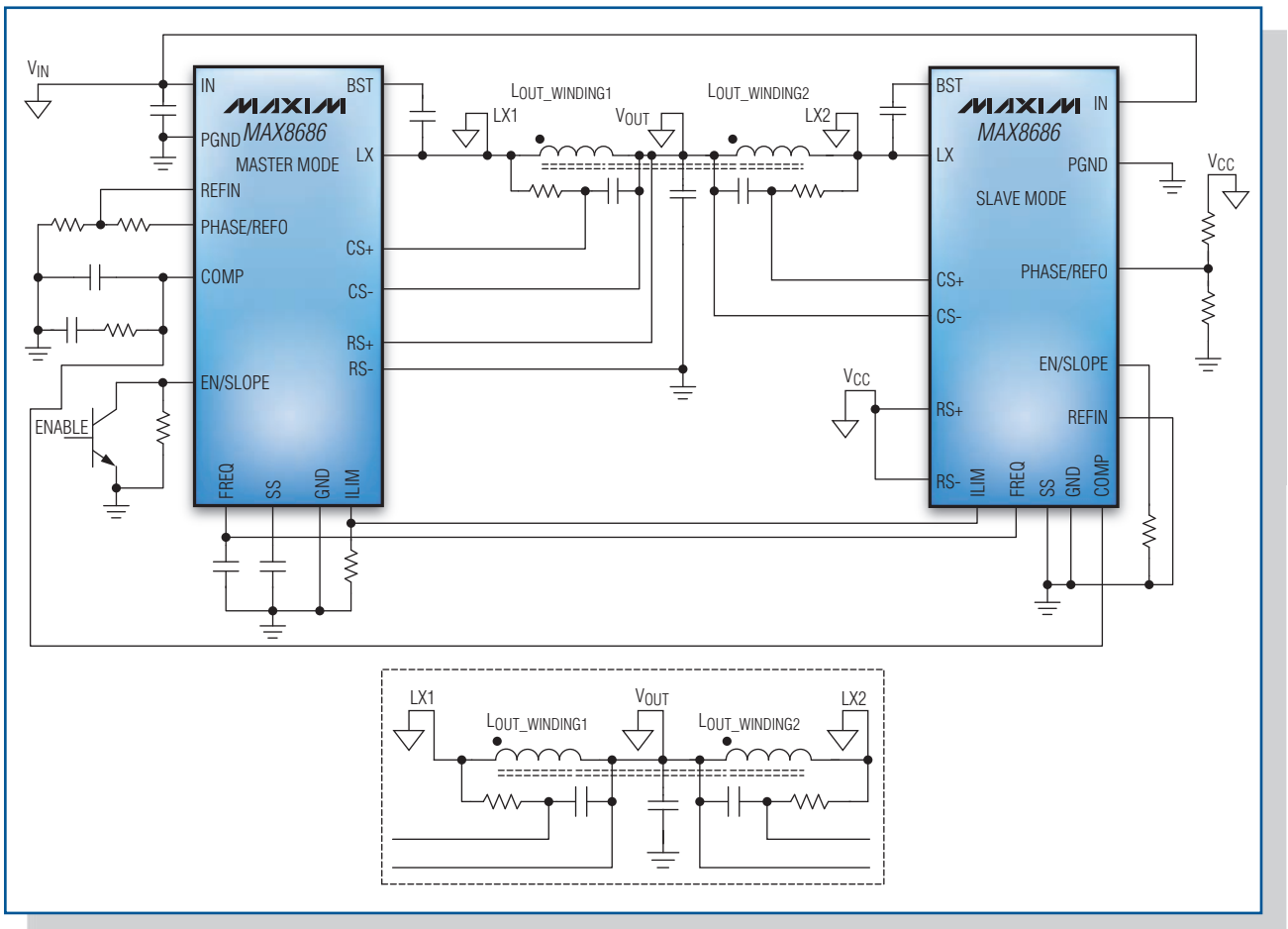

Figure 1. Schematic of a two-phase buck converter with a coupled choke. Note the polarity of winding for out-of-phase connection. The winding polarity shown here produces the best performance. In the inset, two inductors are also used to reduce the magnetic coupling. Now polarity does not matter.

0.6µH (typ) and leakage inductance of 0.3µH (min). The waveform in Figure 3b shows inductor current when coupled-choke windings are connected out of phase. Figure 3c shows current waveforms when windings are connected in phase. The in-phase connection is not recommended because it increases the phase current, making the converter less efficient.

Figure 3a shows that with two separate inductors there is only one current pulse per phase through each inductor. This compares with Figures 3b and 3c, where there are two current pulses per switching cycle with the coupled choke. However, the in-phase connection of the winding causes current to decrease rather than increase when the second phase turns on. When the windings are connected out of phase with the coupled-choke approach, the ripple current is cancelled. It does not matter how the two separate inductors are connected, as there is no mutual inductance between them. The waveform in Figure 3d shows phase current with a coupled choke and with the windings connected out of phase at a load current of 40A.

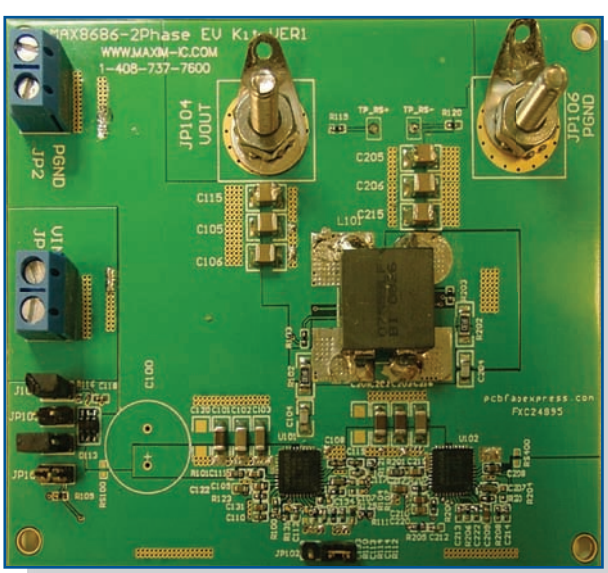

Figure 2. A prototype board with two MAX8686 PWM controllers and a coupled choke can deliver a maximum current of 50A at an output voltage of 1.2V.

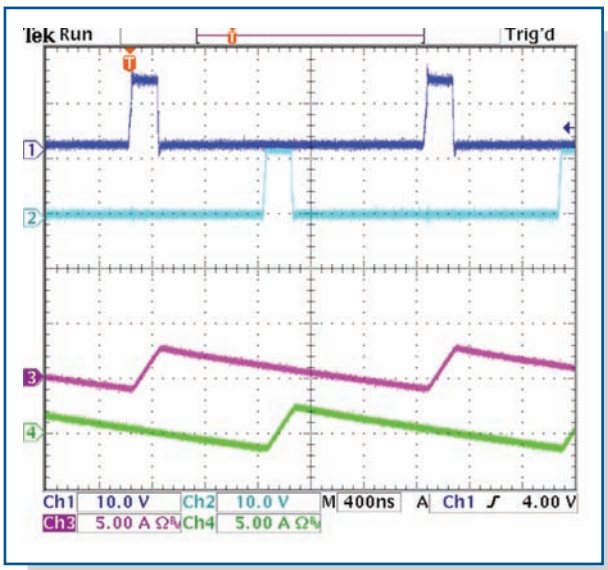

Figure 3a
Two-phase board with two chokes.
Ch1: master LX voltage; Ch2: slave LX voltage;
Ch3: master inductor current; Ch4: slave inductor current;
V_{IN} = 12V; V_{OUT} = 1.2V/no load.

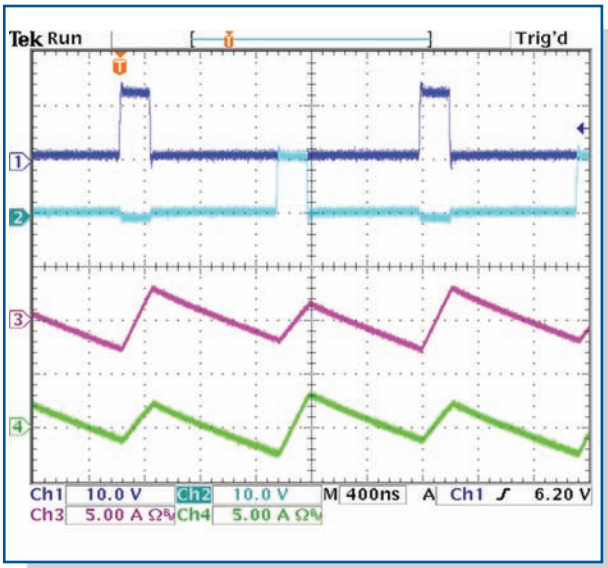

Figure 3b
Two-phase board with coupled choke, out of phase.
Ch1: master LX voltage; Ch2: slave LX voltage;
Ch3: master inductor current; Ch4: slave inductor current;
V_{IN} = 12V; V_{OUT} = 1.2V/no load.

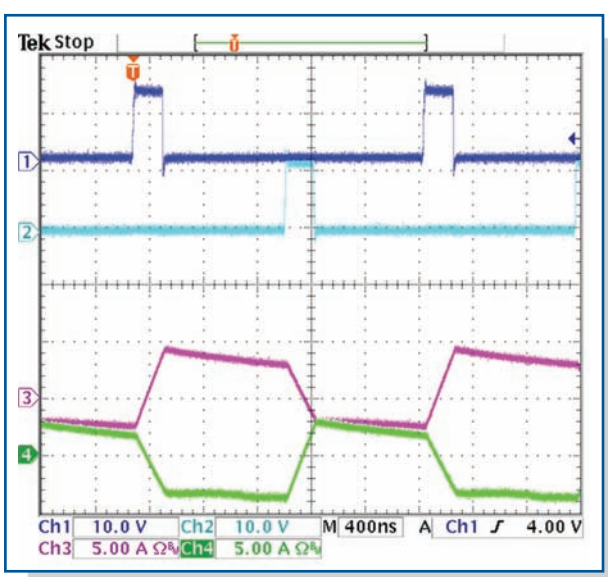

Figure 3c
Two-phase board with coupled choke, in phase.
Ch1: master LX voltage; Ch2: slave LX voltage;
Ch3: master inductor current; Ch4: slave inductor current;
V_{IN} = 12V; V_{OUT} = 1.2V/no load.

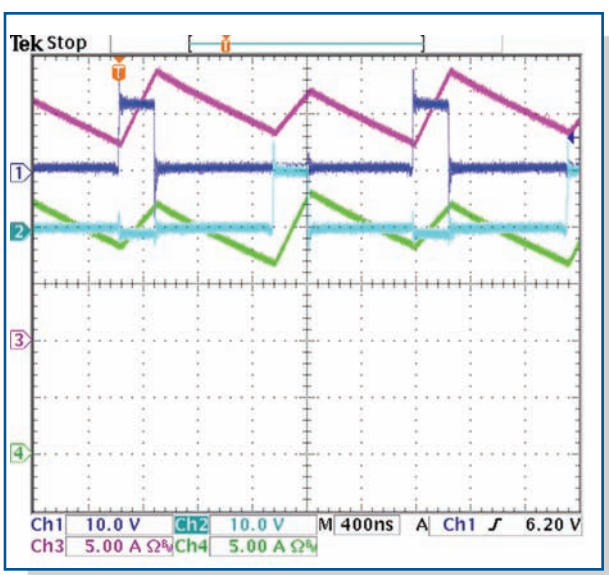

Figure 3d
Two-phase board with coupled choke, out of phase.
Ch1: master LX voltage; Ch2: slave LX voltage;
Ch3: master inductor current; Ch4: slave inductor current;
V_{IN} = 12V; V_{OUT} = 1.2V/40A.

Figure 3. Waveforms for various choke combinations show the differences in converter performance. In 3a and 3b a two-phase board is demonstrated using discrete inductors and a coupled inductor, respectively. In 3c and 3d the coupled-choke performance is shown for in-phase and out-of-phase connections, respectively. ***Note:*** *When a coupled choke is connected in phase, then ripple current is increased and efficiency is reduced. This design is not recommended.*

The selection of the output inductor is very important for efficiency and transient response optimization. Its value is calculated based on the amount of permitted inductor ripple current. A larger inductance can reduce ripple current and increase efficiency, provided that the DC resistance of the choke is not increased. However, the larger inductance value will increase the inductor's size since a larger value will require more wire. However, to keep the resistance value constant, a larger diameter wire must be used, thus making the inductor larger.

If a larger value inductor is used, the output inductor's current slew rate will slow down during a load transient. LIR is defined as the ratio of ripple current to load current per phase. A compromised LIR value ranges from 0.2 to 0.5. LIR can be higher when more phases are used to take advantage of ripple-current cancellation. Therefore, to ensure optimal LIR the selected inductor should have a low DC resistance and the saturation current should be greater than the peak inductor current. If the inductor's DC resistance is used to sense output current, then the current-sense signal should have enough amplitude for current-mode operation of the MAX8686. A signal level of 10mV (min) is recommended to avoid any sensitivity to noise.

Issues Involving the Capacitors

An input capacitor is used both to reduce the peak current drawn from the DC input source, and to reduce noise and ripple voltage caused by the circuit switching. The input capacitor must meet the ripple-current requirement imposed by the switching current. Low-ESR (equivalent series resistance) aluminum electrolytic, polymer, or ceramic capacitors should be used to avoid large-voltage transients at the input during a large-step load change at the output. The ripple-current specifications provided by the manufacturer should be carefully reviewed for temperature derating. A 10°C to 20°C rise in temperature is acceptable. Additional small-value low-ESL (equivalent series inductance) ceramic capacitors can be used in parallel to reduce any high-frequency ringing.

The key selection parameters for output capacitors are the actual capacitance value, the ESR, ESL, and the voltage rating requirement. These parameters affect overall stability, output voltage ripple, and transient response. The output ripple voltage has three components: variations in the charge stored in the output capacitor, the voltage drop across ESR, and ESL due to current flowing into and out of the capacitors. The design equations used to select the capacitors are given below.

Design Calculations

Starting Conditions

V_{IN} = 12V; V_{OUT} = 1.2V; I_{OUT} = 50A; η = 0.85

Operating frequency = 400kHz; N = 2

N = number of phases; η = efficiency factor

Inductor Value Calculations

Start by calculating the power dissipation and the input current for the converter:

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

$$P_{IN} = \frac{P_{OUT}}{\eta}$$

$$P_{DISS} = P_{IN} - P_{OUT}$$

$$60W = 1.2V \times 50A$$

$$70.58W = 60W/0.85$$

Therefore:

$$P_{DISS} = 10.58W\ (70.58W - 60W)$$

$$I_{IN}\ (av) = P_{IN}/V_{IN} = 70.58W/12V = 5.882A$$

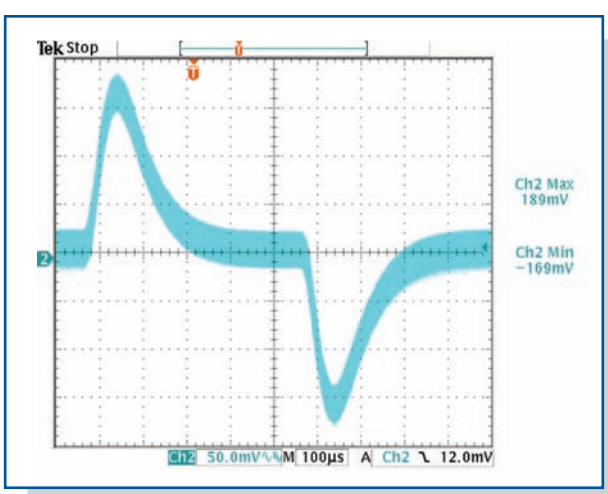

Figure 4a
Two-phase board with two separate inductors.
Transient loading;
Ch1: O/P voltage;
V_{IN} = 12V; V_{OUT} = 1.2V/5A–25A–5A.

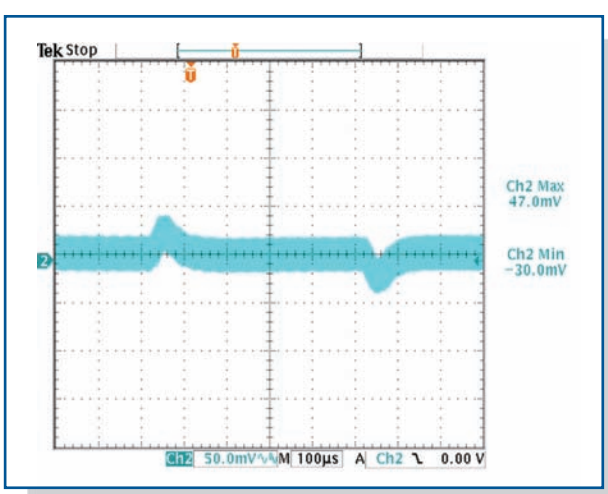

Figure 4b
Two-phase board with coupled choke, out of phase.
Transient loading;
Ch1: O/P voltage;
V_{IN} = 12V; V_{OUT} =1.2V/5A–25A–5A.

Figure 4. The waveforms in this figure show the out-of-phase transient response for two separate inductors (4a) and a coupled inductor (4b).

Next, calculate the output inductor value:

$$D = \frac{V_{OUT}}{V_{IN} \times \eta} = 1.2/(12 \times 0.85) = 0.118$$

LIR = inductor ripple current factor = $\Delta I/I_{OUT} = 0.2$

Now solve for $\Delta I \rightarrow 0.2 \times I_{OUT}$ (This will be needed in the output ripple calculation.)

$$L_{OUT} = \frac{V_{OUT} \times (1 - D) \times N}{LIR \times Freq \times I_{OUT}}$$

$$= (1.2 \times (1 - 0.118) \times 2)/(0.2 \times 400kHz \times 50)$$

$$= .5294\mu H$$

The closest off-the-shelf inductor value is 0.56µH and it has a DC resistance of 0.0017Ω.

Peak Current Calculations

$$I_{PK} = \frac{I_{OUT}}{N} \times \left(1 + \frac{LIR}{2}\right) = 50/2 \times (1 + 0.2/2) = 27.7A$$

Input Capacitor (C_{IN}) Calculation

$N \times D = 0.235$, and for $N \times D < 1$

$$I_{IN(RMS)} = D \times I_{OUT} \times \sqrt{\frac{1}{N \times D} - 1}$$

$$= 0.118 \times 50 \times 1.804$$

$$= 10.6A$$

Where $I_{IN(RMS)}$ is the RMS ripple current through the input capacitor.

Output Ripple Voltage (V_{RIPPLE}) Calculations

Assume:

ESR = $(2.5/6) \times 10^{-3}$ (ESR of output capacitor)

ESL = $(1/6) \times 10^{-9}$ (ESL minus the parasitic inductance of output capacitor)

$C_{OUT} = 600\mu F$

Calculate V_{RIPPLE}:

$$V_{RIPPLE} \text{ (at } C_{OUT}) = \frac{\Delta I}{8 \times C_{OUT} \times Freq \times N}$$

$$= 10/(8 \times 600\mu F \times 400kHz \times 2)$$

$$= 2.6mV$$

$$V_{RIPPLE} \text{ (ESL)} = \frac{V_{IN}}{L_{OUT} + ESL} \times ESL$$

$$= (12V/(0.56\mu F + 0.166pH)) \times 0.166pH$$

$$= 3.56mV$$

$$V_{RIPPLE} \text{ (ESR)} = \Delta I \times ESR = 10 \times 0.416 \times 10^{-3} = 4.16mV$$

Thus, the full V_{RIPPLE} voltage is:

$$V_{RIPPLE} (C_{OUT}) + V_{RIPPLE} \text{ (ESL)} + V_{RIPPLE} \text{ (ESR)}$$

Therefore:

V_{RIPPLE} = approximately 10mV

Performance Improvements of the Coupled-Choke Topology

Figures 4a and **4b** show the transient load comparison for the converters with coupled choke and two separate inductors. The coupled-choke approach delivers a considerably improved transient response because the transient load in the coupled choke is restricted by leakage inductance only, and not by self-inductance. This design experienced no decrease in phase inductance.

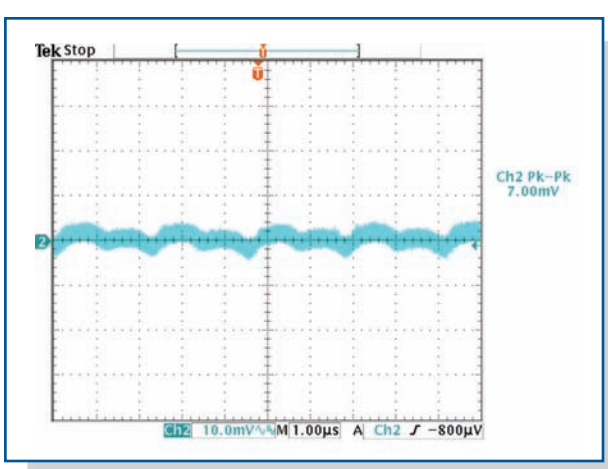

Figure 5a

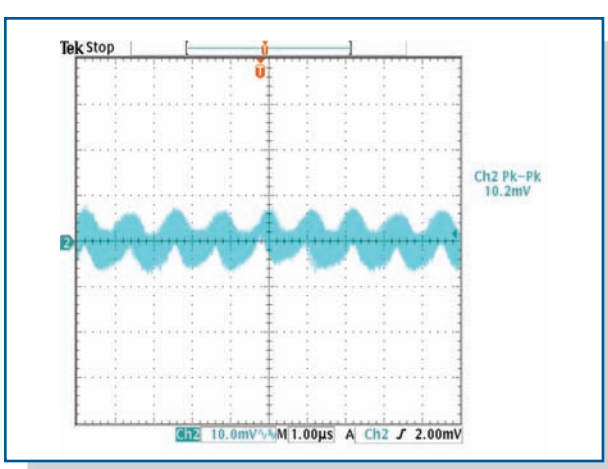

Figure 5b

Figure 5. Output ripple for the coupled inductor (coupled choke, 5a) is much smaller than the ripple for a design using two separate inductors (separate chokes, 5b).

The waveforms in **Figure 5a** and **5b** show the output ripple voltage at full load using both approaches. The curves in **Figure 6** compare the efficiency for an uncoupled and coupled version of two-phase converters. Once again, efficiency is also improved with the coupled choke. No-load current will be more with the coupled choke, which is why the coupled-choke approach will have a lower efficiency during light load conditions. At higher loads the coupled-choke topology delivers better efficiency.

A similar article appeared in the May, 2009, edition of *Power Electronics Technology* magazine.

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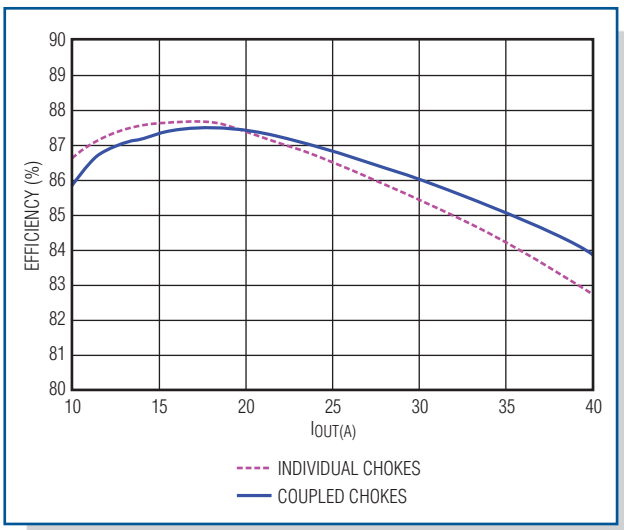

Figure 6. The converter efficiency for the coupled inductor is better for heavy loads. For light loads the two separate inductors deliver slightly better efficiency.