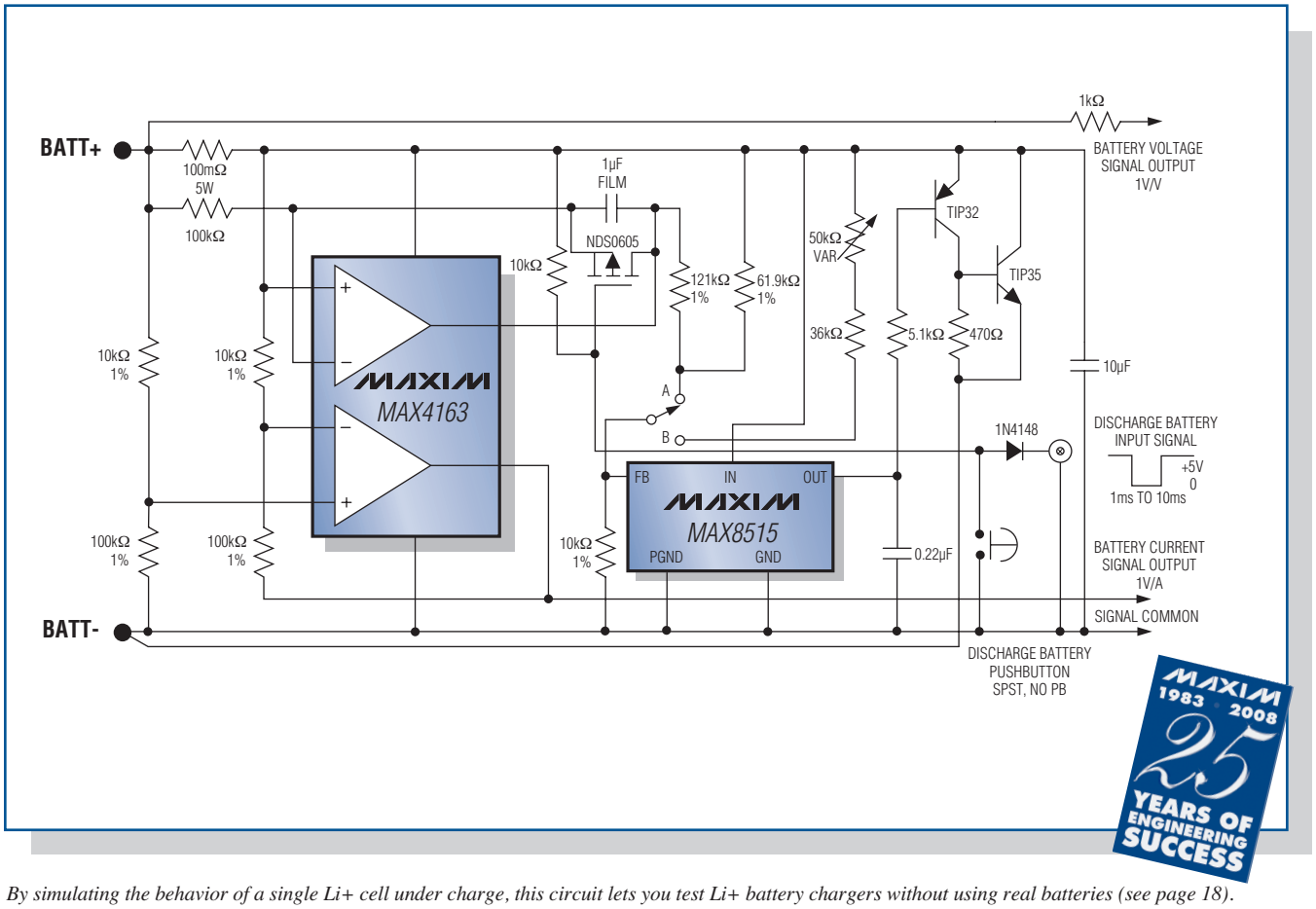
MAXIM Engineering Journal

Volume Sixty-Four



By simulating the behavior of a single Li+ cell under charge, this circuit lets you test Li+ battery chargers without using real batteries (see page 18).

Letter from the CEO

Making Your Life Easier

For over 25 years, Maxim has been simplifying the lives of design engineers worldwide. Our highly integrated engineering solutions reduce the complexity of designs, minimize system costs, and speed your time to market. And, with over 5700 ICs in 28 product categories, we offer a broad range of solutions for your many design challenges.

Yet, we do more than provide integrated circuits. As fellow engineers, we also know that you have to make difficult choices throughout the design process, and that time to market can frequently determine the success or failure of a design. Thus, we have made it easier for you to find the right IC, evaluate potential solutions, and get technical support if you encounter an obstacle in your design.

Maxim recently introduced a much-improved, web-based parametric search system to help you find exactly the right part for your application. Designed by engineers for engineers, the revamped parametric tool offers the functionality you need, while delivering extremely fast search responses.

For rapid navigation, all functions (such as searching and sorting) are executed locally by the user's browser. Thus, once a product family page has loaded, there are no more calls back to Maxim's server. Because it is so fast, the search system can automatically update the list of matching products and the remaining available choices the instant you make a selection. Additionally, the intelligent search algorithm only shows valid criteria, ensuring that you do not waste time making selections that eliminate all products.

The parametric system also offers powerful filtering and sorting tools. You can sort hierarchically on any number of parameters (in columns), hide and show columns, and select and compare any shortlist of products from the current results. Again, all of this happens on your computer, so the search system is faster and more responsive than our competitors' tools.

As ever, almost all of Maxim's products are available as free samples upon request. To speed your evaluations, we have increased the availability of samples and evaluation kits. We now ship over 55% of samples the same day, and over 95% the same week.

Should you encounter an obstacle in your design, Maxim's dedicated technical support team is available to help you find a solution. Internally, we have updated our request tracking system so that it monitors customer traffic on our website's Maxim Support Center. Requests are now entered into a database and tracked online, with replies and follow-ups threaded and visible to our staff so that nothing falls through the proverbial cracks.

Whether through engineering solutions or up-to-date resources, Maxim continues to search for ways to make your life easier. Stay tuned for simulation tools and more. And if there is anything else that we can do to better serve you, please let me know at tunc@maxim-ic.com.

We are always at your service,

Tunç Doluca
President and Chief Executive Officer

Unbalanced Twisted Pairs Can Give You the Jitters!

By Ron Olisar, Principal Member of Technical Staff

The transmission of serial-digital video above 1Gbps (as required by the DVI™, HDMI™, and DisplayPort™ video-interface standards) has elevated the performance requirements for the cables that connect PC and HDTV monitors. Consequently, the traditional suppliers of analog audio/video cable must now learn the same lessons that makers of datacom serial-digital differential cables learned for InfiniBand® and PCI Express® at 2.5Gbps, CX4 at 3.125Gbps, and Fibre Channel at 4.25Gbps.

This article highlights the phenomenon of data jitter caused by conversions between differential- and common-mode components of the video signal. It also exposes myths about intrapair skew, and proposes cable tests for the purpose of predicting jitter. The article demonstrates that differential cables with good performance need not be expensive, just well balanced.

The most common type of differential cable for digital-video signaling in the 0.25Gbps to 3.40Gbps range required by DVI/HDMI systems is 100Ω shielded twisted pair (STP). One-hundred-ohm twin-axial (twinax) cable is an alternative, and is a mainstay of datacom applications.

Keeping Your Balance

DVI, HDMI, and DisplayPort systems each include four lanes of differential interconnect for digital-video signaling. The signal can be recovered with inexpensive receive electronics, if two provisions are met: 1) the differential paths maintain the transmitted signals in differential mode, with little or no conversion to common mode; 2) the differential paths are balanced, which means that the two lines have symmetrical effects on the signal.

A cable that maintains signal energy in differential mode produces predictable phase delays and skin-effect losses across the frequency spectrum. Both effects are easily compensated. Otherwise, the signal may not be recoverable by an ordinary receiver. Indeed, conversion between differential and common modes in a coupled differential cable (STP or twinax) is an aberration that destroys the ability to predict phase delay and signal loss.

A related measurement of signal corruption is intrapair skew, which results from different propagation delays on the two lines of a differential pair. To illustrate, consider a pair of twin-coax cables cut into different lengths **(Figure 1)**. The input is differential; that is, no common-mode voltage is present. The output, however, contains intrapair skew equal to the difference in propagation delays. Along with intrapair skew you find common-mode energy, as well as reduced differential-mode energy.

The stimulus used in this example is sinusoidal, rather than a digital nonreturn-to-zero (NRZ) waveform. Skew delay

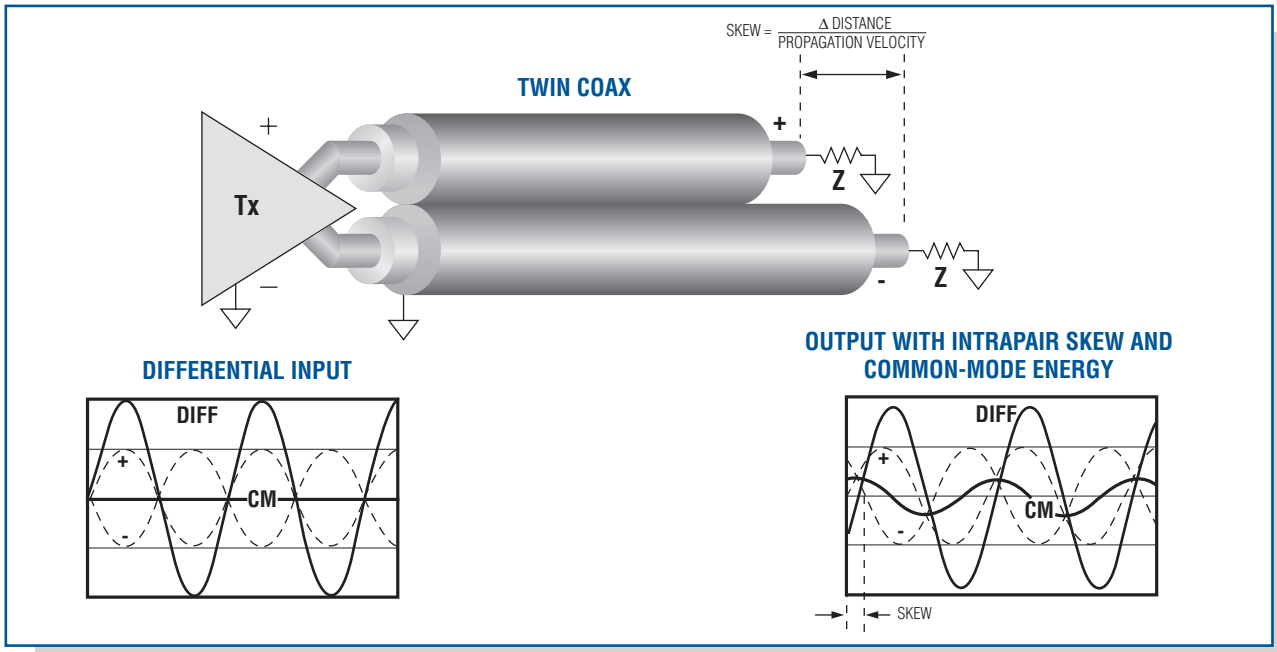


Figure 1. Simple intrapair skew converts some differential signal to common-mode (CM) energy.

for the simple twin-coax cable in Figure 1 is constant over frequency. In STP or twinax cables, however, each sinusoidal (Fourier) component of a digital NRZ waveform suffers a different amount of skew.

Myths of Intrapair Skew

A commonly measured symptom of conversion between differential- and common-mode energy, intrapair skew is frequently used by cable manufacturers as a QA test for cables. However, the conventional methods for measuring intrapair skew provide misleading results that are not predictive of jitter.

Myth 1: Intrapair skew has a fixed value vs. frequency.

This statement is true for uncoupled differential pairs like twin coax, but it is not true for coupled cables such as STP and twinax. **Figure 2** illustrates this effect for 28AWG twinax. Intrapair skew can actually reverse its polarity at different frequencies.

Myth 2: Intrapair skew scales with cable length.

This characteristic is true at very low frequencies (wavelength long compared to the cable length), but it is not true at high frequencies for coupled cables such as STP and twinax. Figure 2 shows the intrapair skew for various lengths of 28AWG twinax. Note that between 300MHz and 1500MHz, the 10-foot length has the worst intrapair skew.

Myth 3: Intrapair skew can be predicted using the step-stimulus test method.

This test launches a differential or single-ended voltage step into one end of a cable, and measures the time difference (skew) between (+) and (-) edges at the other end. Unfortunately, the cable itself lowpass-filters these output edges, and that effect is dramatic in long cables. Thus, the method demonstrates low-frequency intrapair skew, but says nothing about the high-frequency intrapair skew that matters most for serial-digital video!

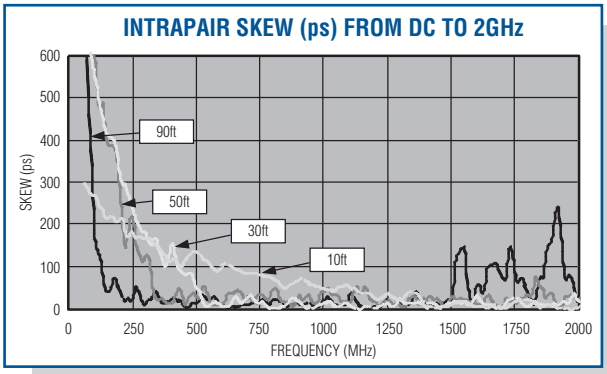


Figure 2. Intrapair skew vs. frequency for 28AWG twinax.

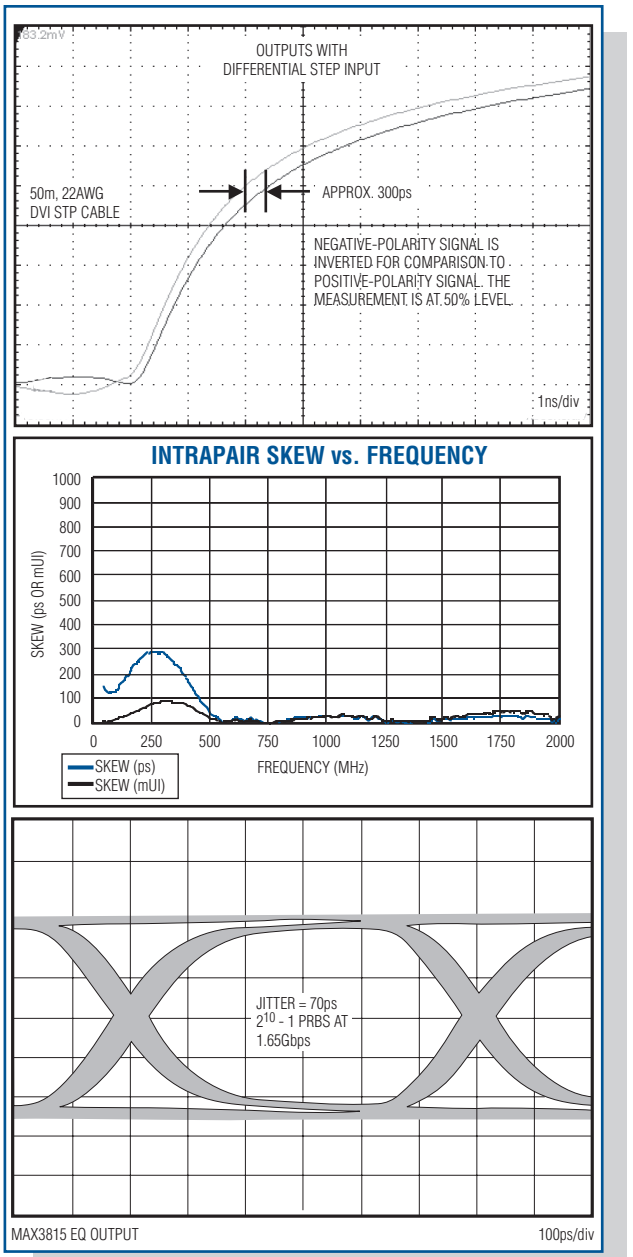


Figure 3. Step method fails to predict serial data jitter.

Again, intrapair skew is a function of frequency in STP and twinax cables. **Figure 3**, for instance, shows measurements on a 50m 22AWG STP cable for DVI systems. Note that the step method predicts intrapair skew of 300ps, which is about one half period (0.5UI) at the 1.65Gbps video rate necessary for WUXGA displays. The cable, therefore, fails intrapair skew requirements for the DVI/HDMI standards. Yet, the receiver's equalized eye diagram looks great, because the high-frequency intrapair skew is very low in this cable, allowing excellent performance at 1.65Gbps. The step method only examines low-frequency intrapair skew. So, do not throw that cable away!

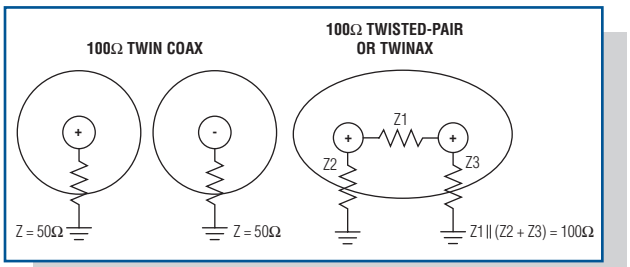


Figure 4. Uncoupled (twin coax) and coupled (twinax, STP) 100Ω differential pairs.

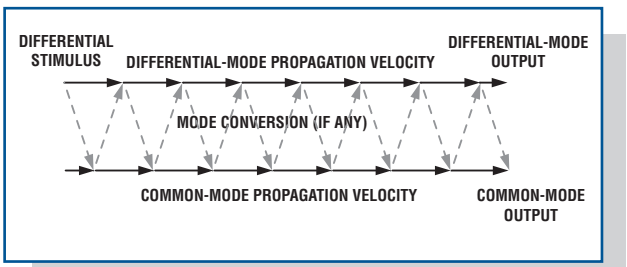


Figure 5. Illustration of mode conversion along cable length.

Coupled Differential Pairs

As shown in **Figure 4**, coupled cables (STP, UTP, twinax) derive their differential characteristic impedance both from coupling between the (+) and (-) lines of a pair (Z1), and coupling of each side to ground (Z2, Z3). Any imbalance in a differential pair, such as asymmetry of length, or twist, or dielectric environment (in which Z2 ≠ Z3), causes a differential-to-common-mode conversion with measurable symptoms, such as intrapair skew.

As a further complication in coupled cables, the differential- and common-mode signals have different propagation velocities, which can amount to several nanoseconds of difference over the length of a long cable. As the differential energy converts to common-mode and back again, it returns with arbitrary phase. This effect is one source of differential-mode jitter. When the signal is able to convert freely between the two modes, the cable frequency and phase responses are no longer predictable.

Differential- and common-mode signals also have different loss rates (in dB/m) due to the skin effect. This behavior is not all bad, because it can be used to advantage: a cable whose common-mode loss is significantly higher than its differential-mode loss has little intrapair skew. A cable with no common-mode energy at the output end has no intrapair skew at all. As an extreme example, any high-frequency common-mode energy in a CAT5 UTP cable dissipates as EMI (because it has no shield), leaving only differential-mode energy. Again, there is no intrapair skew.

Predicting Jitter from Differential-to-Common-Mode Conversion

The simple model of double conversion (differential mode to common mode and back) serves well here, though it is clearly a lumped approximation of a continuous process. Mode conversion is progressive and can be partial or multigenerational, depending on the cable length relative to wavelength **(Figure 5)**.

Note that common-mode energy by itself does not impart timing jitter to differential signaling. Rather, mode conversions corrupt the signal by permitting a return of incoherent signals back into the differential mode. So, the measurement of common-mode energy (given a differential stimulus) provides evidence for mode conversion, from which we can then estimate the differential-mode jitter.

A measurement of cable quality should be predictive of digital-video signaling quality. For instance, it should predict zero-crossing jitter in the data, which is the residual jitter that remains due to cable imbalances after an ideal equalization of skin-effect and dielectric losses in the receiver. Intrapair skew measurements using the step stimulus are inadequate for predicting jitter.

We therefore propose the measurement of differential-to-common-mode conversion as a better predictor of data-jitter contribution from cable imbalance. Ideally, only differential-mode, and not common-mode, energy remains at the cable output. If common-mode energy is present, the cable has some imbalance and has converted some differential energy to common mode.

As a heuristic justification, we can use a simple model that has a sine-wave differential source at the cable input.

1) Assume that a fraction of the sine-wave energy is converted from differential to common mode in the cable, and by symmetry the same fraction is converted back to differential mode. Using S-parameter naming conventions, the two conversion factors are SCD21 and SDC21, respectively (note that output ports are named first):

- SCD21 is differential-mode to common-mode conversion from Port 1 to Port 2
- SDC21 is common-mode to differential-mode conversion from Port 1 to Port 2
- SCD21(magnitude) = SDC21(magnitude) is a good approximation in real-world cables
- SDD21 is differential-mode transfer from Port 1 to Port 2

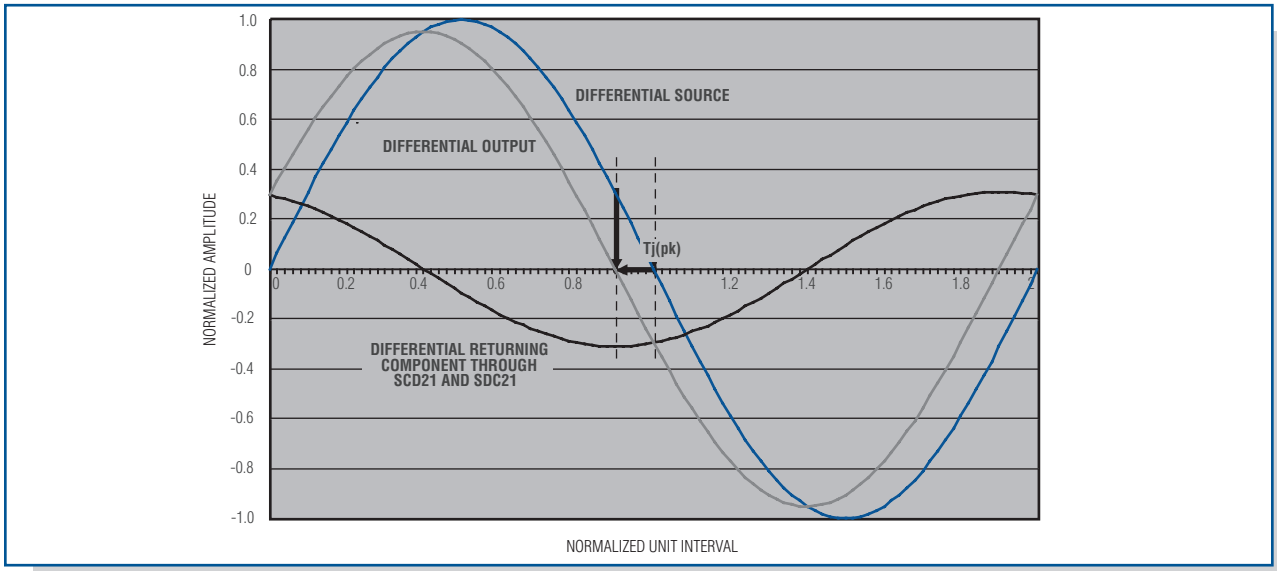


Figure 6. Offset in the zero-crossing time TJ(pk) is caused by SCD21 and SDC21. All waveforms shown are differential signaling (single ended not shown).

2) Assume that the energy making the full conversion (from differential to common mode and back) returns with arbitrary phase. This behavior results from differences in the propagation velocity between differential and common modes, which is typical in STP and twinax. It also assumes a cable of sufficient length to exhibit a delay difference greater than the sine period.

The zero crossing of a differential sinusoidal component can be shifted by TJ(pk), due to a returning version of itself through SCD21 and SDC21 (**Figure 6**). Note the returned differential component, whose maximum amplitude at the zero crossing of the differential output signal causes the worst-case skew. The returned amplitude, A(dB), required to introduce TJ(pk) jitter relative to the total differential output level (SDD21) is:

Eq. 1

$$A(dB) = [SCD21(dB) - SDD21(dB)] + [SDC21(dB) - SDD21(dB)]$$

$$= 20 \times LOG\{\sin[2\pi \times TJ(pk) \times Frequency]\}$$

Because a good approximation for real-world cables is SCD21(magnitude) = SDC21(magnitude), the difference between common-mode and differential-mode levels at the cable output lets you measure the quality of a cable that imparts less than TJ(pk-to-pk) jitter due to imbalance:

Eq. 2

$$SCD21(dB) - SDD21(dB) = A(dB)/2$$

$$< 10 \times LOG\{\sin[\pi \times TJ(pk\text{-}to\text{-}pk) \times Frequency]\}$$

Where added jitter due to imbalance is:

$$TJ(pk\text{-}to\text{-}pk) = 2 \times TJ(pk)$$

Figure 7 shows the common- and differential-mode responses of a cable, and **Figure 8** plots their difference, showing common-mode relative to differential-mode outputs. Figure 8 also includes templates for 0.1UI and 0.2UI (lines of constant error in the differential zero-crossing TJ[pk]), where UI is the unit interval for the bit period at the given data rate. For example, the 0.1UI jitter line calculated for 1.65Gbps (WUXGA) represents a constant maximum zero-crossing error of $60ps_{P\text{-}P}$.

Template Interpretation and Simplification

If the cable measurement in Figure 8 (SCD21 - SDD21) reaches the 0.1UI line at any point, cable imbalance creates a potential for $0.1UI_{P\text{-}P}$ jitter. That is, if a spectral component in the data-signaling sequence coincides with a frequency at which the cable measurement touches the $0.1UI_{P\text{-}P}$ template, the zero-crossing error (phase-shift range) for that spectral component is $0.1UI_{P\text{-}P}$ ($60ps_{P\text{-}P}$).

DVI and HDMI TMDS® signaling is not scrambled, so the harmonic content of its frequency spectrum changes according to data content. It is, therefore, reasonable to assume that the entire spectrum will get "exercised" over time, with dominant components falling roughly between (data rate)/20 and (data rate) x 0.8. (Note that the $sinc^2$ power function of an NRZ data signal goes to zero at frequency = data rate.)

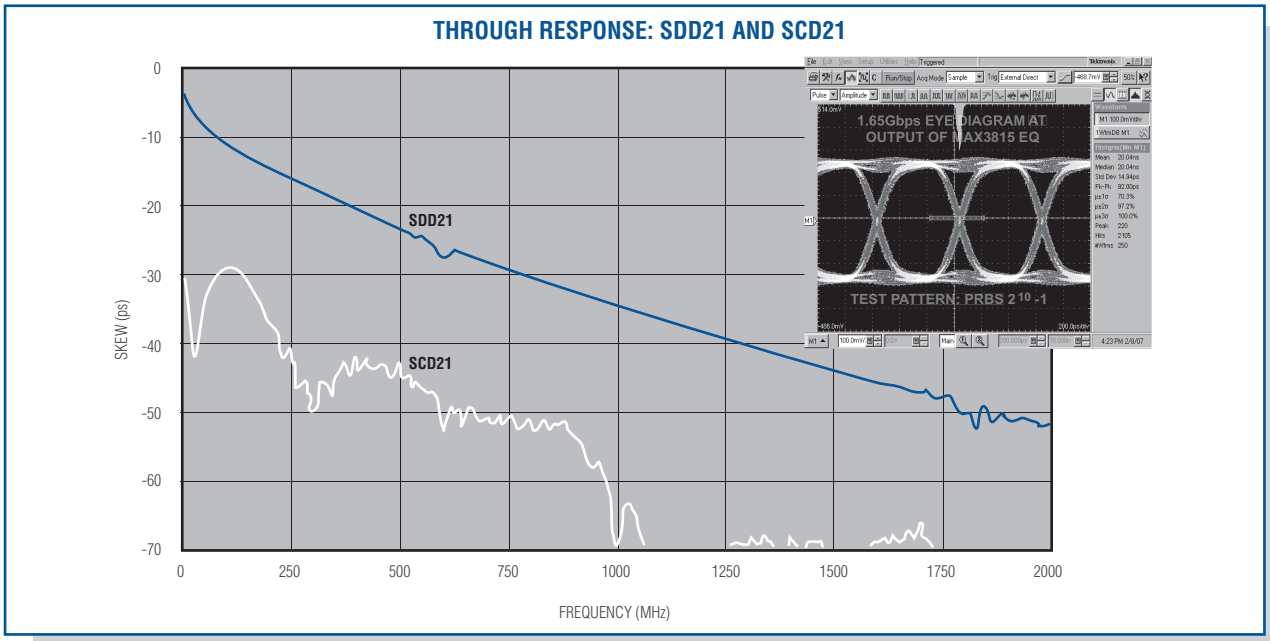


Figure 7. Frequency response of a 60m cable, showing common-mode output (SCD21) and differential-mode output (SDD21). Data is gathered on the MAX3815 TMDS digital-video equalizer.

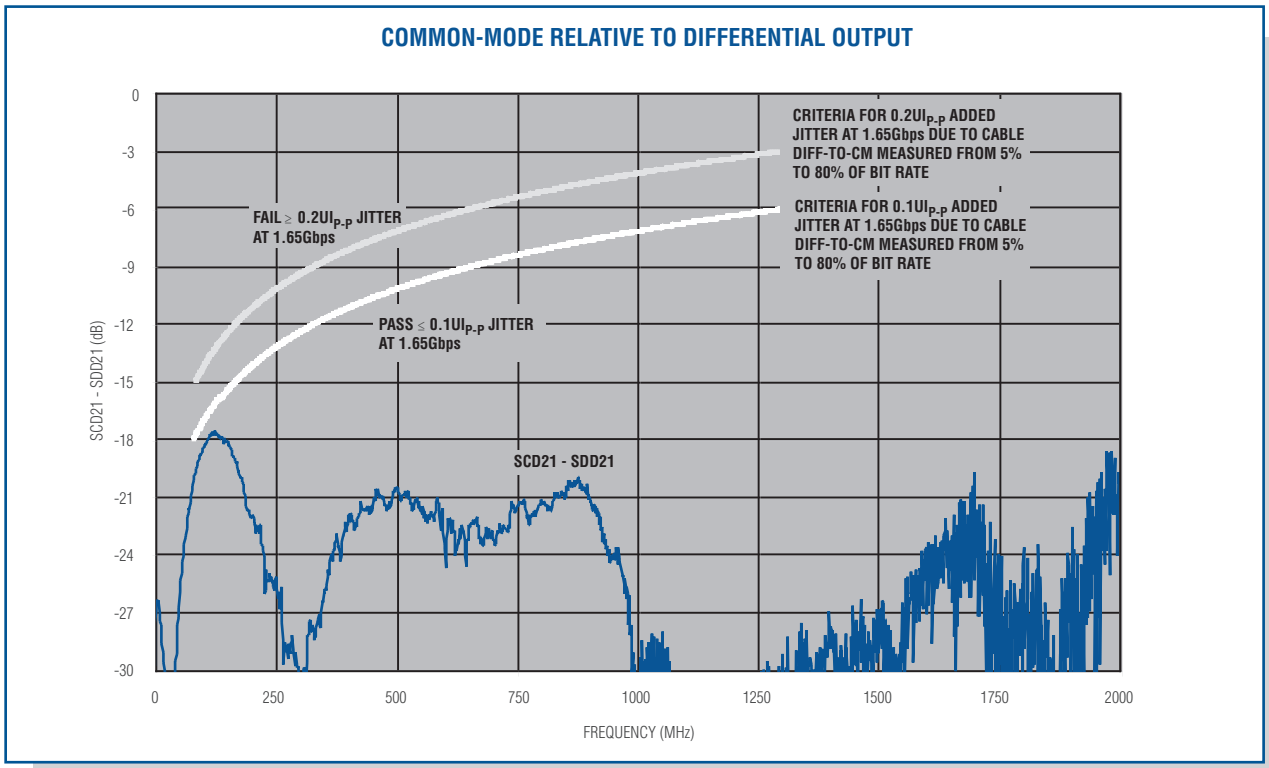


Figure 8. Plot of (SCD21 – SDD21) difference, with pass/fail template superimposed.

Figure 9 shows a simplified pass/fail template, derived from the formula in Eq. 2. The $0.1UI_{P-P}$ template is -11dB from 0.05 to 0.25 times the maximum bit rate, and a flat ramp up to -6dB at 0.8 times the maximum bit rate. The template simply scales with the maximum operating bit rate specified for the cable (1.65Gbps, in this case).

This simplified template also takes into account harmonic support for fundamentals less than 0.25 times the max bit rate. **Figure 10** shows the underlying formula curve (fundamental only), as well as the offsets for 2-component and 3-component mitigation of jitter at low frequency.

NRZ data patterns with fundamentals below 0.25 times the max bit rate contain harmonics that help mitigate the errant return of a single component that has suffered mode conversion. Fundamentals above 0.25 times the max bit rate are likely not to have harmonics that matter, because the frequency response of equalizer and receiver circuits typically rolls off above 0.75 times the max bit rate (i.e., the 3rd harmonic of the fundamental at 0.25 times the max bit rate).

Numerous tested cables exhibit maximum jitter potential at a single worst-case frequency. In conjunction with the signal's varying harmonic content, this effect supports the assumption of a single worst-case tone for the template.

Use $0.1UI_{P-P}$ Pass/Fail Template Line, or Better

The allowed jitter budget for a DVI/HDMI TMDS cable interconnect (including connectors and equalization) is roughly $0.2UI_{P-P}$ total added jitter, which is the difference between a TMDS Tx mask and Rx mask. The $0.2UI_{P-P}$ template lines just meet this criteria, and allow no room for other jitter contributors in the channel.

Hence, the $0.1UI_{P-P}$ pass/fail template line in Figure 10 is the basic recommended criterion, given its margin for other jitter contributors in the channel—such as connectors and residual jitter from equalization and switching. Tighter criteria are possible for premium cable performance; you could use a $0.05UI_{P-P}$ pass/fail template, for example.

Measuring the Conversion from Differential Mode to Common Mode

We recommend direct measurements of differential-to-common-mode conversion (SCD21), relative to the differential through response (SDD21), as the most diagnostic, flexible, and economical test method. The objectives are:

1) Test results that are predictive of NRZ signaling with equalized jitter performance

2) An economical test method—it should not require expensive oscilloscopes or network analyzers

3) A simple pass/fail test template

A 4-port S-parameter network analyzer configured as a 2-port differential analyzer (**Figure 11**) measures SDD21 and SCD21 directly, but its price ($50k to $100k) does not satisfy the second objective above. As an alternative, you can measure SDD21 and SCD21 accurately using a low-cost test setup (**Figure 12**) that consists of a sine generator, two baluns, and two power meters (or one 2-input power meter). These items have been around awhile, so you can easily stay under $10k by taking advantage of the used-equipment market.

Key components in this test setup are the model H9-SMA couplers from M/A-COM (a division of Tyco Electronics®), specified from 2MHz to 2GHz. The first coupler generates the differential source signal from a single-ended sine-wave generator, while the second coupler separates differential- (SDD21) and common-mode (SCD21) signals for measurement.

Use good quality SMA cables, and matched-length pairs where indicated. SMA-to-DVI/HDMI test boards are available from Tektronix® and Agilent™. Measure (SCD21[dB] - SDD21[dB]) across the frequency range of interest, and then plot it against the pass/fail templates.

Conclusion

Digital-video data can be recovered from long cables using inexpensive receive electronics, provided that the cables impose little or no differential-to-common-mode conversion. Such cables exhibit predictable phase delay and loss across the frequency spectrum, which is easily compensated. This statement is not true if the cable has excessive differential-to-common-mode conversion.

Intrapair skew is widely misunderstood as a measure of quality for the STP and twinax cables used in DVI, HDMI, and DisplayPort digital video. Beware that the traditional methods for measuring intrapair skew using a step stimulus give misleading answers for the purpose of separating good from bad cables for serial-digital video. Thus, a direct measurement of the key culprit—differential-to-common-mode conversion resulting from cable imbalance—is recommended as the most direct, flexible, and economical test method.

The author would like to thank Chad Nelson for his invaluable assistance in setting up the test beds and taking all the measurements used to confirm the performance results.

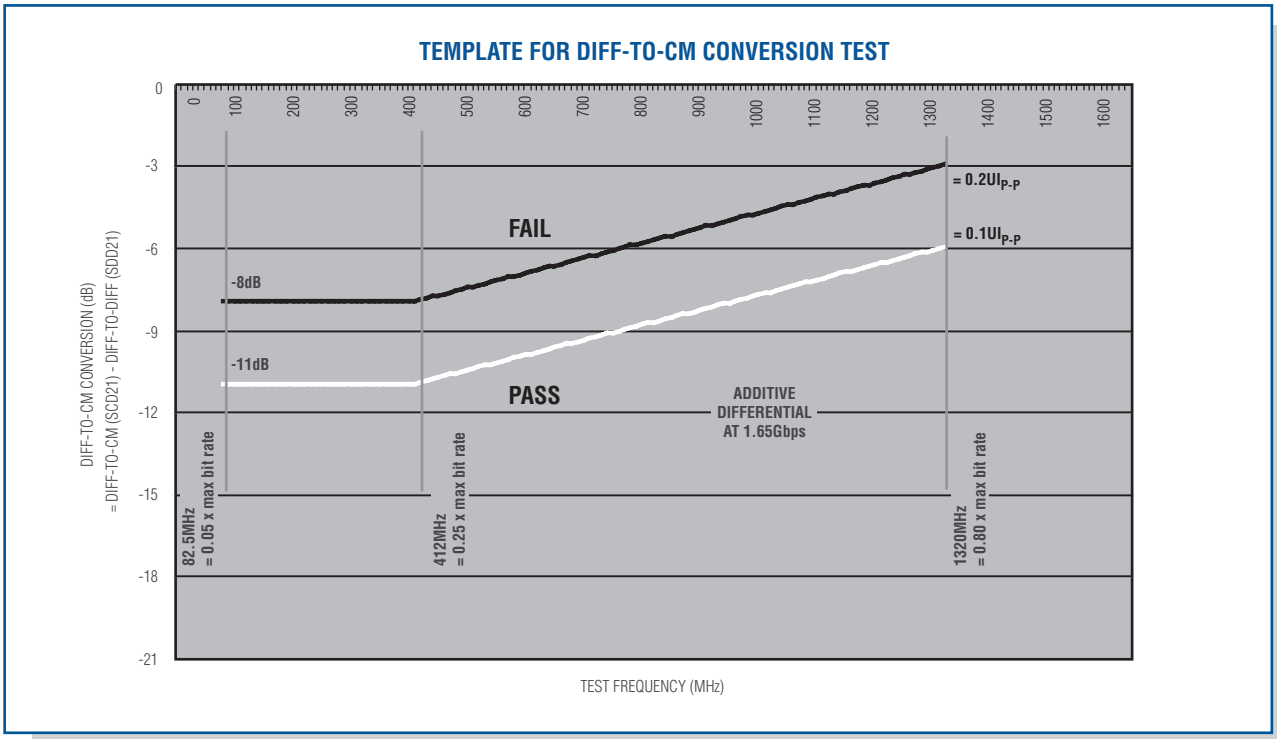


Figure 9. Simplified test template, for which $0.1UI_{P-P}$ pass/fail criteria are recommended.

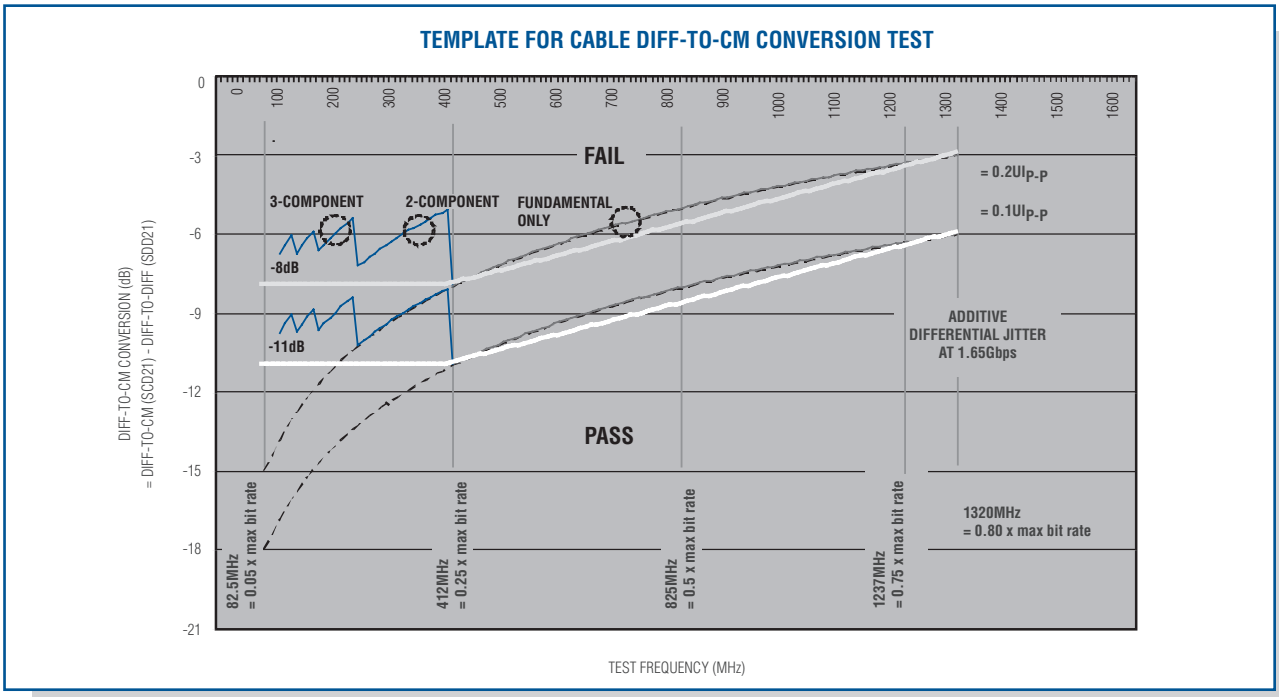


Figure 10. Simplified test template, with underlying family of curves shown for fundamental-only and multiple-harmonic cases.

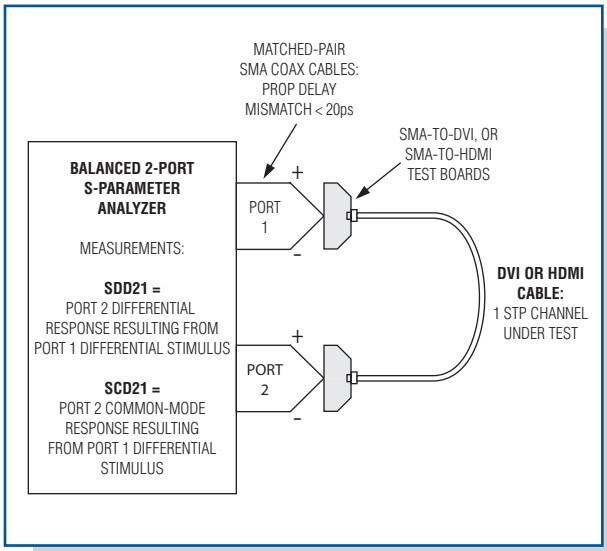


Figure 11. This 4-port S-parameter network analyzer is configured as a balanced 2-port analyzer.

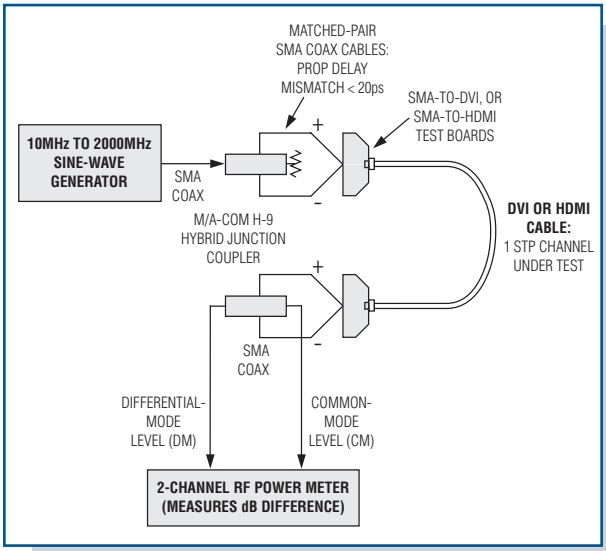
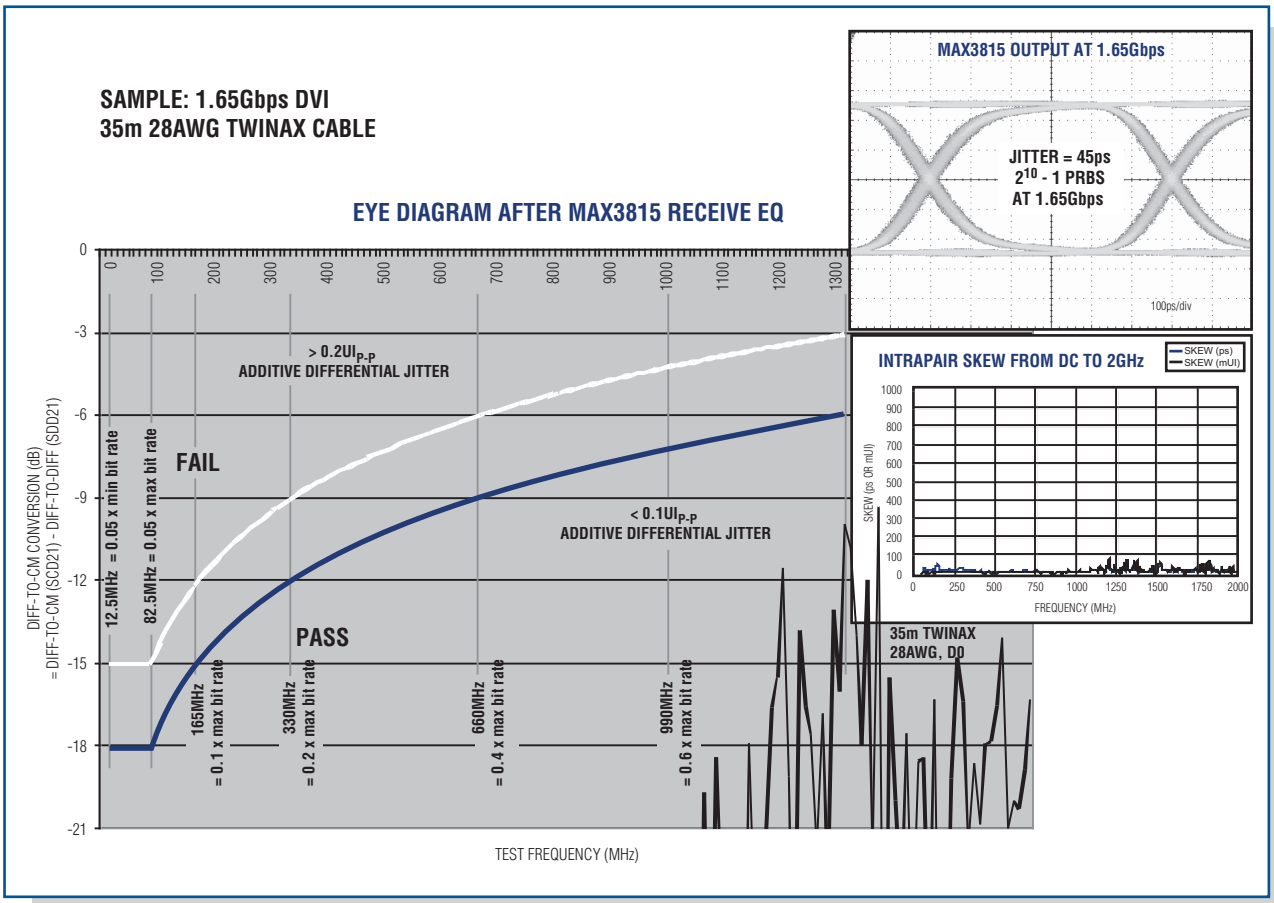
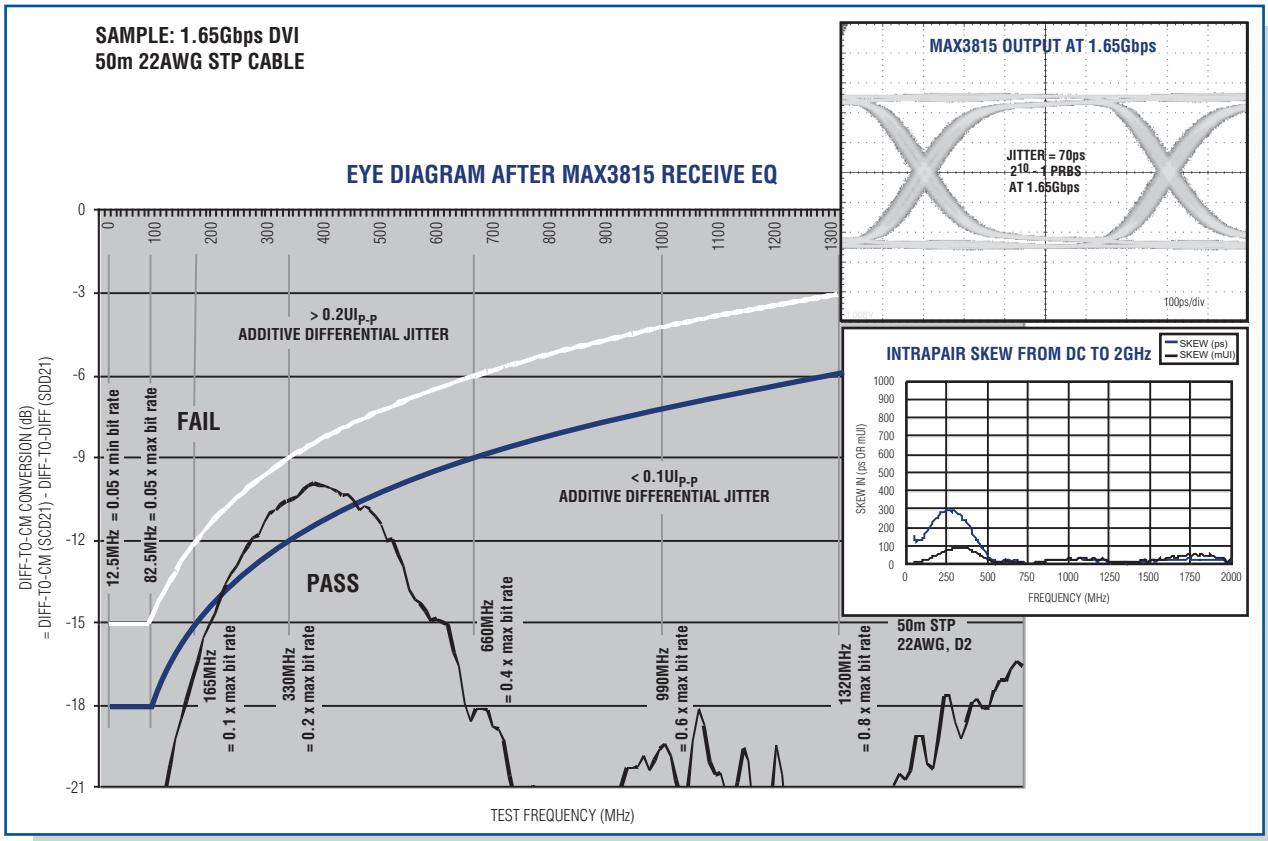
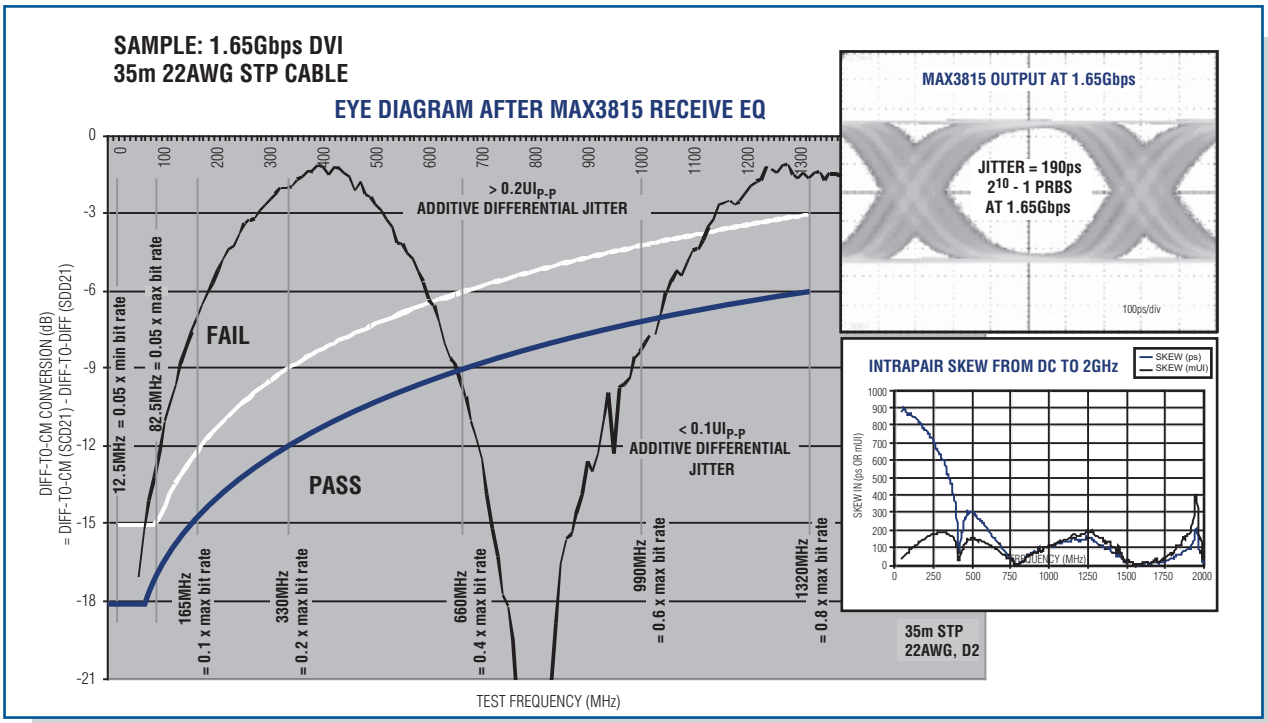


Figure 12. This test setup features a low-cost generator, couplers, and power meters.

Appendix: Real Cables Tell the Story




SAMPLE: 1.65Gbps DVI
50m 22AWG STP CABLE
EYE DIAGRAM AFTER MAX3815 RECEIVE EQ
MAX3815 OUTPUT AT 1.65Gbps
JITTER = 70ps
2^10 - 1 PRBS
AT 1.65Gbps
100ps/div
INTRAPAIR SKEW FROM DC TO 2GHz
SKEW (ps)
SKEW (mUI)
SKEW IN (ps OR mUI)
FREQUENCY (MHz)
> 0.2UI P-P
ADDITIVE DIFFERENTIAL JITTER
< 0.1UI P-P
ADDITIVE DIFFERENTIAL JITTER
FAIL
PASS
12.5MHz = 0.05 x min bit rate
82.5MHz = 0.05 x max bit rate
165MHz = 0.1 x max bit rate
330MHz = 0.2 x max bit rate
660MHz = 0.4 x max bit rate
990MHz = 0.6 x max bit rate
1320MHz = 0.8 x max bit rate
50m STP
22AWG, D2
DIFF-TO-CM CONVERSION (dB)
= DIFF-TO-CM (SCD21) - DIFF-TO-DIFF (SDD21)
TEST FREQUENCY (MHz)


SAMPLE: 1.65Gbps DVI
35m 22AWG STP CABLE
EYE DIAGRAM AFTER MAX3815 RECEIVE EQ
MAX3815 OUTPUT AT 1.65Gbps
JITTER = 190ps
2^10 - 1 PRBS
AT 1.65Gbps
100ps/div
INTRAPAIR SKEW FROM DC TO 2GHz
SKEW (ps)
SKEW (mUI)
SKEW IN (ps OR mUI)
FREQUENCY (MHz)
> 0.2UI P-P
ADDITIVE DIFFERENTIAL JITTER
< 0.1UI P-P
ADDITIVE DIFFERENTIAL
JITTER
FAIL
PASS
12.5MHz = 0.05 x min bit rate
82.5MHz = 0.05 x max bit rate
165MHz = 0.1 x max bit rate
330MHz = 0.2 x max bit rate
660MHz = 0.4 x max bit rate
990MHz = 0.6 x max bit rate
1320MHz = 0.8 x max bit rate
35m STP
22AWG, D2
DIFF-TO-CM CONVERSION (dB)
= DIFF-TO-CM (SCD21) - DIFF-TO-DIFF (SDD21)
TEST FREQUENCY (MHz)

High-Frequency Losses in Long Cables

Skin-effect and dielectric loss are the dominant high-frequency loss mechanisms in a cable. Fortunately, commercial DVI/HDMI equalizer ICs (such as the MAX3815) are available to extend cable reach by economically compensating these losses.

Skin-effect loss (in dB) is proportional to cable length and to the square root of frequency. Dielectric loss (in dB) is proportional to cable length and frequency. Skin-effect loss dominates from low to mid frequencies, and dielectric loss dominates at high frequencies.

Such losses introduce jitter due to ISI (inter-symbol interference). An uncompensated loss of 6dB to 8dB at half the bit rate increases jitter, and lowers amplitude, to full closure of the eye diagram displayed on an oscilloscope. By compensating these losses, economical equalization can remove the ISI-related jitter and restore signal amplitude.

M/A-COM H9-SMA Hybrid Junction Coupler

Frequency Range: 2MHz to 2000MHz

Impedance: 50Ω

Transmission Through-Loss: 3.4dB to 4.8dB (see graph below)

Mode Isolation: 30dB (min, see graph below)

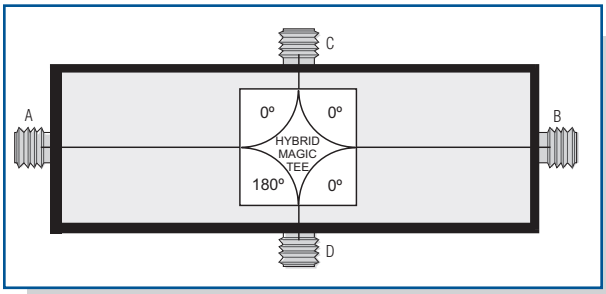
Application 1: Single-ended-to-differential converter

Port A: Single-ended stimulus input

Port B: Connect 50Ω termination

Port C: Differential (+) output

Port D: Differential (-) output



Application 2: Mode splitter (separate differential and common modes)

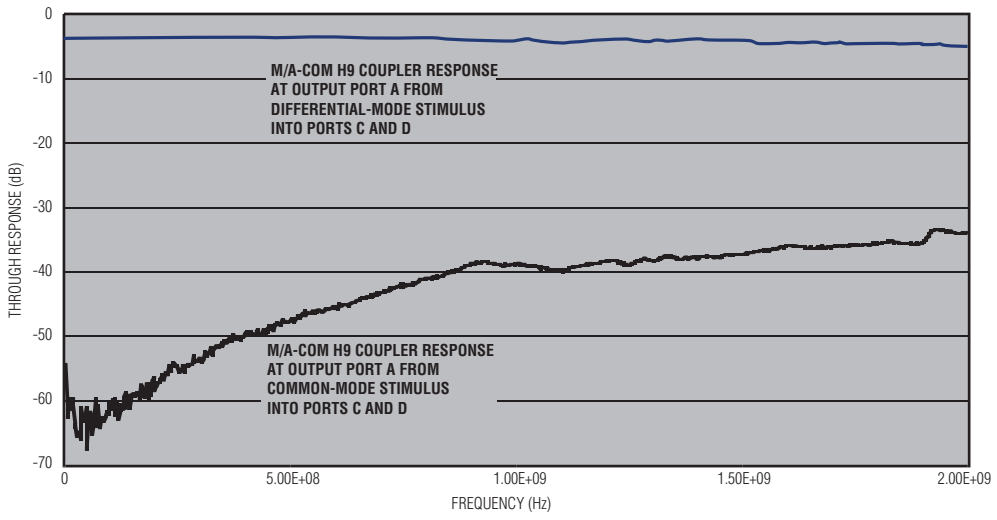
Port C: Differential (+) input

Port D: Differential (-) input

Port A: Differential level output (single ended)

Port B: Common-mode level output (single ended)

The plot below shows Application 2, with the outputs of ports A and B in response to inputs at ports C and D. The upper line (port A) is the differential stimulus at ports C and D, and the lower line (port B) is the common-mode stimulus at ports C and D.



Negative Charge Pumps Achieve Inductor-Like Efficiency for WLED Backlights

By Jay Kim, Senior Scientist

Offering a small footprint and high light output, white LEDs (WLEDs) provide an ideal backlight solution for small color displays in cellular phones and other portable devices. WLEDs, however, do present one difficulty in devices powered from a single-cell lithium-ion (Li+) battery. The operating voltage from most Li+ cells is 3V to 4.2V, while a WLED's forward voltage is typically 3.5V to 3.8V (at 20mA). Consequently, the voltage output at the lower end of a Li+ battery's operating range is not enough to bias WLEDs.

Two approaches are commonly used to generate adequate forward bias for WLEDs: capacitor-charge-pump and inductor-based boost circuits. Inductor-based circuits are generally the best choice for efficiency and battery life. However, they require the addition of that costly inductor, and necessitate careful layout and design to avoid electromagnetic and radio-frequency interference issues. In contrast, charge-pump solutions are simpler to implement and cost less, but they have also typically been less efficient, which can reduce battery runtime.

With the advent of negative-charge-pump designs, new WLED driver ICs achieve inductor-like efficiencies (averaging 85%) while still retaining the simplicity and low cost of an inductorless design.

Efficiency Improvements Among Fractional-Ratio Charge Pumps

The first generation of WLED charge-pump solutions used a basic doubler topology (or 2x mode) at its core. The efficiency of a 2x charge pump is:

$$P_{LED}/P_{IN} = (V_{LED} \times I_{LED})/[(2 \times V_{IN} \times I_{LED}) + (I_Q \times V_{IN})]$$

Where I_Q is the circuit's quiescent operating current.

Because the I_Q is usually small when compared to the WLEDs' load current, the efficiency can be closely approximated by:

$$P_{LED}/P_{IN} \approx V_{LED}/(2V_{IN})$$

To improve efficiency, second-generation WLED charge pumps did not always drive the output to a whole multiple of the input. If the battery voltage was sufficient, an adequate WLED drive voltage could be generated with a 1.5x charge pump. The conversion efficiency of a 1.5x pump is:

$$P_{LED}/P_{IN} = (V_{LED} \times I_{LED})/[(1.5 \times V_{IN} \times I_{LED}) + (I_Q \times V_{IN})]$$
$$\approx V_{LED}/(1.5V_{IN})$$

As can be seen, the 1.5x pump substantially improves efficiency. With a 3.6V battery voltage and a 3.7V WLED, efficiency jumps from 51% with a 2x pump to 69% with a 1.5x pump.

Third-generation WLED drivers maximize efficiency even more. They employ a 1x transfer mode to connect the battery directly to the WLEDs through low-dropout current regulators when the battery voltage is high enough to drive the WLEDs. The efficiency of a 1x transfer mode is:

$$P_{LED}/P_{IN} = (V_{LED} \times I_{LED})/[(V_{IN} \times I_{LED}) + (I_Q \times V_{IN})]$$
$$\approx V_{LED}/(V_{IN})$$

When the battery voltage is sufficient to directly drive WLEDs, 1x mode efficiency can be over 90%. With a 4V battery and a 3.7V WLED, efficiency is 92%.

Maximizing Efficiency at Each Battery Voltage

An optimum WLED driver design employs the most efficient power-transfer mode possible for a given battery and LED voltage. The design also changes modes as the battery (or WLED) voltage changes. However, switch losses can force the circuit into a less efficient mode at a higher battery voltage than might otherwise be necessary. It is always best for the driver to stay in a high-efficiency mode as long as possible while the battery voltage falls. However, this performance requires minimum loss in the power switches and, consequently, more space and cost.

As noted above, the best conversion efficiency is offered by a 1x transfer mode, but this mode can only be used when the battery voltage is more than the WLEDs' forward voltage (V_F). The key to utilizing 1x mode for the lowest possible battery voltage has usually focused on lowering both the voltage drop of the 1x mode bypass FET and that of the current regulator. These voltage drops determine the series losses and minimum input voltage that can sustain 1x mode. The minimum battery voltage required by 1x mode is:

$$V_{IN(MIN\_1x)} = (V_{LED} + \text{Bypass pFET } R_{DS(ON)}) \times (I_{LED} + V_{DROPOUT} \text{ of the current regulator})$$

A traditional positive-charge-pump WLED solution uses a pFET bypass switch to connect the battery voltage to the

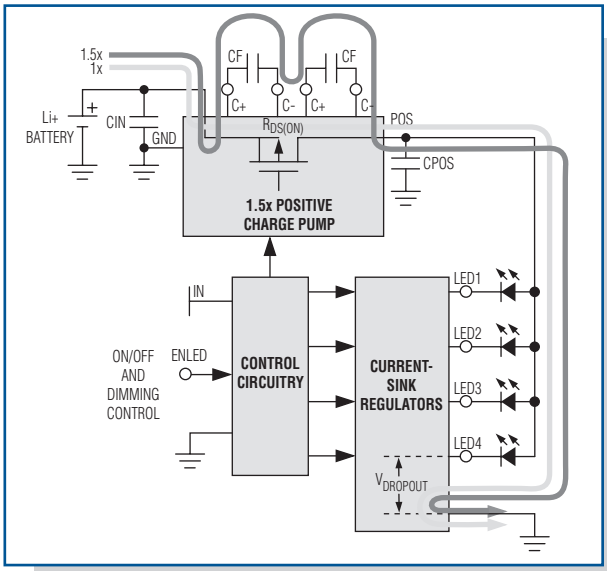


Figure 1. In 1x mode, the positive charge pump uses an internal switch to bypass V_{IN} to the WLEDs' anodes.

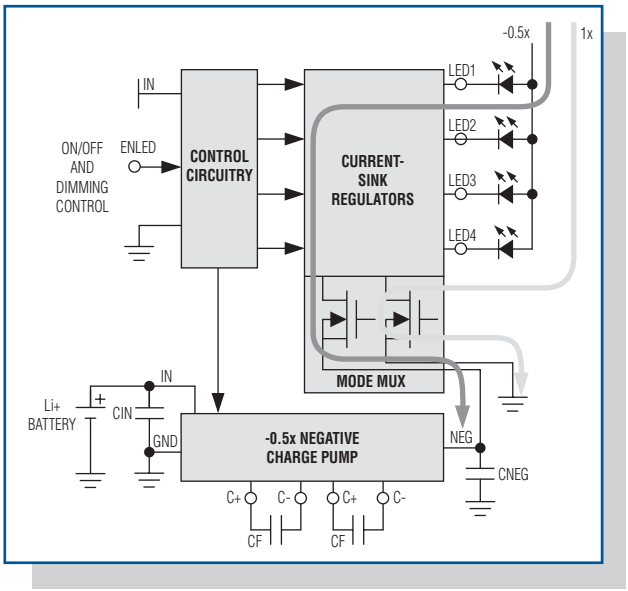


Figure 2. Individual switchover for each WLED is possible when the driver switches to its negative-charge-pump mode, which improves overall efficiency.

WLEDs, as shown in **Figure 1**. This FET's $R_{DS(ON)}$ is typically 1Ω to 2Ω. Further resistance reductions are limited since lower resistances typically would necessitate a larger FET, increasing the cost of the power device.

A positive charge pump generates 1.5x V_{IN} or 2x V_{IN} to drive the WLED anodes when V_{IN} is insufficient to drive a 1x transfer mode. To implement the 1x mode in a positive-charge-pump architecture, we must use an additional internal switch to route V_{IN} directly to the WLEDs' anodes, thereby bypassing the charge pump.

A negative-charge-pump architecture also generates -0.5x V_{IN} to drive WLED cathodes when V_{IN} is insufficient for the task. This architecture, however, does not require that you bypass the -0.5x V_{IN} charge-pump output to ground in 1x mode because current regulators control the WLEDs' current directly from V_{IN} to ground. As a result, the negative-charge-pump architecture extends 1x mode all the way down to:

$V_{IN(MIN\_1x)} = V_{LED} + V_{DROPOUT}$ of the current regulator

Figure 2 shows the current path of 1x mode with a negative charge pump. The circuit does not require a pMOS bypass switch, and it directly regulates WLED current from V_{IN} to ground. If I_{LED} is 100mA total (i.e., 5 WLEDs x 20mA), a 2Ω pMOS bypass switch's voltage drop would be 200mV. As it discharges, the Li+ battery voltage holds relatively stable around the 3.6V to 3.8V (typical) voltage range. Assuming a typical Li+ battery-discharge curve, the 200mV increase in operating voltage enabled by 1x mode dramatically improves efficiency.

Maximizing Efficiency at Each LED Forward Voltage

In a traditional 1x/1.5x positive-charge-pump WLED driver, the WLED anodes connect to the charge pump's output. If the WLEDs are mismatched, the driver must switch to 1.5x mode when there is not enough (V_{IN} - V_{LED}) headroom to support the worst forward-voltage WLED.

With the negative-charge-pump architecture, it is no longer necessary to abandon the efficient 1x mode due to the bad forward voltage of only one WLED. As Figure 2 illustrates, the Mode Mux circuit individually selects 1x mode or -0.5x mode for each WLED, thereby maximizing overall efficiency.

The MAX8647/MAX8648 charge-pump drivers, for example, turn on the -0.5x charge pump when the input voltage is insufficient to drive the highest forward-voltage WLED. In this situation, the devices drive only the highest V_F WLED through the -0.5x negative rail (instead of ground), while the WLEDs with lower forward voltages remain in 1x mode.

To further improve efficiency, the MAX8647/MAX8648 provide individual mode switching for the WLEDs. This technology adaptively switches the WLEDs to -0.5x mode at different times and at different V_{IN} levels due to V_F mismatches or temperature changes (**Figure 3**).

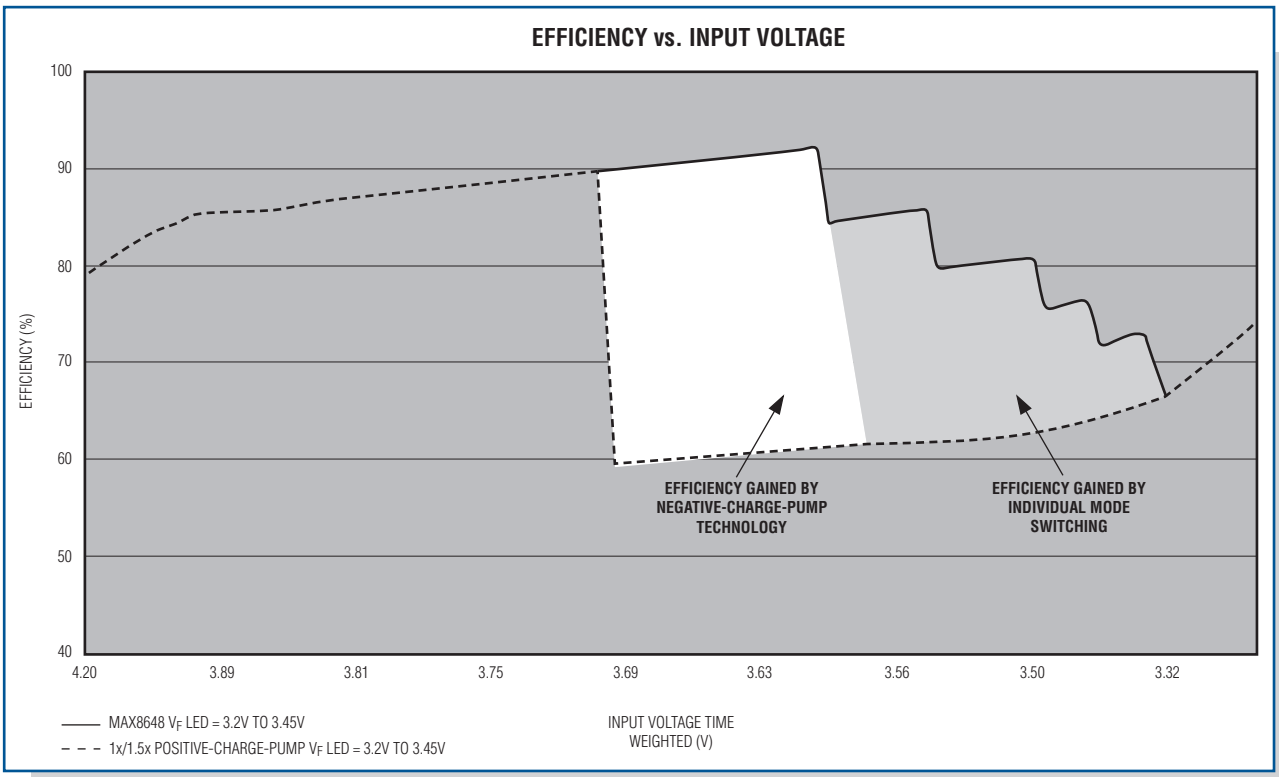


Figure 3. The efficiency of the MAX8647/MAX8648 charge-pump WLED drivers can be extended by switching to a negative-charge-pump mode and to individual mode switching for each WLED.

Summary

Traditionally, WLED backlight designs that employ charge pumps have been less efficient than inductor-based designs. A positive-charge-pump architecture switches from its highest efficiency mode (1x) when any single WLED current falls below a predetermined level. Thus, systems with a large number of WLEDs and large forward-voltage mismatch waste a significant amount of power.

A negative-charge-pump architecture overcomes the inefficiencies typically encountered in positive-charge-pump designs. Devices such as the MAX8647/MAX8648 use this negative-charge-pump architecture, as well as individual mode switching for each LED, to dramatically improve efficiency and extend battery runtime. These WLED drivers enable designers to achieve inductor-like efficiencies while benefiting from the simplicity and cost savings offered by charge-pump solutions.

Simplified Li+ Battery-Charger Testing

By Alfredo H. Saab, Applications Engineering Manager, and Shasta Thomas, Applications Engineer

Lithium-ion (Li+) batteries are more delicate than other battery chemistries and have little tolerance for abuse. Consequently, Li+ battery chargers are complex circuits, requiring highly accurate current and voltage settings. If these accuracy requirements are not met, the charger may fail to completely charge the battery, severely reduce battery life, or otherwise degrade battery performance.

Given the demands imposed on Li+ chargers, it is critical that charger designs be tested thoroughly and stepped through their entire operating range. However, testing a Li+ charger with its natural load (i.e., a Li+ battery) can be time consuming and impractical in laboratory and production environments. To simplify the process, this article presents a battery-emulation circuit for accelerated, realistic testing of Li+ battery chargers without actual batteries.

CC-CV Charging

The Li+ battery-charging process requires medium-accuracy constant-current (CC) charging in a first phase, transitioning to high-accuracy constant-voltage (CV) charging in a second phase.

Figure 1 illustrates the V-I characteristics of a modern CC-CV integrated circuit (the MAX1737) used for a Li+ battery charger. This type of IC is at the heart of all Li+ battery chargers in consumer products. The CC (between 2.6V and 4.2V battery voltage) and the CV (4.2V) regions are clearly shown.

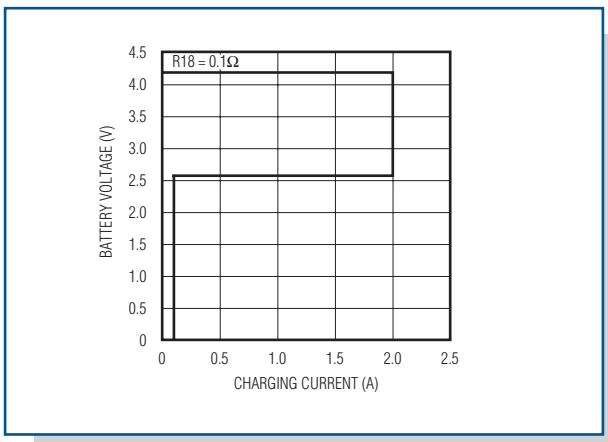


Figure 1. This V-I curve from the MAX1737 is typical for Li+ cell chargers.

The region below 2.6V requires a different charging technique. If charging is attempted on a battery discharged below 2.6V, the charger applies a low-value ("conditioning current") charging current until the battery reaches the 2.6V level. This is a safety mechanism made necessary by the behavior of Li+ batteries when overdischarged. Forcing a fast-charge current when V_{BATT} < 2.6V can cause the battery to go into an irreversible short-circuit condition.

The transition point from the CC to the CV phase has a critical tolerance of ±40mV. The reason for the narrow tolerance is that a lower CV will not allow the battery to acquire its full charge, and a higher one will reduce its useful life.

Charge-process termination involves sensing that the battery has reached its full charge and that the charger must be disconnected or shut down. This is accomplished by detecting, while in the CV phase, the point where the charge current is reduced to a fraction (usually < 10%) of the so-called fast-charge or maximum charge current.

Testing Parameters for Li+ Chargers

Li+ battery-charger designs usually have two basic building blocks: a digital block (control state machine) and an analog block, composed of a well-regulated current/voltage power supply with an accurate (better than 1%) reference. A complete test of a Li+ charger product (not just the IC) is a more involved and time-consuming task than just verifying a few current or voltage values.

Testing should step the charger through its entire operating range: through the CC phase, up to the transition from CC to CV, and on to charge termination. Recall that the most realistic condition for such a test is to use the natural load for the charger: a Li+ battery. However, using a Li+ battery to test a Li+ charger is time consuming because the charging process can take an hour or more. The test time varies widely, according to whether you combine a higher-capacity battery with a slow charger, a lower-capacity battery with a fast charger, or something in between.

The charging process cannot, moreover, be accelerated beyond a limit imposed by the battery's maximum charge rate (the so-called fast-charge current) without damaging the battery. For normal batteries used in consumer products, this current is rarely specified above 1C (the current needed to fully discharge the battery in one hour). Therefore, the time required to carry the charger through the full cycle will be longer than two hours, in most cases.

If the test needs to be repeated, you must discharge the battery in full—a process only slightly shorter than charging. Or, you must have available a supply of consistently discharged batteries.

An alternative to load testing with a real battery is to test the charger using a simulated but realistic load. This simulation should verify the circuit's DC response and dynamic stability. Battery simulation, however, is difficult to implement with the standard loads used in power testing. Unlike most bench loads for power-supply testing, batteries do not behave as resistances or constant-current sinks. As noted above, testing must also step the charger through its entire operating range. The Li+ charger test circuit outlined below satisfies all of these requirements.

Choosing a Battery-Modeled Load

Let us digress to discuss two modeling approaches that should be considered, but will then be discarded.

One approach to modeling a battery load is to use a voltage source capable of current sourcing (discharge) and sinking (charge) in series with a resistor that represents the battery's internal resistance. Because Li+ batteries demand precision limits for voltage termination and charge current, all Li+ chargers today are, in effect, regulated power converters.

Moreover, because the stability of a regulated power converter (the charger) depends on dynamic properties in the attached load (the battery), you must choose a load that closely resembles the characteristics of the model. Otherwise, testing may only verify the V-I limits in the charger itself.

Using a shunt voltage regulator with a resistor in series to simulate the battery's internal resistance may be adequate, if the test is a one-time task and the simplest of battery models satisfies the test requirements. This approach also offers the advantage of being powered by the charger itself.

More rigorous testing, however, requires a more elaborate model. This model uses an internal voltage source whose value is a function of the total electrical charge supplied to the battery during the charging process.

The voltage between the terminals of a battery being charged at constant current varies continuously and with a positive slope. This behavior is caused by the progressive reduction of depolarizing ions accumulated around the battery's cathode during discharge and other chemical processes internal to the battery. As a result, the charger's operating point depends on the length of time that it has been connected to the battery, as well as the battery's past history. A load that simulates this more complex model is harder to set up using the general-purpose instruments found in most electronics labs.

When charging circuits must be tested often, or when circuit performance must be characterized in detail, a circuit that closely simulates the battery under charge is a useful bench accessory. The simulation should sweep continuously through all DC operating points possible for the charger. The circuit should also display the results so that operators can search for problems, glitches, and oscillations. If the simulator provides outputs for the battery voltage and signal, these results can be presented directly as a scope shot.

The test can be accelerated (from hours to tens of seconds) and repeated as many times as necessary, making it much more convenient than tests with a real battery. Accelerated tests are not adequate, however, for determining the thermal effects of power stress on the charger circuits. Therefore, you may need to conduct additional tests over a longer period to accommodate thermal time constants in the charger's power and regulation circuits.

Building the Battery-Modeled Load

The circuit in **Figure 2** simulates a single-cell Li+ battery. Both the termination voltage and the fast-charge current sourced during the charger's CC phase are commanded by settings on the charger. The internal battery voltage is set at 3V when the simulator is initialized to the fully discharged condition, but that level can be raised to 4.3V for testing an overcharge condition. The 3V initialization is typical for the low-battery shutdown circuits used to terminate the discharge of Li+ batteries. This design is intended for use with standard, CC-CV type Li+ battery chargers that terminate the charge at 4.2V. The design can easily be adjusted to accommodate nonstandard levels of termination voltage and fully discharged voltage.

The charger under test drives the simulator with charging currents as high as 3A, subject to a limit set by dissipation in the power transistor. The battery-voltage increase simulated by the Figure 2 circuit is a function of all the charging current integrated by the circuit from the moment the simulator is set to the fully discharged state.

With the values shown and a 1A charging current, the integrating time constant allows the simulator to reach the charger's 4.2V limit in six to seven seconds. This simulation of current range, internal resistance, charge-termination voltage, and fully discharged voltage is based on the specifications of a typical Li+ cell—in this case, the Sony® US18650G3. The simulated battery voltage does not include a simulation of ambient-temperature effects.

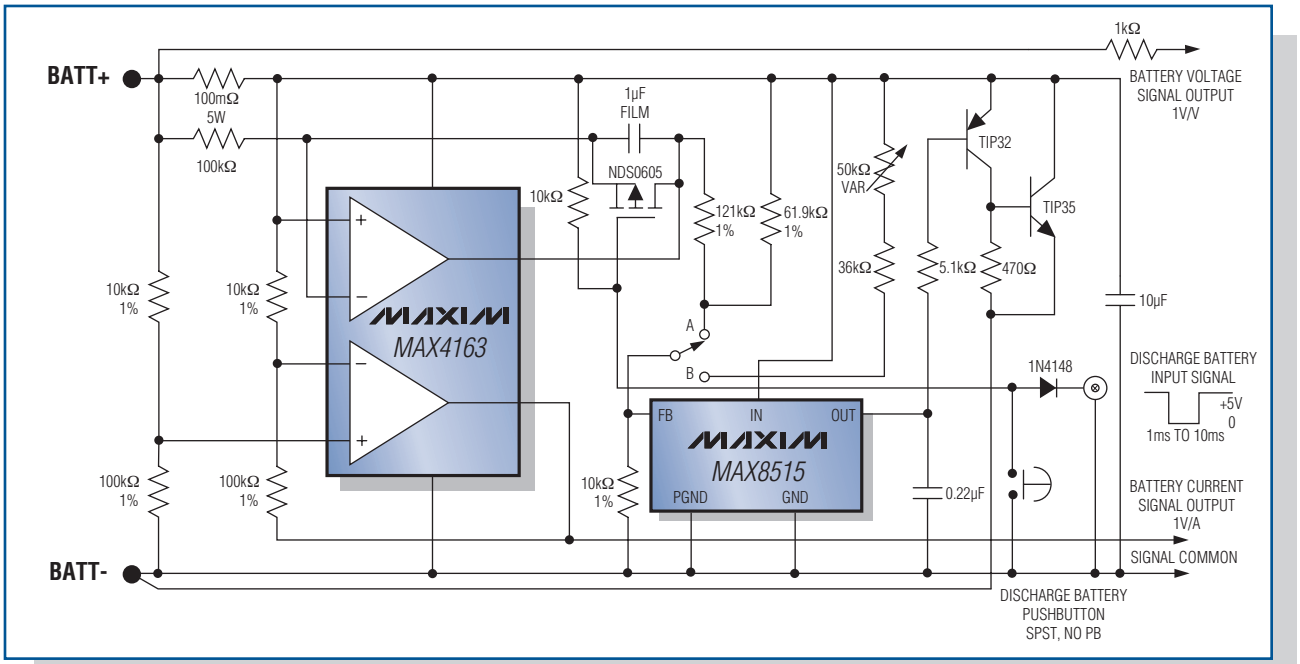


Figure 2. By simulating the behavior of a single Li+ cell under charge, this circuit lets you test Li+ battery chargers without using real batteries.

The shunt voltage regulator is designed around a MAX8515 shunt regulator and a pair of bipolar power transistors. (This regulator was selected for the accuracy of its internal voltage reference.) The high-current TIP35 transistor is attached to a heatsink capable of dissipating about 25W.

One half of the MAX4163 dual operational amplifier integrates the charge current, while the other half amplifies and level shifts the current-measurement signal. The operational amplifiers' high PSRR and rail-to-rail input and output ranges simplify the circuit design for both functions. Note that the 0.100Ω current-sense resistor, in series with the positive side of the battery simulator, also serves as the battery's internal resistance.

The simulator can be reset to the fully discharged state by an external signal when operating in a system with automated test-data acquisition. Alternately, it can be reset by a pushbutton when the test setup is manually operated.

A single-pole, single-throw switch lets you choose from two modes of operation for the simulator. In position A, the switch operates as an integrating charge simulator as described. In position B, it assumes a set output voltage and sinks current as necessary for spot-testing a charger at a fixed DC operating point. For that purpose, the "set" voltage can be manually adjusted between 2.75V and 5.75V by the 50kΩ variable resistor. These set-voltage values refer to the internal sinking source. The voltage actually measured between the simulator terminals (V_{BATT}) equals the set voltage plus a drop caused by the sink current flowing in the simulator's internal resistance (the 0.100Ω resistor). All the power necessary for operating the simulator comes from the battery charger's output.

Simulator Performance

Figure 3 shows the typical V-I waveforms obtained while simulating the charging of a Li+ battery up to 4.2V. Two test runs are shown: one with an initial fast-charge current of 1A (traces B and D), and one with a fast-charge current of 2A (traces A and C). In both cases, the CC phase continues until the termination voltage reaches 4.2V. After that point, current decays exponentially while the simulated battery voltage remains constant. The shorter time to termination for the 2A run is just what you would expect after doubling the charging current for a real battery. Notice, however, that doubling the current does not halve the total charge time; it only halves the time required to reach CV mode, as is the case with a real battery.

Figure 4 shows the V-I curves obtained when sinking current at two different set voltages: 3V and 4.1V. For both curves, the dynamic resistance (indicated by slope) is simply the internal resistance simulated by the 0.100Ω resistor.

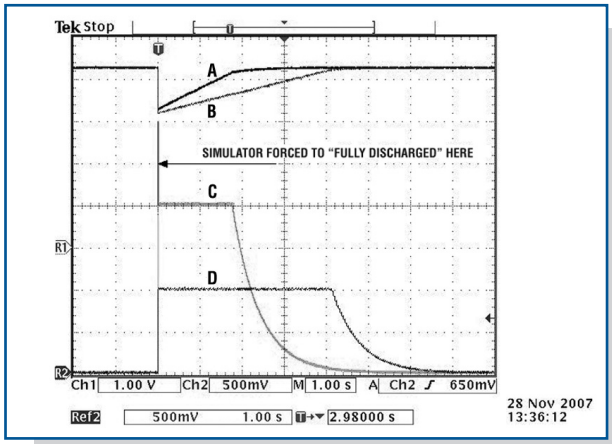


Figure 3. Taken from the Figure 2 cell-simulator circuit, these fast-charge waveforms show the behavior of a battery charger delivering 1A during the CC phase (traces B and D) and then 2A (traces A and C).

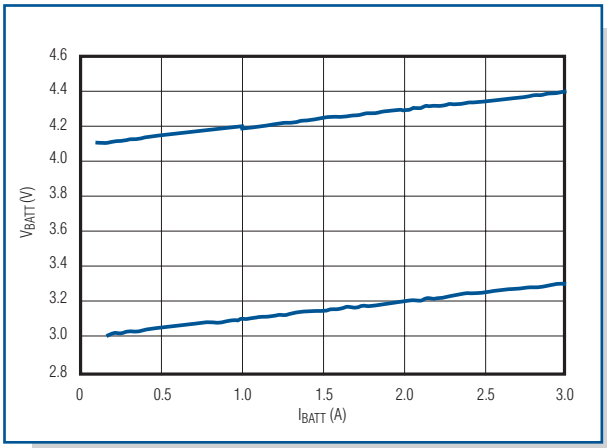


Figure 4. The slope of these plots, which represent the Figure 2 circuit sinking current at 4.1V (top trace) and 3V (bottom trace), shows the 0.1Ω internal resistance in both cases.

Summary

Because the charging process for Li+ batteries can take an hour or longer, testing a Li+ battery charger using its natural load is time consuming and frequently impractical. To speed battery-charger testing, this article presents a simple circuit for simulating the behavior of a Li+ battery. This circuit provides an efficient means of testing Li+ chargers without using real batteries.

A similar article appeared in the May 2008 issue of Power Electronics Technology.

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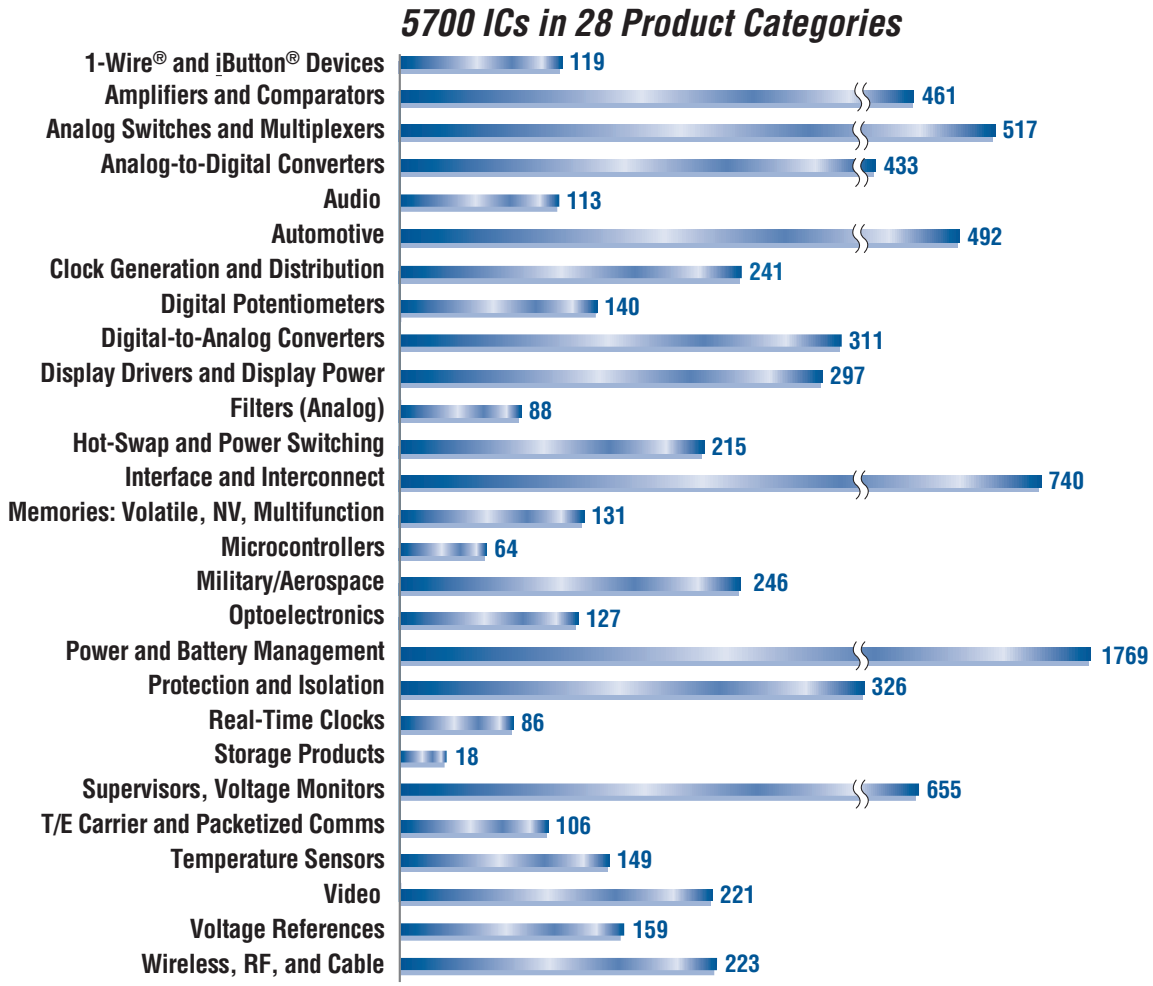

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