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APPLICATION NOTE 2858

DS1859 Internal Calibration and Right Shifting (Scalable Dynamic Ranging)

Dec 10, 2003

Abstract: What sets the DS1859 apart from the crowd is its internal calibration and right shifting (scalable dynamic ranging) features. When used in conjunction, these features greatly enhance the DS1859's 12 bit analog-to-digital converter (ADC), giving it the precision and accuracy of up to a 16 bit ADC without the added cost and size. Furthermore, the DS1859's internal calibration features both programmable gain and programmable offset, eliminating most, if not all, external signal conditioning circuitry. By providing programmable gain in the analog domain before the ADC, the input signal can be amplified/attenuated to make use of the entire range of the ADC. Then, while in the digital domain, right shifting can then be used to scale (divide) the digital output back down so that the desired (or mandated by SFF-8472) LSB remains unaffected and even transparent to the user.

The purpose of this application note is to illustrate how an application can benefit from using internal calibration and right shifting. Furthermore, this application note will provide valuable information on how to implement internal calibration and right shifting. Finally, an example is provided to illustrate the application of the discussed topics.

DS1859 Analog Monitor Inputs

Before going any further, it is beneficial to look at a block diagram of the DS1859 MON inputs (see **Figure 1**). For the sake of clarity, only one input is illustrated, although the concepts apply to all three MON inputs.

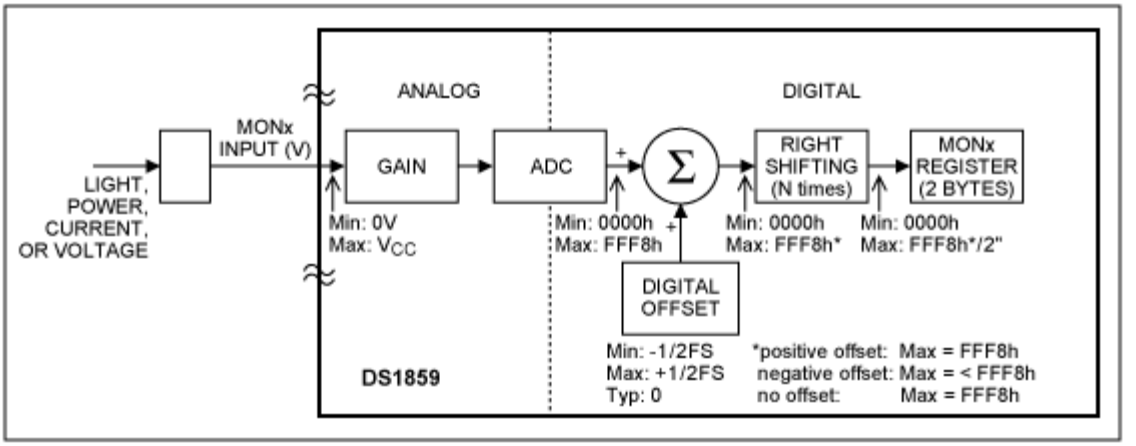

Figure 1. DS1859 MON input block diagram.

As shown in the figure, a single-ended voltage is applied to a DS1859 MON pin. While in the analog domain, the voltage is fed into a programmable gain block capable of attenuation as well as gain. The gain block makes it possible to calibrate the MON channel to achieve a desired LSB or *full-scale voltage*. The full-scale voltage is the voltage at which the digital output reaches full scale (FFF8h). Furthermore, the gain block makes it possible to internally gain small input signals in order to maximize the use of the ADC. This will be described in more detail later.

Following the gain block is the 12-bit ADC. The 12-bit conversions are output left justified in 2 byte (16 bit) values. The ADC is capable of outputting digital values of 0000h to FFF8h.

Once in the digital domain, the DS1859 impressively takes internal calibration a step further by featuring a user-programmable digital offset capable of adding either positive or negative offset. The digital offset can be used to internally add positive or negative offsets by simply performing digital addition. It is important to point out that positive offsets will still clamp at the digital value of FFF8h, but the minimum digital value will now be greater than zero. Likewise, negative offsets will have a full-scale digital value of less than FFF8h (since the negative offset subtracts from the conversions). The minimum digital value in this case will remain at 0000h. Detailed information regarding the digital offset is provided later in the *Offset Cal register* section.

The final operation before the digital values are output is Right Shifting. Each MON input has 3 bits, which control the number of desired right shifts. The benefits of right shifting will be discussed later. Setting the three bits to zero results in zero right shifts and disables the right shifting functionality. As was the same with offset, right shifting also affects the full-scale digital output. For example, if set to 2 right shifts, the full-scale digital output becomes 3FFEh. After the shifting is performed, the value is then written to the appropriate register where the user reads the conversion. This is also the value that is used for alarm and warning comparisons.

The Factory Calibrated DS1859

Each of the DS1859 MON inputs are factory trimmed to a full scale voltage of 2.5V. This means that an input voltage of 2.5V will output the full-scale digital value of FFF8h. Also, each of the digital offsets are factory programmed to zero so that a 0V input will output a digital value of 0000h. And last of all, the right shifting factory default is 0. The transfer function for the factory calibrated DS1859 is illustrated in **Figure 2B** and will be described later.

A factory-trimmed device will output one of 4096 digital values for input voltages from 0 to 2.5V, yielding a

resolution of 610µV (2.5V/4096) for the 12-bit conversion. Ideally, the input signal to be digitized is a 0 to 2.5V signal so that the entire range is utilized. However, in real life, we know this will not always be the case. Take Receive Power for example, where voltages of 0 to .5V are common. It is a shame that 80% of the digital output codes will never be used. It is a waste that the 12-bit converter, capable of generating 4096 codes, will only be outputting one of 820 codes (20% of 4096). The remaining 3276 digital codes will never be used. Furthermore, of the 820 codes that are used, the resolution remains 610µV.

In an attempt to make use of more of the digital codes, it is tempting to re-calibrate at least the Receive Power MON input to a full-scale voltage less than 2.5V. However, doing so alone does not solve the problem because the LSB will change and no longer match the desired LSB. The way to solve the problem is by using internal calibration in conjunction with right shifting as described in the following section.

The Benefit of Using the DS1859 Internal Calibration and Right Shifting

Internal calibration and right shifting are most beneficial when the signal to be monitored is small and hence, not making use of the entire ADC range. By amplifying the signal in the analog domain before the analog to digital conversion, and then dividing it back down by the same factor in the digital domain, the desired LSB is preserved and both precision and accuracy are improved by a factor of 2 for every right shift (up to 4). After 4 right shifts, precision is lost, but the accuracy continues to improve. The beauty of this is that it is done at the expense of the previously wasted range.

The benefit of using internal calibration and right shifting can best be illustrated in the example shown in Figure 2. **Figure 2A** is a voltage vs. time plot of an example signal that is to be monitored. The example signal swings between 0V to 0.5V. Figure 2B and **Figure 2C** are MON input voltage vs. digital output plots that show the factory calibrated transfer function as well as an example transfer function using 2 right shifts and a full-scale voltage of 2.5V/4 = 0.625V, respectively. A full-scale voltage of 0.625V means that fewer codes will be wasted resulting in conversions that are four times larger than the 2.5V full-scale voltage, but which are then divided back down by a factor of 4 (two right shifts). Determining the number of right shifts and hence the full-scale voltage will be discussed in the following section. Two right shifts are used here just to compare a right shifting example against no right shifting. The device settings used, as well as calculations pertaining to each of the transfer functions are shown below each of the corresponding transfer functions.

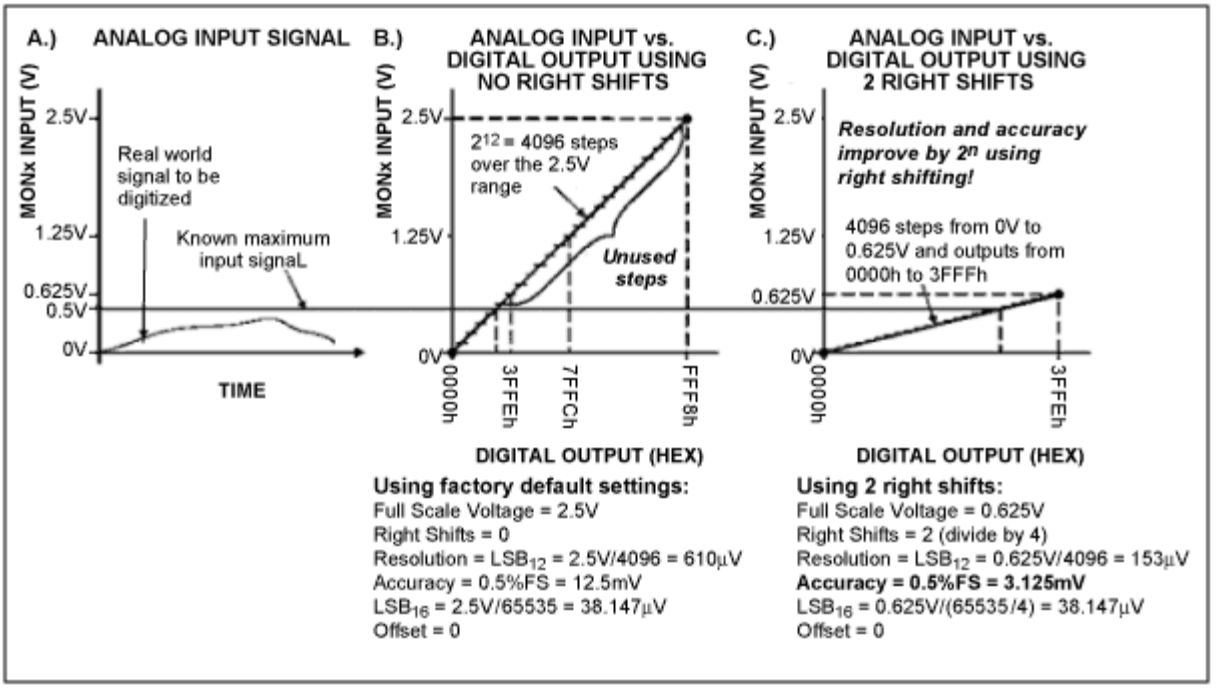

Figure 2. No right shifting vs. right shifting comparison.

All three plots in Figure 2 are shown side-by-side on the same y-axis and scale so that for a particular point on the input signal (Figure 2A), a horizontal line can be drawn through the point and each of the transfer functions so that a rough approximation of the digital output can be made. Going back to the example input signal ranging from 0V to 0.5V, where 0.5V is indicated by the bold horizontal line across all 3 plots, the benefit of right shifting can be seen by comparing plots B and C. This simply reiterates that when the input range of the ADC spans a voltage range much greater than the range of the input signal, numerous steps will be wasted (see plot B). Only 819 of the 4096 are used. The remaining 80% in plot B are wasted. In contrast, plot C shows that by internally calibrating to a smaller full-scale voltage and using right shifting, the precision increased. Now 3276 of the 4096 digital codes are used to digitize the signal. The best part is that after right shifting, the desired LSB is maintained. The right shifting is transparent to the user. This can be verified by observing that both plots output approximately the same digital value.

How to Determine How Many Right Shifts Can Be Used

The number of right shifts that can be used in an application is a function of the full-scale voltage (internal calibration) as well as the percentage of digital codes that are used for a given input signal. If the maximum voltage of the input signal is known (in addition to the full-scale voltage), then the expected digital outputs can be calculated. Otherwise, a "hands on" approach will be required during the engineering evaluation to determine the range of digital outputs, and hence, the ideal number of right shifts. The "hands on" approach is detailed step by step below.

1. Set the right shift bits to 0.
2. Internally calibrate the part to yield the desired LSB (this will determine the initial full-scale voltage).
3. Apply the min and max input signal and read the corresponding digital outputs to determine the used range.
4. Determine what percentage of the ADC range is used. If the digital readings exceed 7FFFh, then right shifting should not be used (zero right shifts). However, if the digital readings are less than 7FFFh, then at least one right shift can be used. If the digital readings are less than 3FFFh, then

two right shifts can be used, and so forth. Refer to Table 9 in the DS1859 data sheet for the remaining ranges.

5. In order to compensate for the division of the digital values, which result from right shifting, gain must be added in the analog domain so that the desired LSB is maintained. This is done by calculating a new full-scale voltage using the formula: new full-scale voltage = initial full-scale voltage / $2^{\#\text{ of right shifts}}$. So, if the internal calibration from step 2 resulted in a full-scale voltage of 2.0V (in order to obtain the desired LSB), and digital readings were greater than 1FFFh but never exceeded 3FFFh, two right shifts would be ideal. The new full-scale voltage for this example is $2.0V/2^2 = 0.5V$.
6. Internally calibrate the channel (with the right shift bits still set to 0) to the new full-scale voltage.
7. Set the right shift bits to their new value.

Once the evaluation determines the ideal number of right shifts and the full-scale voltage for a particular application, only steps 1, 6, and 7 are needed for production calibration.

DS1859 Internal Calibration and Right Shifting Registers

The DS1859 device registers responsible for each analog channel's internal calibration and right shifting settings are summarized in **Table 1**. Register addresses are shown for each of the MON channel settings as well as V_{CC}. V_{CC} has been included in the table for completeness although it will not be discussed in this application note. The locations of the digital conversions have also been included in the table to show their relative location. Notice that the gain, offset, and right shifting registers reside in memory Table 01h (not to be confused with Table 1 of this application note). Memory Table 01h is selected by writing 01h into the Table Select byte, 7Fh. Since the digital conversions are in the lower bank of memory (0-7Fh), they are independent of the Table Select byte.

Table 1. DS1859 internal calibration and right shifting registers

	V_{CC}	MON1	MON2	MON3
Gain Cal	92-93h	94-95h	96-97h	98-99h
Offset Cal	A2-A3h	A4-A5h	A6-A7h	A8-A9h
Right Shifts	N/A	8Eh (b6-b4)	8Eh (b2-b0)	8Fh (b6-b4)
Readings	62-63h	64-65h	66-67h	68-69h
	Table 01h			

Gain Cal Register

The Gain Cal register is a two-byte value that determines the amount of gain/attenuation of a particular monitored channel by adjusting the input switched capacitor network. This gives the user the ability to calibrate the full-scale voltage to any desired value between ~500mV and 6.5535V.

Programming the Gain Cal register, unfortunately, is not as simple as saying "I would like a gain of 4...so I will write a 4 into the Gain Cal register." Furthermore, due to device to device (and lot to lot) variation of the capacitors in the switched capacitor network, it really is necessary to calibrate the setting. The procedure for this calibration and for determining the value that needs to be written in the Gain Cal register is provided in the DS1859 data sheet in the section titled "Internal Calibration". Additional information is provided in this application note in the "How to Internal Calibrate" section.

One final note of caution when calibrating the DS1859, it is important to know the value of the both the offset and the right shifting registers. Otherwise, if they are non-zero and not compensated for, the device

will not be calibrated as intended.

Offset Cal Register

The Offset Cal register is a two-byte value that determines the amount of digital offset applied to each of the monitored inputs. Recall that the DS1859's offset is a simple digital addition or subtraction of the converted values. So once the gain is trimmed to the desired value (and before right shifting is enabled), the offset can be programmed to null out any offset or to move the range. Unfortunately, similar to the Gain Cal register, determining the value to program is not as easy as saying "I would like 100mV of offset...so I will write 100 into the register."

While the internal calibration pseudo code shown in the DS1859 "Internal Calibration" section of the data sheet shows how to determine the Offset Cal value needed to "null" out the offset, this section provides additional information as well as examples of positive and negative offset.

Offset Cal is calculated by first determining how many counts should be added to or subtracted from the conversions. One way this is typically done is by applying the null input (such as laser off) and then reading the conversion. This would be the value that you would have subtracted off of all the conversions.

The value that needs to be written into the Offset Cal register is calculated by inserting the desired count into the equation provided in the DS1859 data sheet and repeated below.

Offset Cal Register = [4000h - (Count/2)] XOR 4000h

Example 1: If you apply 0V to the MON input and see a count of 200 (C8h), you can use the offset register to subtract say 200 (C8h) from the A/D conversions to null it out. Using the formula to determine what to write to the register:

Offset Cal register = [4000h - (C8h/2)] XOR 4000h = 7F9Ch

Keep in mind that in this case, a subtraction is being performed, so the full-scale count (FFF8h) will also decrease by C8h, giving a new full-scale count of FF30h.

Example 2: Now lets say for some reason you wanted to add 200 counts to the readings. In this case, the 2 negatives (the negative in the formula and the -C8h cancel) make the second term positive, yielding:

Offset Cal register = [4000h + (C8h/2)] XOR 4000h = 0064h

To calculate the new full-scale count you would (attempt) to add C8h to FFF8h. However FFF8h is the maximum possible reading, so the full-scale count would remain FFF8h.

Example 3: Calculate the Offset Cal value for zero offset.

Offset Cal register = [4000h - (0/2)] XOR 4000h = 0000h

This also happens to be the factory default for the Offset Cal register.

Right Shifting Registers

The right shifting registers (Table 01h, bytes 8Eh-8Fh) are much easier to understand than the gain and offset registers. Since MON1-MON3 are capable of performing up to 7 right shifts, three bits are required

for each MON input. The settings for MON1 and MON2 reside in Table 01h, byte 8Eh, while the setting for MON3 resides in Table 01h, 8Fh. Refer to the memory map in the datasheet for the location of the bits. The factory default of these EEPROM registers are 00h, disabling right shifting.

To further illustrate the result of right shifting, **Figure 3** shows several examples of the resultant MON values.

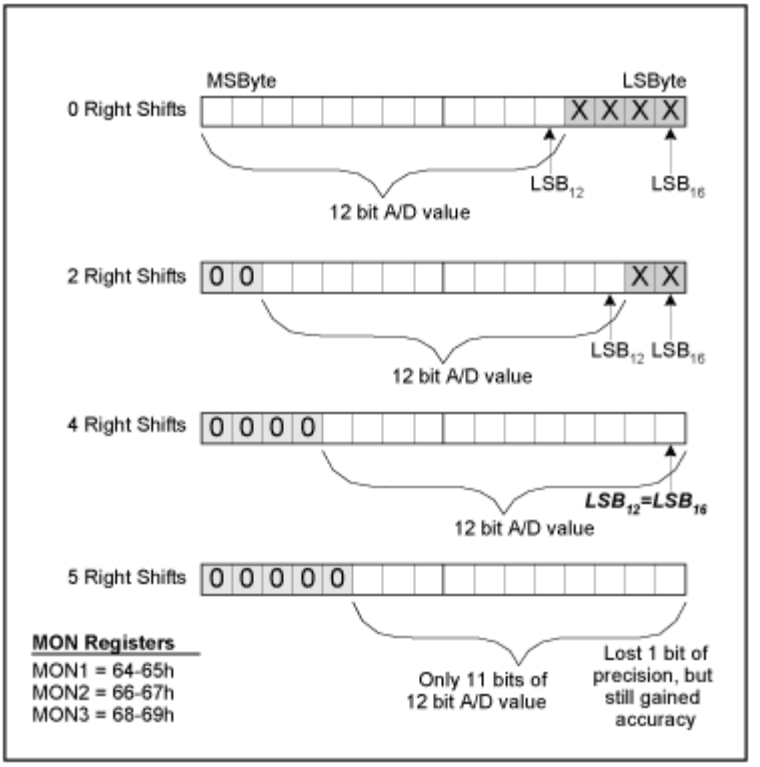

Figure 3. MON register right shifting examples.

How to Internal Calibrate

While there are several ways internal calibration can be performed, this application note discusses the binary search approach shown (using pseudo-code) in the DS1859 data sheet. The outputs of the pseudo-code algorithm are gain and offset register values, which yield the desired transfer function, i.e., the desired LSB.

In order to use the pseudo-code algorithm, one must have the ability to set the laser to two different intensities, for example minimum and 90% of the maximum, and also have ability to go through multiple iterations. For non-optical applications, two different voltages must be applied on command to the MON inputs. The algorithm provided in the data sheet uses 90% of maximum so that the upper limit is less likely to clamp. However, when applying a percentage of the desired full scale it is important to calculate the corresponding percentage of the digital values as well.

The algorithm begins by setting the offset and right shifting registers to a known state, namely zero offset and zero right shifts. Although this example sets both registers to zero, other values can be used as long as they are compensated for. For example, when starting out with a programmed offset, FFF8h may no longer be the clamped, full-scale digital value (see the Offset Cal Register section). In addition to initializing registers, the algorithm begins by also calculating a few important constants, which are a

function of the desired LSB.

The binary search for the gain value begins by setting the Gain Cal register to half scale, 8000h. The gain value is then tested by applying the 90% maximum input to the MON channel being calibrated and then reading the corresponding digital conversion. This value is then called Meas2. Meas2 is checked to see if it is clamped, FFF8h (since offset and right shifts are zero). If the reading is clamped, it cannot be concluded whether the conversion is actually FFF8h or if it is much greater (which is also FFF8h). Either way, the gain setting is too high. In binary search fashion, the gain value is cut in half and the process repeats until a non-clamping gain value is found.

As soon as a non-clamping Meas2 is found, the algorithm continues by forcing the null input and reading its digital conversion. This conversion becomes Meas1. Finally, the delta between Meas2 and Meas1 is calculated and compared to the desired delta (CNT2-CNT1) using the constants calculated at the beginning of the algorithm. If Meas2-Meas1 is less than CNT2-CNT1, then the gain is again cut in half. Otherwise, if Meas2-Meas1 is greater than CNT2-CNT1, then the gain is increased by cutting the gain in half and this time adding it to the current gain. The process repeats until a total of 16 iterations are performed. The resultant is a 16-bit value that yields the desired gain (and desired LSB).

An alternate way of visualizing the gain calibration procedure is as follows. Beginning with the MSB (b15) of the 16 bit Gain Cal register, set the bit to a 1 (all other bits are initially set to 0). With the MSB = 1, the process of applying the analog input and reading the digital output is performed. If the reading is clamped, then the gain is too high and the MSB is written back to a 0. Otherwise, the MSB remains a 1. The MSB is now known. Now on to the next bit, b14. Set b14 to 1 (leave b15 set to what was already determined). Bits 13 down to b0 are still 0. Again go through the process to determine if the gain is still too high. If so, then b14 becomes a 0. Otherwise, it becomes a 1. The procedure then continues bit by bit until all 16 bits are determined. The result is again a 16 bit value which yields the desired gain.

Once the desired gain is achieved, a new offset can be calibrated or it can be left at 0 (no offset). The method of calibration depends on how the offset feature is to be used. The explanation accompanying the algorithm in the data sheet assumes that the user wants to apply negative offset to null out the digital readings so that the null analog input will produce all zeros output. This is done simply by applying the null analog input and reading the conversion. If the null input (laser off for example) produces a digital output of say 20h, the offset can be programmed such that 20h will be digitally subtracted from every conversion. In this example, 20h is substituted into the offset formula and the result is then programmed into the Offset Cal register for the desired MON channel.

Internal Calibration and Right Shifting Example

In order to demonstrate the concepts presented in this application note, the following example has been provided.

In this example, MON3 is used to monitor Rpower. When the minimum input of -40dBm is applied, a voltage of 10mV is presented to the MON3 pin of the DS1859. The desired digital output for this input is 0000h. When a 0dBm input is applied, 300mV is presented to MON3. The desired digital output in this case is 2710h and was chosen in order to satisfy the LSB dictated by SFF-8472 (the LSB for Rpower is 0.1µW).

Determining the ideal number of right shifts for this example is relatively simple since the range of the desired digital output has been given (0000h-2710h). Using Table 9 of the DS1859 data sheet, the ideal number of right shifts is 2. Now with 2 right shifts in mind, in order for a 2710h to be the final output ***after*** two right shifts, we can conclude that an input of 300mV must result in a conversion of 9C40h ***before*** the right shifts. Therefore, internal calibration will be used to "gain up" the conversion to 9C40h for an input of

300mV. Once the internal calibration and programming of the offset are complete, two right shifts will be enabled. Our example is summarized in **Table 2**.

Table 2. Internal calibration and right shifting example

Customer Signal Rpower (dBm)	Voltage applies to MON3 pin (mV)	Digital outputs during cal. (0 right shifts)(hex)	Final Digital output (2 right shifts)(hex)
-40	**10**	0000	**0000**
	50		0563
	100		0C1F
	150		12DB
	200		1997
	250		2051
0	**300**	9C40	**2710**

Once the relationship between input and output is determined (shown in Table 2), the internal calibration routine provided in the data sheet is used to internally calibrate the device. The routine begins by performing some preliminary calculations, which are shown below. Notice that the 90% shown in the data sheet routine is not used here because the second calibration point (300mV = 9C40h) is already less than 90% of the full scale value. Therefore the internal calibration routine used in this example has all references to the 90% removed.

Given Table 2, the following calculations are made.

LSB = (0.300V - 0.010V)/(9C40h - 0000h) = 0.290V/40,000 = 7.25µV

Full Scale Voltage = FS = LSB × 65535 = 7.25µV × 65535 = 0.475128V

CNT1 = 0.010/LSB = 1379.3 => 1379 (dec)

CNT2 = 0.300/LSB = 41379.31 => 41379 (dec)

CNT1 and CNT2 are the expected (desired) digital outputs when the two calibration points are applied. The internal calibration routine will iterate in search for a slope as close as possible to the slope determined by these two values.

The iterative portion of the routine goes through 16 cycles of programming a slope in a binary search fashion and then checking if it is equivalent to the desired slope. For the purpose of this example, a DS1859 was calibrated using the internal calibration procedure and the inputs and outputs of all 16 iterations are shown in **Table 3**.

The first column of Table 3, Iteration, is equivalent to n in the routine. The column *gain_result* is the value programmed into the Gain Cal register (device Table 01h, bytes 98-99h) for every iteration. Columns Meas2 and Meas1 are the digital values read from the device with 300mV and 10mV applied to the input, respectively. Finally, for iterations in which Meas2 did not clamp, Meas2-Meas1 is compared to CNT2-CNT1. If Meas2-Meas1 is greater than CNT2-CNT1, then the gain_result is too large. The Gain Cal bit corresponding to that iteration becomes a zero, which in turn determines the gain_result of the successive iteration. Once all 16 iterations are complete, the Gain Cal value is known. The device used in this example resulted in a Gain Cal value of **5038h**.

Table 3. Actual internal calibration values

Iteration	gain_result	Meas2	Meas1	Meas2	Meas1	Meas2-Meas1	CNT2-CNT1	bit result	Gain Cal
(dec)	(hex)	(hex)		(dec)		(dec)	(dec)	(bin)	(hex)
15	8000	fd58	870	64856	2160	62696	40000	0	5
14	4000	82a0	450	33440	1104	32336	40000	1	
13	6000	c010	658	49168	1624	47544	40000	0	
12	5000	a138	558	41272	1368	39904	40000	1	
11	5800	b0b8	500	45240	1280	43960	40000	0	0
10	5400	a938	5a0	43320	1440	41880	40000	0	
9	5200	a530	578	42288	1400	40888	40000	0	
8	5100	a328	568	41768	1384	40384	40000	0	
7	5080	a238	568	41528	1384	40144	40000	0	3
6	5040	a1a8	560	41384	1376	40008	40000	0	
5	5020	a170	558	41328	1368	39960	40000	1	
4	5030	a190	558	41360	1368	39992	40000	1	
3	5038	a198	558	41368	1368	40000	40000	1	8
2	503C	a1a0	558	41376	1368	40008	40000	0	
1	503a	a1a0	558	41376	1368	40008	40000	0	
0	5039	a1a0	558	41376	1368	40008	40000	0	

With the device programmed to its new Gain Cal value, the Offset Cal is determined by forcing 10mV (the voltage which we want to read 0000h) and reading the digital result. The device used in this example output a value of 0558h with 10mV applied. Using the offset formula, the Offset Cal is calculated as shown below.

MON3 Offset Cal = [4000h - 0558h/2] XOR 4000h = 7D54h

And finally, the new clamp value can be calculated as follows:

New clamp value (pre- right shift) = FFF8h - 0558h = FAA0h

With the internal calibration complete, the 2 right shifts are enabled by writing 20h to Table 01h, location 8Fh.

Conclusion

The internal calibration and right shifting features of the DS1859 provide the utmost flexibility and make the DS1859 suitable for a wide variety of applications. This application note has provided additional information not found in the DS1859 data sheet, such as why internal calibration and right shifting are beneficial as well as how to implement them. A "hands on" example was also provided to tie the concepts together and to provide actual data read from a DS1859 during the internal calibration procedure.

Questions/comments/suggestions concerning this application note can be sent to: mixedsignal.apps@maximintegrated.com.

Related Parts

DS1858	Dual Temperature-Controlled Resistors with Three Monitors	Free Samples
DS1859	Dual, Temperature-Controlled Resistors with Internally Calibrated Monitors	Free Samples

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