Keywords: jitter, class D, speaker amplifier, digital input, cycle-skipped clock, PDM, PCM, I2S, TDM, wideband, class-D, sigma delta, WLP, PDM_CLK, PDM_DATA, BCLK, LRCLK, PSRR, EMI, delta sigma

APPLICATION NOTE 5461

Digital-Input Class D Amplifiers Expand the Benefits of Traditional Class D and Simplify System Design

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Nov 21, 2012

Abstract: This application note describes a new generation of digital-input Class D audio amplifiers that achieve high PSRR performance, comparable to traditional analog Class D amplifiers. More importantly, these digital-input Class D amplifiers provide additional benefits of reduced power, complexity, noise, and system cost.

A similar version of this article appears on *EDN*, November 3, 2012.

Introduction

Electronics vendors commonly use high-efficiency, filterless, analog-input Class D amplifiers to manage the power requirements of portable audio speakers found in cell phones, tablet computers, and personal navigation devices. These Class D amplifiers allow direct connection to a battery, which minimizes losses and reduces component count. The amplifiers also achieve > 70dB PSRR performance, which is important to avoid audible buzzing with 217Hz demodulated GSM signals.

Analog-input Class D amplifiers normally require a digital-to-analog converter (DAC) and line driver amp on the application processor (**Figure 1**). Unfortunately, this adds die cost, power, and noise to the speaker output. These Class D amplifiers also require careful board design to avoid degradation because of signals coupling onto the analog board routes.

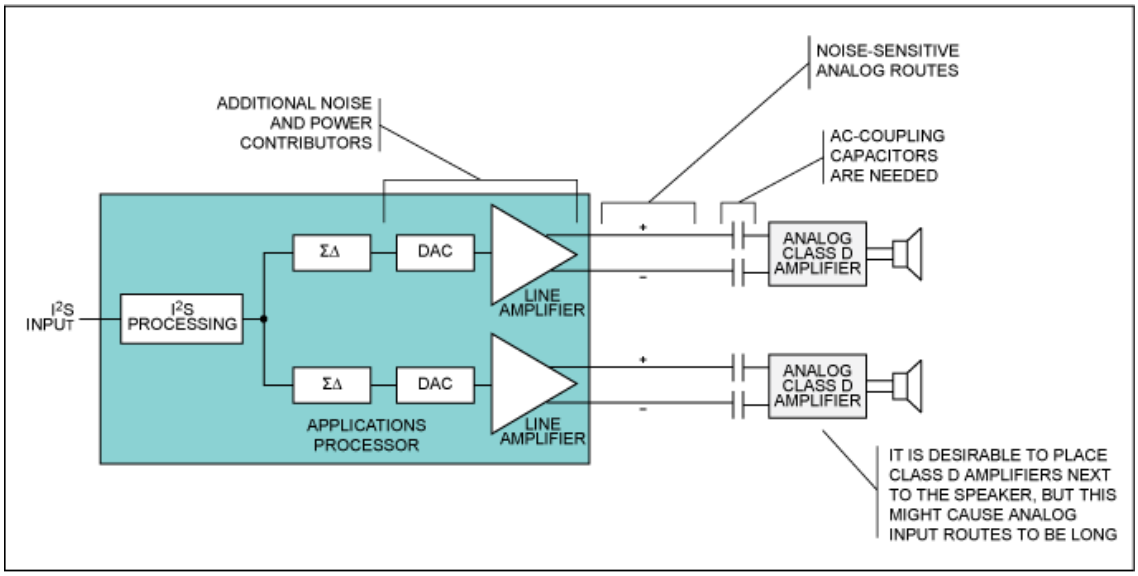

Figure 1. Conventional system with analog-input Class D speaker amps. The DAC and line driver amp on the application processor add die cost, power, and noise to the speaker output.

Digital-input Class D audio amplifiers are immune to most board design issues. Single-channel Class D amplifiers can be placed at remote locations on a board to minimize the routing of the high-current battery and speaker load connections. These amplifiers do not need the DAC and line driver amp of analog-input Class D designs. Thus, space and system costs drop and designs are simpler.

Simplified System Design

The most common type of digital-input for an amplifier is pulse-density modulation (PDM) which requires only two wires: PDM_CLK and PDM_DATA. Single-bit PDM data is created with an oversampled delta-sigma modulator on the application processor (**Figure 2**).

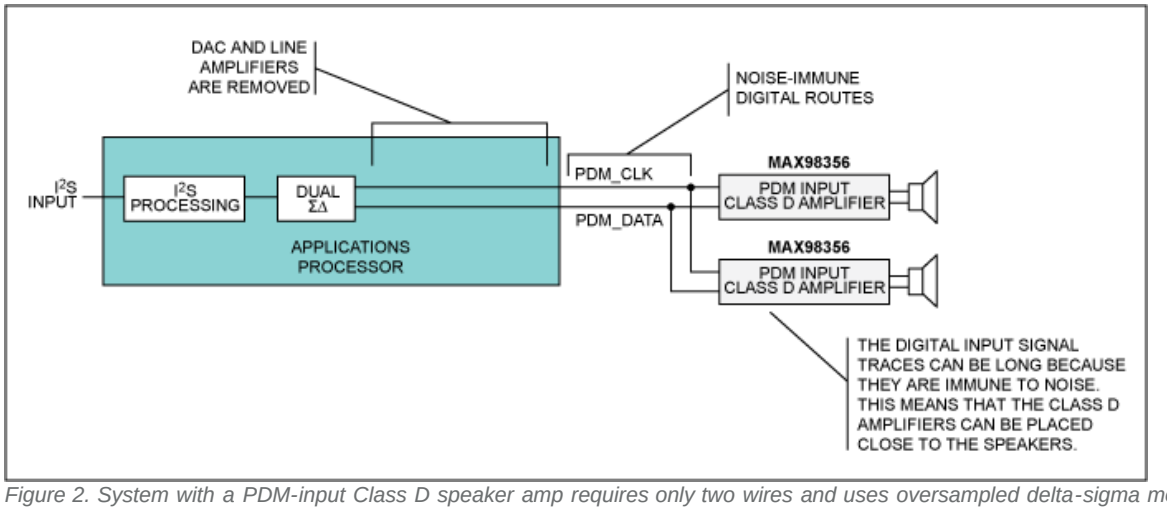

Figure 2. System with a PDM-input Class D speaker amp requires only two wires and uses oversampled delta-sigma modulator on the application processor to create single-bit data.

A few amplifiers will accept pulse-code modulated (PCM) or I²S data, which requires three wires: BCLK, LRCLK, and DIN. The PCM data format does not require a modulator or upsampling of the data on the application processor (**Figure 3**). Some older implementations of PCM-input amplifiers also require a clean master clock (MCLK) to derive a jitter-free sampling clock. Newer PCM input amplifiers like the MAX98355 no longer require the MCLK input so pin count, power consumption, and board complexity are all reduced.

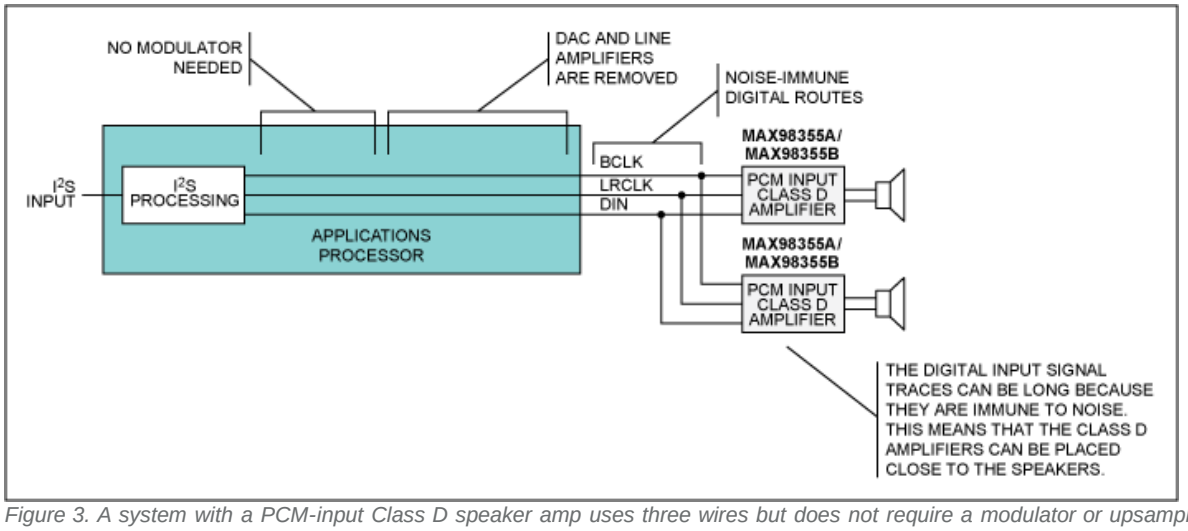

Figure 3. A system with a PCM-input Class D speaker amp uses three wires but does not require a modulator or upsampling of the data on the application processor.

Older digital-input amplifiers offer adjustable sample rate and/or bit depth that, in some cases, require complex programming of

the amplifier. Newer generations of digital-input amplifiers like the MAX98355/MAX98356 automatically detect a wide range of sample rates and bit depths to self-configure without any programming.

In a multichannel implementation the digital-input Class D audio amplifier reduces the number of external capacitors and routed lines on the board. Only PDM_CLK and PDM_DATA lines are needed for PDM inputs to provide stereo data to two Class D amplifiers. The BCLK, LRCLK, and DIN lines are needed for PCM inputs to provide stereo data. As a comparison, a stereo analog-input Class D amplifier will normally require two differential input signals (four wires) to be routed with AC-coupling capacitors. (See Figures 1, 2, and 3.)

Most digital-input amplifiers require both a low digital-supply voltage (1.8V) and a high speaker-supply voltage (2.5V to 5.5V). Now board design and component count can be simplified by using a single-supply Class D amplifier like the MAX98355/MAX98356.

Jitter Tolerance and Clock Generation

Digital-input Class D audio amplifiers do, admittedly, present a new challenge for clock jitter. For good audio quality, most digital-input amplifiers require fairly low levels of jitter on BCLK or PDM_CLK. The jitter tolerance is often not quoted in the data sheet; when jitter tolerance is quoted, the typical specification is ~200ps of RMS jitter. High levels of clock jitter will typically degrade either the amplifier's dynamic range or the full-scale THD+N performance.

In many systems the reference oscillator for the application processor is not a convenient multiple of the PDM_CLK or BCLK, so providing a low-jitter clock for the amplifier is not easy. For example, 13MHz is a common crystal frequency used for GSM phones and 27MHz is commonly used in video solutions. Neither of these reference frequencies is a convenient multiple of the 44.1ksps or 48ksps audio sample rates. These systems will, therefore, often implement a complicated fractional-N PLL to create the clock for the audio. In some cases, the solution will require a separate audio reference oscillator which increases complexity and bill of materials (BOM).

An alternative, and preferable, solution is a digital-input amplifier that can tolerate very high clock jitter without degrading the audio performance. Such an amplifier will reduce system complexity. In the simplest case, a cycle-skipping clock can be used to generate the PDM_CLK or BCLK, but this generates extraordinarily high jitter. If a 13MHz reference clock is cycle skipped to create a 6.144MHz PDM_CLK (48ksps x 128OSR), then the peak jitter will be 38.4ns and the RMS jitter will be 22.2ns (**Figure 4**). This represents two orders of magnitude higher jitter than most DACs can tolerate. The MAX98355 PCM and MAX98356 PDM Class D audio amps, however, still produce near 100dB dynamic range performance with this amount of clock jitter. A cycle-skipped clock can be created with a very small number of digital gates on the application processor. They do not need the oscillator or a loop filter that would otherwise be required in a PLL solution. See **Figure 5**.

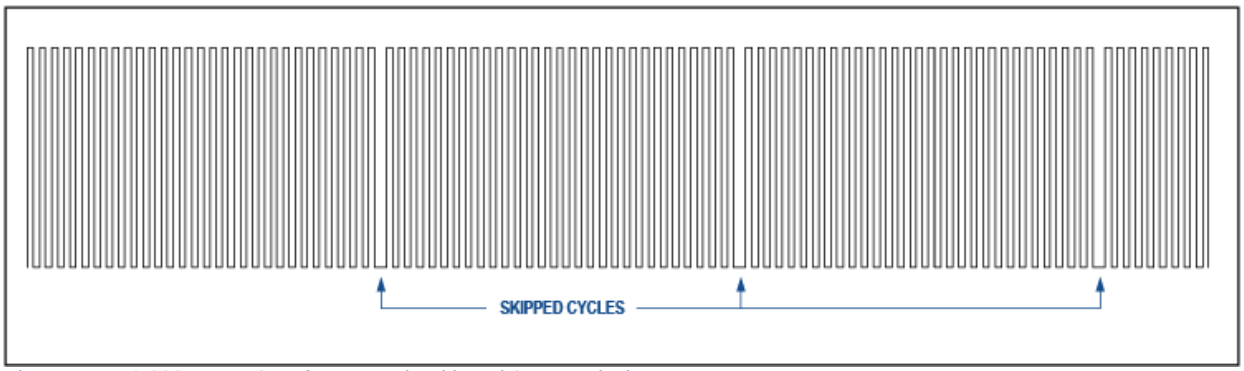

Figure 4. A 12.288MHz MCLK from a cycle-skipped 25MHz clock.

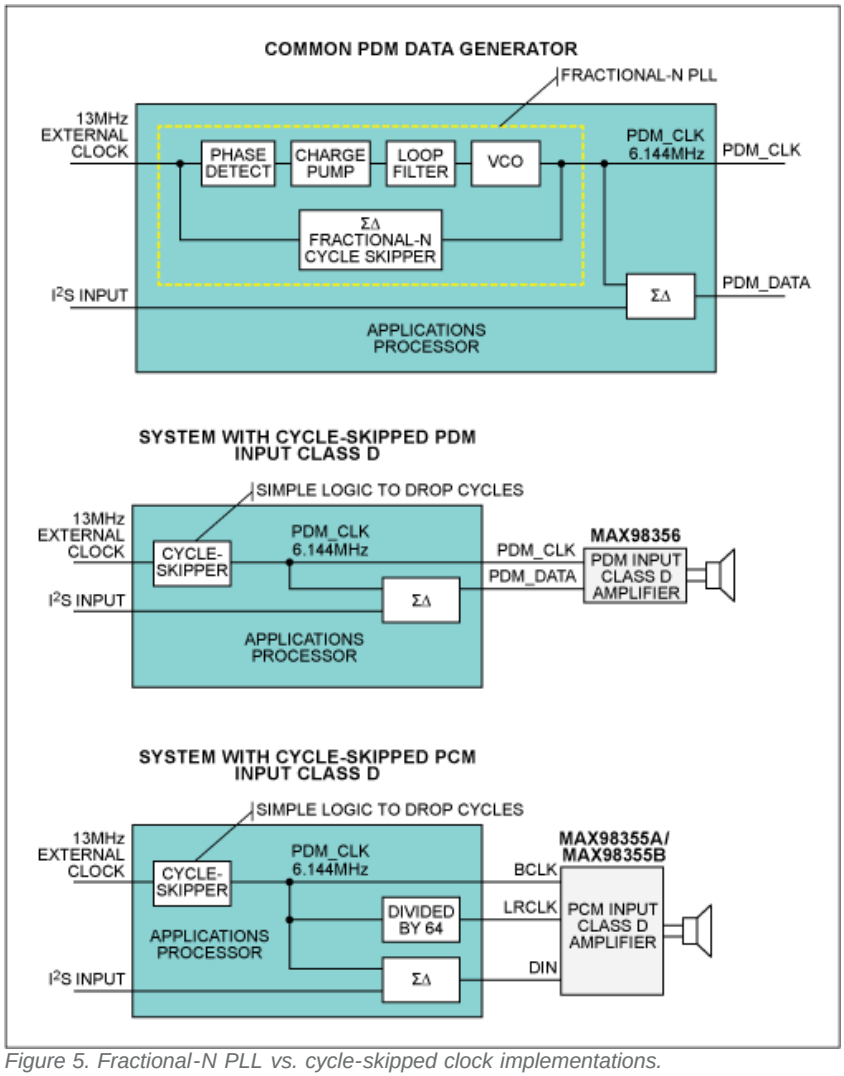

Figure 5. Fractional-N PLL vs. cycle-skipped clock implementations.

Jitter Tolerance Test Results

Test results show that the MAX98355's dynamic range does not degrade with the cycle-skipped jittered clock. The MAX98355 outperforms the "120dB DAC" by more than 20dB with the jittered clock. Further details on jitter tolerance in delta-sigma DACs can be found in application note 5477, "Analyzing Audio DAC Jitter Sensitivity."

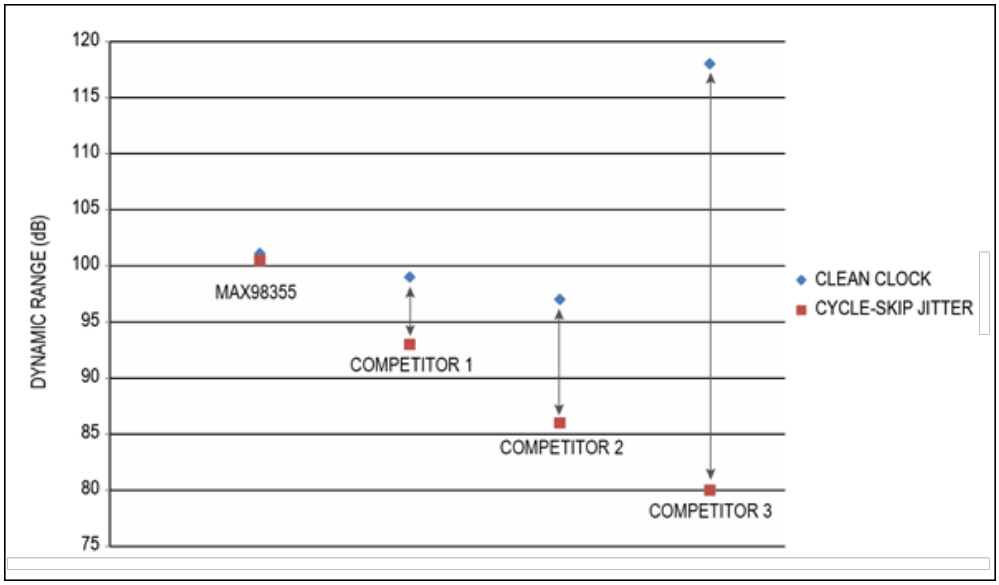

Figure 6. Dynamic range degradation with 11.5ns RMS cycle-skipped clock jitter.

Conclusions

Digital-input filterless Class D audio amplifiers like the MAX98355/MAX98356 allow simple board-level implementation, a low BOM, high efficiency, low EMI, and high output power. These amplifiers are available in a 1.345mm x 1.435mm, 9-pin WLP package and produce as much as 3.2W of output power.

Related Parts		
MAX98355A	PCM Input Class D Audio Power Amplifiers	Free Samples
MAX98355B	PCM Input Class D Audio Power Amplifiers	
MAX98356	PDM Input Class D Audio Power Amplifier	

More Information
For Technical Support: http://www.maximintegrated.com/support
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