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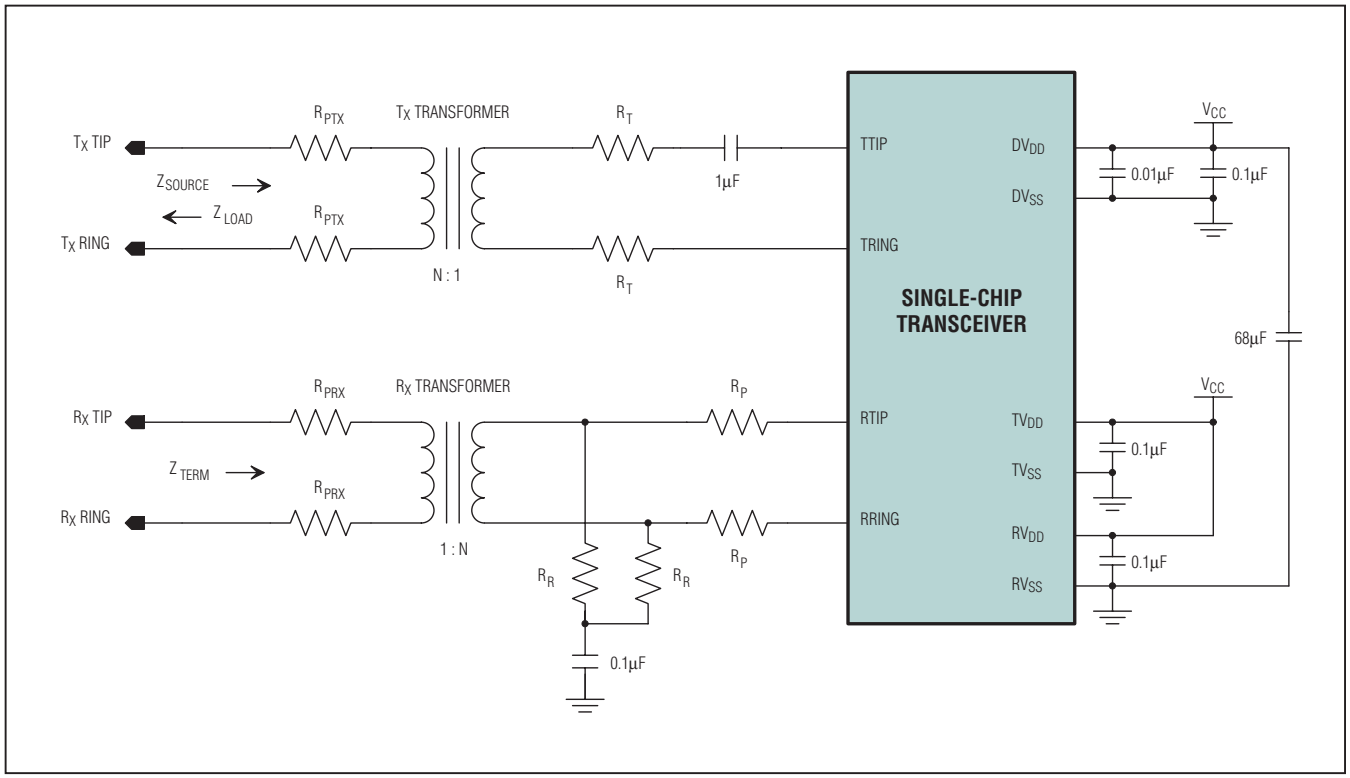

This traditional interface circuit for T1/E1 devices illustrates how resistance is distributed around transformers. Using the model as the baseline circuit for network interface design, users can better understand secondary voltage protection for the DS2155. (See article inside, page 3.)

News Briefs

MAXIM REPORTS REVENUES AND EARNINGS FOR THE FIRST QUARTER OF FISCAL 2002

Maxim Integrated Products, Inc., (MXIM) reported net revenues of $239.4 million for its fiscal first quarter ending September 29, 2001, a 43.3% decrease from the $422.3 million reported for the first quarter of fiscal 2001 and a 24.7% decrease from the $318.1 million reported for the fourth quarter of fiscal 2001. Net income for the quarter was $61.3 million compared to $119.1 million last year, a 48.5% decrease. Diluted earnings per share were $0.17 for the first quarter, a 48.5% decrease from the $0.33 reported for the same period a year ago.

During the quarter, the Company repurchased approximately 8.2 million shares of its common stock for $286.6 million and acquired a total of $25.6 million of capital equipment. The stock repurchase was enabled by temporary suspension by the SEC of regulations relating to stock repurchases after pooling-of-interests transactions. The Company also purchased an additional 2.0 million shares of its common stock during the first week of the second quarter of fiscal 2002. Accounts receivable decreased by $53.0 million in the first quarter to $99.5 million due to the decrease in net revenues, and inventories decreased $3.3 million to $159.3 million.

Gross margin for the first quarter was 70.0%, after increasing inventory reserves $3.5 million, compared to 69.8% reported for the fourth quarter. Research and development expense was $66.0 million or 27.6% of net revenues in the first quarter, compared to $70.0 million or 22.0% of net revenues in the fourth quarter. Selling, general and administrative expenses decreased $4.1 million from $29.2 million in the fourth quarter to $25.1 million in the first quarter. Operating expenses decreased as a result of the reduction of sales representative commissions, labor consolidation in the combined sales organizations completed in the fourth quarter, and controlling other discretionary spending.

First quarter bookings were approximately $211 million, an 18% increase over the previous quarter's level of $179 million. Turns orders received during the quarter were $102 million, a 64% increase over the $62 million received in the prior quarter (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders). Bookings increased in the U.S. both for OEM and distribution channels and in the Pacific Rim region. Bookings for most product lines were higher than in the fourth quarter of fiscal 2001. First quarter ending backlog shippable within the next 12 months was approximately $196 million, including $172 million requested for shipment in the second quarter of fiscal 2002.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the quarter: "Allowing that the economic recovery will continue through the next two to three quarters, Maxim performed generally according to our plan for the first quarter of this recovery. Order patterns stabilized early in the first quarter and increased as the quarter progressed. While we are encouraged by the increase in order rates, we remain cautious about our short-term revenue outlook because of customers' backlog situations and their unwillingness to commit to inventories and longer term orders due to short lead times. As lead times begin to creep out, we expect bookings rates to continue to increase. We do expect that our fourth quarter was the bottom of the dot com-induced correction period for bookings, with the first quarter representing the revenue low point. Although we expect second quarter bookings to exceed first quarter levels, we estimate that second quarter revenues and earnings will increase only slightly over first quarter levels due to available backlog at the beginning of the second quarter."

Mr. Gifford concluded: "Our productivity improvement plans associated with the acquisition of Dallas Semiconductor are progressing according to schedule. Consolidation of our worldwide distribution channels, reorganization of our internal sales organization, the transferring of Dallas' back-end manufacturing offshore, and other initiatives resulted in over $35 million in savings in the first quarter of fiscal 2002, even on a reduced revenue base."

Certain statements in this press release are forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. These statements involve risk and uncertainty.

All forward-looking statements included in this news release are made as of the date hereof, based on the information available to the Company as of the date hereof, and the Company assumes no obligation to update any forward-looking statement.

Network interface and circuit designs for secondary protection of the DS2155 single-chip transceiver

T1/E1 single-chip transceivers (SCTs) are used in applications that connect directly to outgoing telephone lines that can expose the applications to hazardous overvoltage or overcurrent conditions. For such applications, protection networks (either primary voltage protection or secondary voltage protection) must be used to direct high voltages or currents away from the sensitive low-voltage CMOS devices.

Gas discharge tubes or carbon blocks located at the point where the line enters the premises usually provide primary voltage protection; but because primary voltage protection only limits the voltage surges to 1000V peak and power-line cross to 600V_{RMS}, secondary voltage protection is necessary. Secondary voltage protection provides additional voltage and current limiting to prevent damage to the network interface device.

This paper provides general information about the network interface and circuit designs for secondary protection of the DS2155 single-chip transceiver. These designs are targeted for compliance with the following standards:

- Underwriters Laboratories UL 1950 and UL 60950
- TIA/EIA-IS-968
- Telcordia GR 1089-Core
- International Telecommunication Union ITU-T K.20, K.21

Longitudinal (common mode) surges are from tip to ground or ring to ground while metallic (differential) surge types are between tip and ring. Longitudinal surges are formed on the tip and ring conductors by lightning currents that enter the conductive shield of the cable. **Metallic surges** are a byproduct of longitudinal surges and are formed between the tip and ring conductors by imbalances in the operation of the primary protectors or equipment on the line.

The circuit in **Figure 1** is a traditional interface for T1/E1 devices and illustrates how resistance is distributed around the transformers. This model will be used as the baseline circuit for the network interface design. It contains extra resistors that are not used in the final design but are essential for many of the concepts presented in this article.

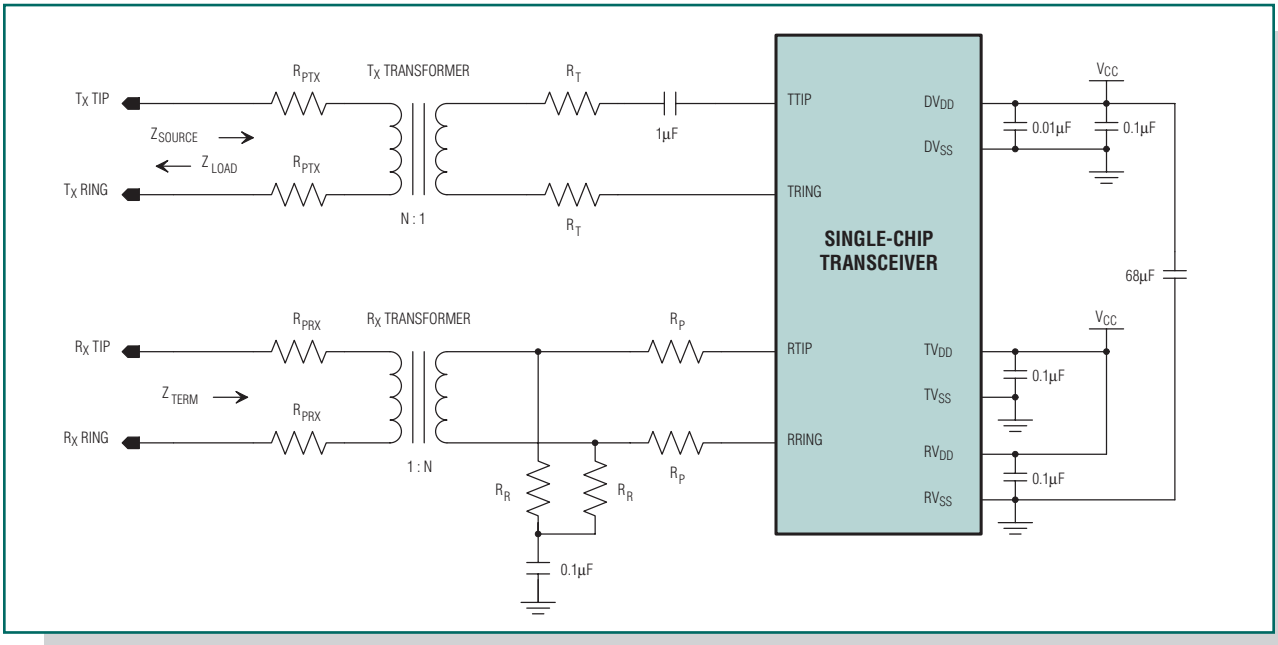

Figure 1. A traditional network interface circuit with distributed resistance for protection.

Receive interface

The receiver inputs present a high impedance and require very little input current to operate. They are designed to recover a signal using a 1:1 transformer with 0Ω of series resistance under a matched load. The primary consideration in the receive circuit is the accurate termination of the transmission line. A T1 signal is carried on 100Ω balanced twisted pair while an E1 signal is carried on either 75Ω unbalanced coaxial cable or 120Ω balanced twisted pair.

The components involved in the termination network are the R_{PRX} resistors, R_R resistors, and the turn ratio of the transformer; the receive-transformer turn ratio is specified as 1:1, N = 1. The termination circuit is ideal if R_{PRX} is 0Ω and the resistance of R_R equals half of the characteristic line impedance. If the R_{PRX} resistors are present, they form a voltage divider and R_R must be adjusted. As the resistance of R_{PRX} increases, the resistance of R_R decreases. The following equation gives an example of how to calculate R_R for proper termination:

$$Z_{TERM} = R_{PRX} + 2R_R / N^2$$

Substitute:

$$Z_{TERM} = 100\Omega,\ R_{PRX} = 0\Omega,\ N = 1 \ \therefore\ 100\Omega = 2R_R$$

$$\text{Solve } R_R \ \therefore\ R_R = 50\Omega$$

To ease the design of receive termination for both T1 and E1 circuits, the D2155 selects the termination by using software. By designing the receive circuit for 120Ω termination, the internal line interface unit (LIU) can selectively add resistance to the line to achieve the additional termination settings of 75Ω or 100Ω. The LIU inserts either 200Ω or 600Ω of internal resistance between the RTIP and RRING pins.

Changes must be made to the traditional network interface when using internal termination. First, any current-limiting resistors, which include R_P and R_{PRX}, must be removed from the receive path. R_P must be removed because the resistors interfere with the additional resistance that the internal circuitry adds. R_{PRX} must be removed so the parallel resistance value of 75Ω, 100Ω, or 120Ω is formed by the combination of R_R resistors and the internal resistors in the DS2155. Second, the R_R resistors must be set to match a line termination of 120Ω. Since R_{PRX} is 0Ω, the resistance of R_R equals 60Ω, which is half of the characteristic line impedance.

Finally, because resistance in the circuit can no longer protect the device from overcurrent conditions, a combination of fuses and voltage suppression must be used. An example of this type of circuit along with test results is discussed later.

Note: The 0.1µF capacitor connected to resistors R_R form a high-frequency cutoff filter for improved noise immunity and does not affect line termination.

Transmitter interface

The transmitter output drivers present a low impedance and are able to drive sufficient current into the primary winding of the transformer to produce the required output pulse. The transmitter outputs are designed to fit an output pulse into a template based on the line impedance, operational voltage, transformer coil winding, inline resistance, and specific mode of operation, i.e., 100Ω T1, 75Ω E1, or 120Ω E1. Unlike the receive transformer, the transmit-transformer turn ratio is directly related to the operational voltage. The DS2155 operates at 3.3V; therefore, the transformer turn ratio is specified as 1:N, where N = 2.

Since the signal pulses and the requirements for the transmit-side interface of T1 and E1 are different, the transmit circuit description is more complicated than the receive circuit. To help users easily understand, the transmitter interface description is broken into two sections. The first section covers the T1 transmitter interface; the second section covers the E1 transmitter interface.

T1 device transmit circuit

The transmitter outputs of Dallas' T1 parts are designed to generate the correct pulse amplitude at the network interface for varying line lengths. Since the different line lengths affect the pulse shape, the parts have programmable output levels. Every part has a transmitter line build-out (LBO) table in the data sheet that shows the settings to choose based on the transformer turn ratio and the line length. A default T1 pulse for a known line length is generated under the following conditions: 3.3V supply; R_{PTX} = 0Ω, R_T = 0Ω; and a transmit transformer with a turn ratio of 1:2.

A nominal 0dB T1 pulse is 3V under a 100Ω load or 3V at 30mA on the network interface. An unprotected circuit using a 1:2 transformer with 0Ω series resistance will have to produce a 3V × 1/2 = 1.5V pulse at the device's output pins. The current drive into the device side, or primary winding, of the transformer will be 30mA × 2 = 60mA.

Traditionally, resistors R_{PTX} or R_T are used to protect the device from surges. But adding series resistance creates a voltage drop that attenuates the output signal pulse. To compensate for the signal loss, select a trans-

former with a turn ratio larger than 1:2. This increases the current draw from the transmitter outputs by more than 20%. For this reason, it is recommended that 3.3V circuits be designed with 0Ω of series resistance and other components be used for overvoltage protection.

The following example illustrates how the 1:2 transformer could be replaced by a 1:2.42 transformer if it were necessary to use R_{PTX} or R_T to protect the circuit from surges. While the current pulse in the network side or secondary winding of the 1:2.42 transformer will remain the same, the current pulse in the primary winding of the transformer will be 30mA × 2.42 = 72.6mA. Because the output voltage pulse is still 1.5V, the net impedance (R_L) seen by the transmitter will be 1.5V / 72.6mA = 20.6Ω and is described by the following:

$$R_L = Z_{LOAD} / N^2 + 2R_{PTX} / N^2 + 2R_T$$

Substitute: $R_L = 20.6\Omega$, $Z_{LOAD} = 100\Omega$, N = 2.42

$$\therefore 20.6\Omega = 100\Omega / 5.86 + 2R_{PTX} / 5.86 + 2R_T$$

Simplify: $3.5\Omega = 2R_{PTX} / 5.86 + 2R_T$

If R_{PTX} is 0Ω, then R_T = 1.75Ω, which is not enough to significantly reduce current. However, if R_T is 0Ω, R_{PTX} can be as much as 10Ω each and will provide current-limit protection for the transformer.

E1 device transmit circuit

The transmitter outputs of Dallas' E1 parts are designed to generate the correct pulse at the network interface under varying termination conditions. The programmable output levels ensure that pulse amplitude at the network interface have a peak voltage of 3.0V for 120Ω termination or 2.37V for 75Ω termination. Unlike in T1, E1 applications can have additional resistance in the transmit path to match the source impedance to the characteristic line impedance. The measure of how well the source and line impedance are matched is return loss. A higher return loss results in greater attenuation of line noise or signal reflections being coupled in the transmitter outputs and is calculated by the following:

$$\text{Return Loss (dB)} = 20 \log_{10} |Z_{SOURCE} + Z_{LOAD}| / |Z_{SOURCE} - Z_{LOAD}|$$

$$Z_{LOAD} = 120\Omega \text{ or } 75\Omega \text{ and } Z_{SOURCE} = 2R_{PTX} + (2R_T + 5) \times N^2$$

The constant 5 in the Z_{SOURCE} equation above is the transmitter's internal impedance. The return loss for an unprotected network interface without a high return-loss condition is shown below. In the example resistors, the supply voltage is 3.3V, R_{PTX} and R_T = 0Ω, the T_X transformer has a turn ratio of 1:2, and the line impedance is 75Ω.

$$\text{Return Loss (dB)} = 20 \log_{10} |Z_{SOURCE} + Z_{LOAD}| / |Z_{SOURCE} - Z_{LOAD}|$$

Substitute: $Z_{LOAD} = 75\Omega$, N = 2, R_{PTX} and $R_T = 0\Omega$

$$\therefore \text{Return Loss} = 20 \log_{10} |5 \times 2^2 + 75| / |5 \times 2^2 - 75|$$

$$\text{Return Loss} = 20 \log_{10} 1.73 = 4.7\text{dB}$$

In this example, 58% of the noise or reflected signal can be coupled into the transmitter outputs. To improve the return loss, the value of R_T can be increased. Changing R_T to a value of 6.2Ω increases the return loss to 28.5dB. This means less than 4% of the inbound signal will be reflected. Because any series resistance will affect the pulse amplitude, the DS2155 compensates for specific R_T or R_{PTX} values. When designing the network interface, use **Table 1**, which is also found in the DS2155 data sheet, for proper transformer and resistor selection. Each setting is based on the operational voltage, the transformer turn ratio, and R_T.

To ease the design of transmit-impedance matching for E1 circuits and to allow T1 circuits to take advantage of this feature, the DS2155 performs internal-impedance matching. By designing the transmit interface circuit with 0Ω of series resistance, the internal LIU can selectively add resistance to match the transmitter output to a 75Ω, 100Ω, or 120Ω line impedance. It does this by inserting internal resistance between the TTIP and TRING transmit output driver and the associated pins on the device.

Table 1. LBO select for DS2155 3.3V devices

L2	L1	L0	Application	T_X Transformer	Return Loss[1]	R_T [2]
0	0	0	75Ω normal	1:2 Step-up	–	0
0	0	1	120Ω normal	1:2 Step-up	–	0
1	0	0	75Ω with high return loss	1:2 Step-up	> 21dB	6.2
1	0	1	120Ω with high return loss	1:2 Step-up	> 21dB	11.6

Notes:
1. Empty cells indicate that the return loss is less than 21dB.
2. The value of R_T shown assumes that R_{PTX} = 0Ω.

Changes must be made to the traditional network interface when using internal termination. Both the R_T and R_{PTX} resistors must be 0Ω. If these resistors are present, the combination of external and internal resistance will cause an impedance mismatch. This end result would be a degraded transmit signal pulse, which will not meet the pulse mask requirements.

A combination of fuses and voltage suppression must be used to protect the device from hazardous transient conditions upon current resistor removal. An example of this type of circuit along with test results is discussed in the following section.

Voltage-suppression protection circuits

The following secondary voltage protection examples provide immunity from metallic and longitudinal surges as well as power-line cross. The designs in **Figures 2** and **3** have several advantages over traditional protection circuits. They decrease the amount of surface area used by components since all of the components used in the design are surface mounted for automated assembly. The components allow low-voltage operation while maintaining the same level of protection as traditional circuits. These circuits allow the use of the new receive-side, software-selected termination and transmit-side line-impedance matching features in the DS2155. Figure 2 is an example of a metallic surge-suppression circuit generally found in customer-premises equipment. Since customer-premises equipment does not have to supply simplex power onto the line, this circuit has the advantage of lower component count and reduced cost. Figure 3 is an example of a longitudinal surge suppression circuit usually found in central office equipment. It is common for central office equipment to supply simplex or phantom power to line repeaters. This is done by applying voltage to the network-side center tap of the transmit and the receive transformer. Because this power connection is longitudinal in nature, it is necessary to ensure that the protection circuit does not activate when this voltage is present.

The three main components used for protection are the fuse, thyristor, and Schottky diode devices. The fuse protects the transformer against high current conditions such as power-line cross. The current rating of the fuse is set to match the maximum power dissipation of the transformer. Typical fuses have a surge current rating above 50A for the different voltage and current surge models. If the surge current rating is less than 100A, a current-limiting series resistor will be necessary. One fuse that passes many of the different surge models and does not

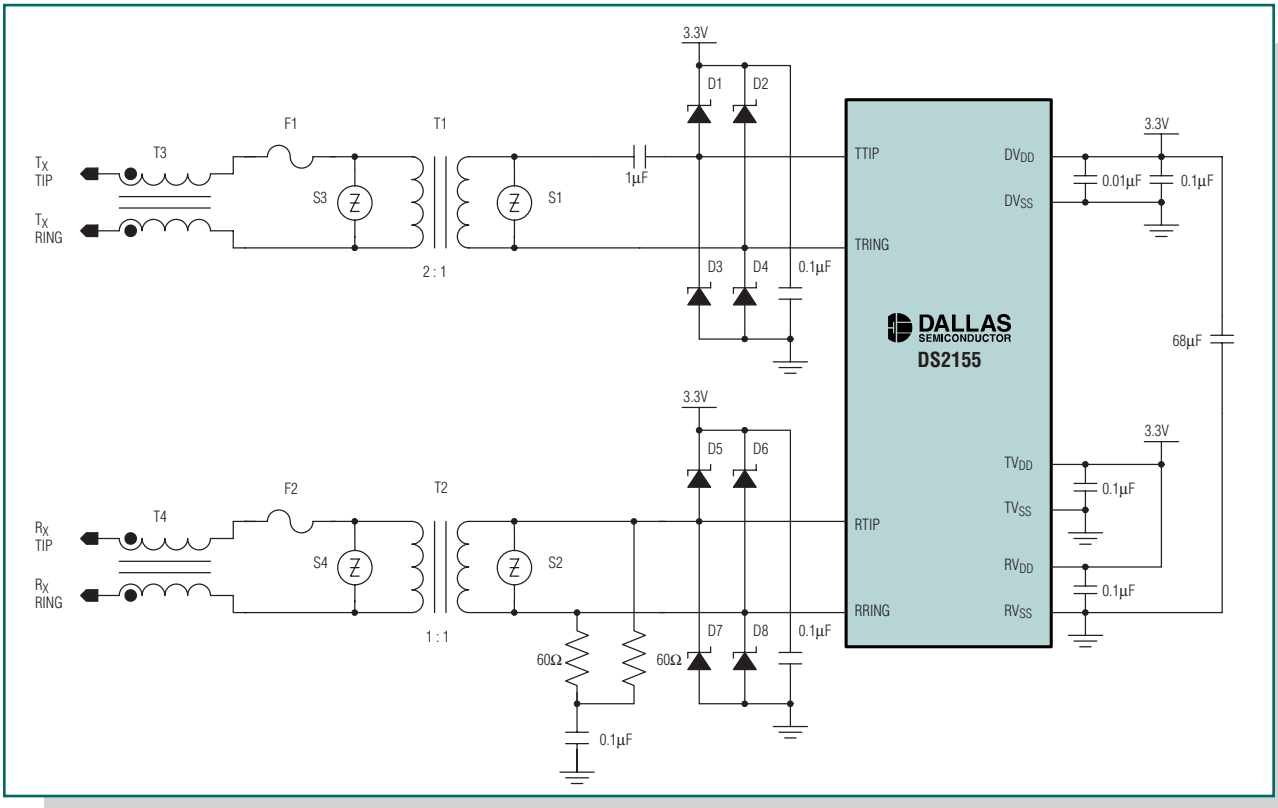

Figure 2. DS2155 network interface circuit with metallic protection and software-selected termination.

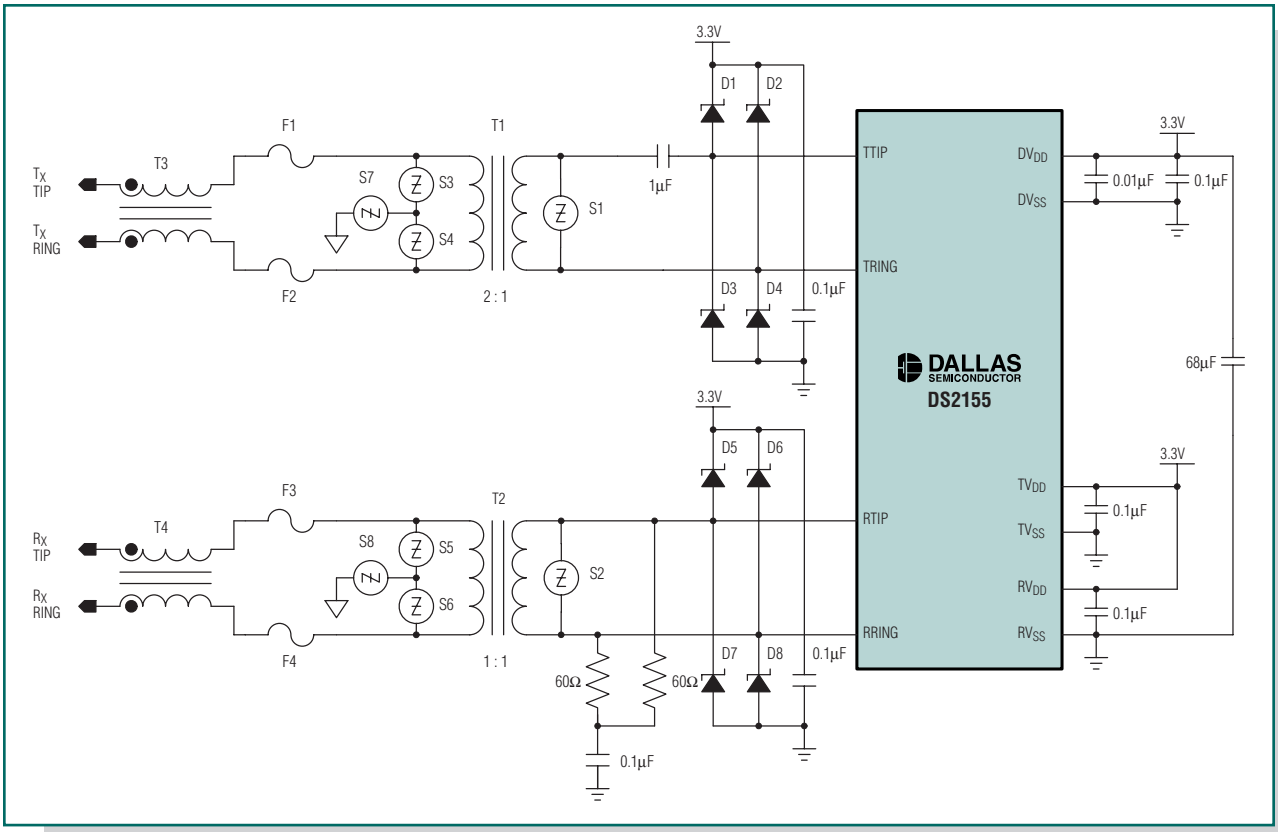

Figure 3. DS2155 network interface circuit with longitudinal protection and software-selected termination.

require current-limiting resistors is the Teccor F1250T TeleLink fuse. The thyristor is a solid-state crowbar device that changes from an open-circuit to a short-circuit condition when the voltage across the device exceeds the switching voltage. The thyristor will remain in the short-circuit state until the current flowing through the device falls below a set-holding current. In the short-circuit state, excess current is routed between the two transmission lines or a transmission line and ground, thus stopping it from damaging the semiconductor device. The Schottky diode is a rectifying device that exhibits large current flows under forward bias and very small current flow under reverse

Table 2. Voltage-suppression protection-circuit components

Reference	Description	Part	Source	Notes
D1–D8	Schottky diode	10BQ040	International Rectifier	
F1–F4	1.25A slow blow fuse	F1250T	Teccor Electronics	
S1, S2	25V max transient suppressor	P0080SA	Teccor Electronics	
S3, S4	77V max transient suppressor	P0640SC	Teccor Electronics	Figure 2
S3–S6	40V max transient suppressor	P0300SC	Teccor Electronics	Figure 3
S7, S8	220V max transient suppressor	P1800SD	Teccor Electronics	Figure 3
T1, T2	Transformer 1:1CT & 1:2CT (SMT)	PE-68678	Pulse Engineering	
T3, T4	Dual common-mode choke (SMT)	PE-65857	Pulse Engineering	

Notes:
1. The layout from the transformers to the network interface is critical. Traces should be at least 20mils wide and separated from other circuit lines by at least 150mils. The area under this portion of the circuit should not contain power planes.
2. Some T1 (never in E1) applications source or sink power from the network-side center taps of the RX/TX transformers.

bias. Since the Schottky diodes have a lower forward bias than the internal diodes inside the device, any excess current that would normally flow through the device will now flow through the Schottky diodes.

Surge results

To meet the aforementioned specifications, various current and voltage surge pulses must be applied between the tip, ring, and ground conductors. The specific circuit application will determine which surges must be applied to the circuit to pass specification. All of the surges consist of three characteristics: voltage, current, and time. The most common way of referring to a specific surge is by the time, which is expressed in the rise and decay of the surge. The surge is a double exponential, meaning that it rises and decays exponentially. The rise time is measured as the time it takes for the surge to reach the peak current rating, whereas the decay time is measured as the time when the surge has reached 50% of the peak current rating. Some of the more common surges are 2 x 10µs, 10 x 160µs, 10 x 560µs, and 10 x 1000µs. While there are other surge combinations, many of those fit inside the template of these four surges. In this case, if the circuit passed the surge that had a larger template, it would theoretically pass any surge that fits inside of that template.

When testing the circuit design, it was decided that the 10 x 1000µs surge would be a sufficient indication of whether or not the circuit would reliably pass and be compliant with the various standards. This was done because of time considerations and the limited availability of the surge generator. Separate 10 x 1000µs surges applied simultaneously to the tip and ring conductors have a peak current of 100A and a peak voltage of 1000V.

Figures 4 and **5** were taken of the surge pulse before they were applied to the network interface circuit. To accurately show the rise and decay of the pulse, a 100X current probe measured the output of the surge generator to ground. Figure 4 shows the rise time of the surge pulse, which is slightly longer than 10µs with no load; the pulse rise time is exactly 10µs when the generator output is loaded. Figure 5 shows the decay time, which is approximately 1000µs.

Figures 6 and **7** were taken of the surge pulse as it was applied to the network interface circuit. In both images, trace 1 is the surge measured with 100x current probe from the output of the surge generator to the tip connector. Because the surges on tip and ring are identical and the surge protection is symmetric, it is only necessary to show the surge at one of the connectors. Trace 2 is the surge measured with a 1x voltage probe from the output of the surge generator to the tip connector.

Figure 6 shows the surge pulse being clamped to a maximum of 178V and a mean of 45V. There is also a slight negative-going pulse that is a byproduct of the surge generator. The residual 45V in the measurement is caused by the inductance of the choke and the large current that is flowing through it. Although it is not shown, the resulting surge on the transformer had a maximum of 178V and was just over 6µs long. The energy contained in this surge is extremely small compared to the original surge present at the tip and ring

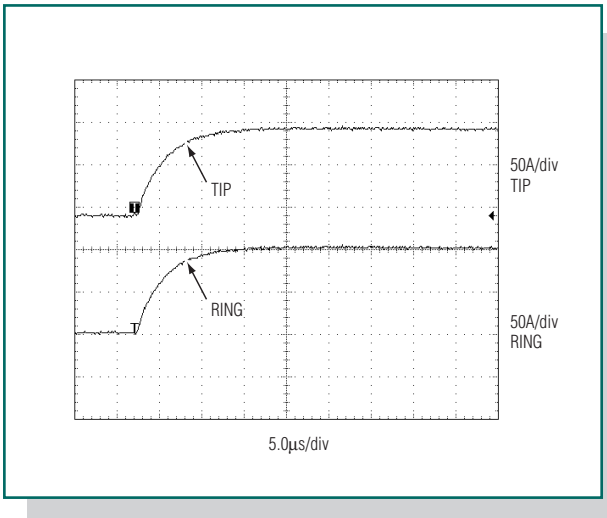

Figure 4. Surge rise time at tip and ring input

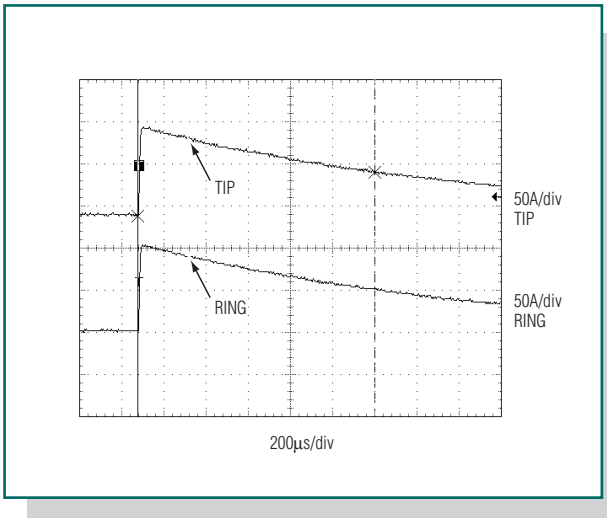

Figure 5. Surge decay time at tip and ring input

pins. Figure 7 is the same surge but shows the speed at which the voltage is clamped and the decay of the surge.

One of the main goals when designing telecommunications equipment is to have the equipment remain in working condition after a lightning strike or power cross.

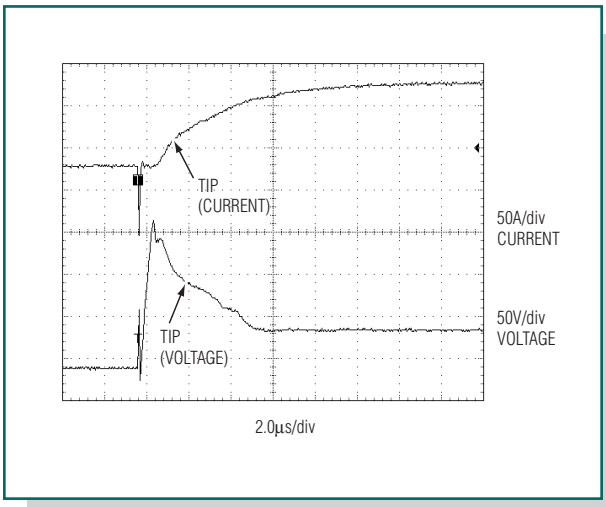

Figure 6. Initial surge clamping at tip input

The circuits presented in this article will allow telecommunication designs to pass even the most stringent compliance standards. The end result will be equipment that is more stable and requires fewer field repairs, which increases customer satisfaction.

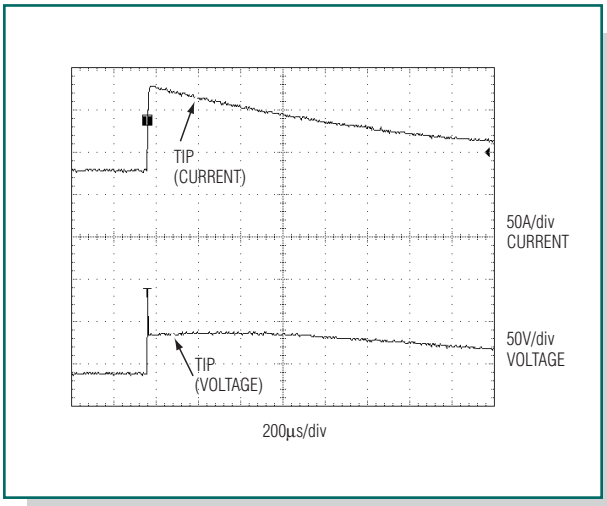

Figure 7. Initial surge voltage spike at tip input

Lithium coin-cell batteries: predicting an application lifetime

Dallas Semiconductor builds a large number of products that incorporate lithium coin-cell batteries to provide nonvolatile (NV) memory or real-time clock (RTC) functionality in the absence of system power. The typical specification for these products has been to provide a 10-year battery lifetime in the absence of system power. Because of end-application uncertainties, the lifetime prediction is conservative.

End users should evaluate the anticipated lifetime in their specific application, especially for applications that exceed typical commercial environments or that need to reach lifetimes beyond 10 years. An understanding of the reliability model is also beneficial for users opting to purchase discrete battery controllers and combine them with a battery, rather than purchasing the module product containing the controller and battery. This article gives the reader an overview of the major factors affecting the lifetime of an integrated circuit (IC) that can be powered by either the system power or a lithium battery for a backup supply.

Why battery backup?

There are several alternatives for data retention while the system is powered-off. Battery-backed SRAMs are a reliable alternative when the read-write speed or number of cycles is important. Flash or EEPROM also provide NV data storage, but at the cost of simplicity or speed. The major disadvantage of battery-backed SRAM is that the battery is a consumable. Therefore, the product selection must consider the available charge within the battery to determine the end product's lifetime. For devices that need to maintain time in the absence of system power, some form of electrical energy needs to be available to maintain a crystal oscillator. This current demand is well suited to being maintained by a battery.

IC current demands

If an IC (SRAM or RTC) is going to be battery powered, there needs to be a match between the current demands of the IC, the expected lifetime, and the energy available in the battery. If the IC and battery are being purchased, the data sheet specifications will provide the information required to predict the lifetime of the battery as a function of the IC load. If the IC and battery are being purchased as a module, end users can rely on the module manufacturer to have the appropriate screens in place to ensure that the system lifetime meets the specification.

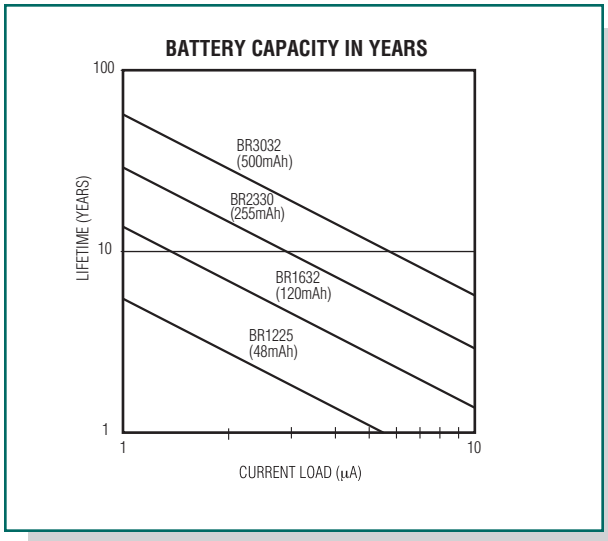

Figure 1. Lifetime based on amount of current being pulled from the battery.

Dallas Semiconductor has established screening limits on all of its battery-backed products that allow the available battery capacity to power the end part for specified lifetimes up to 10 years. In the case of Dallas Semiconductor ICs, the design and fab processes have been optimized to produce low-current demands. In the case of higher density SRAMs purchased from outside vendors, special screening is sometimes required to ensure that the module lifetime specifications are met. **Figure 1** is produced from battery capacities reported by Panasonic. The four lines shown in Figure 1 represent four of the most common battery sizes (BR1225, BR1632, BR2330, and BR3032). The battery manufacturers' rated electrical capacity (in mAh) is shown with each battery size.

Battery construction/attributes

Dallas Semiconductor has chosen to use primary lithium coin-cell batteries in modules that require battery backup. These cells, which have a rated voltage of 3V

and a typical in-system voltage around 2.7V, make them well suited as a backup supply. The voltage also remains stable during the battery discharge (**Figure 2**), so the voltage at the end of life is nearly the same as with a fresh battery. While a flat discharge curve is desirable for backup supply voltage, it does make predicting the remaining electrical capacity difficult.

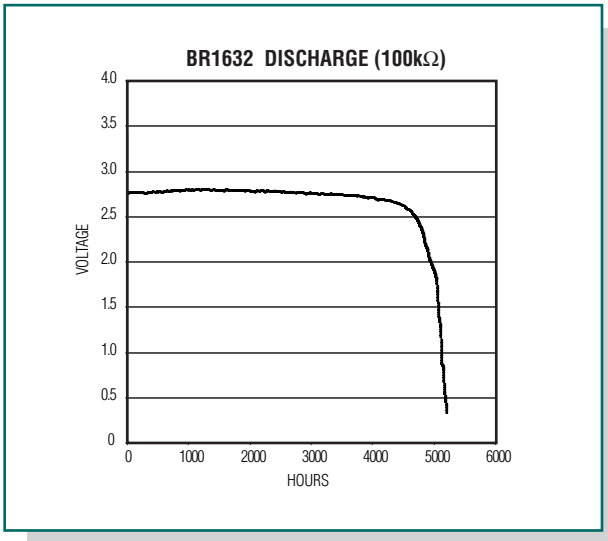

Figure 2. The output voltage remains constant during discharge.

Primary lithium coin-cell batteries have a very predictable behavior. Distributions of such key parameters as open-circuit voltage or internal impedance are very tightly grouped. These tight distributions allow the battery manufacturers to set aggressive test limits in their process to ensure that abnormal cells are excluded from the population. These tight distributions also allow the user of the batteries to identify IC/battery systems that contain a defect. For example, since the voltage distribution and the voltage vs. battery load is very predictable, the battery voltage after a load has been attached can be an indicator of the load placed on the battery. If the battery load is the current demand of a well-behaved distribution of ICs, the resulting loaded voltages will also be tightly distributed. Any loaded voltage that is seen outside of the normal distribution is then an indication of an abnormal IC or battery. This result can be used to reject the resulting module as a potential reliability risk.

Battery testing/screening

The battery manufacturer's 100% testing creates an extremely consistent product. However, anyone using batteries as an integral part of his system should employ testing methods to ensure that only properly functioning cells are included in the end product. There are three types of defects that can be detected by a properly defined screen. First are the test escapes from the battery manufacturers' system. These are the easiest to detect. The second form of defect is low-level internal leakage. It is possible for a battery to have an internal defect that would manifest itself only after some period of time. Detecting these cells requires a thorough understanding not only of the proper testing levels but also the anticipated distribution of results. The third type of defect is a handling or manufacturing defect by the battery user. Because of the limited amount of electrical capacity available, inadvertent loads placed on the cell for even short periods of time can result in reduced electrical lifetimes.

A thorough screening program will involve 100% tests for electrical characteristics at key steps in the manufacturing process. Because of the predictable nature of the electrical performance, measuring the battery voltage before and after load-attach will identify cells that are abnormal. Such screening also identifies loads that are not typical. In addition to the electrical screening, a visual sampling of the batteries will help identify manufacturing variations that could result in degraded leak resistance.

Battery reliability model

The battery is a "balanced construction" with the reactive components included in quantities that should result in full reaction. The key components to the electrical reaction are the metallic lithium, cathode, and electrolyte. The battery manufacturers' goal is to maximize the available energy placed in the cell. Since the internal volume of the battery is limited, the maximum energy density is achieved when the components are in exactly the correct ratios. Therefore, any component loss limits the available reaction of the other components. The reliability model for batteries takes the balanced construction into account and seeks to determine what will cause any key component depletion.

Because the battery is a consumable in the system, the most obvious limitation of the lifetime will be an electrical load placed on the battery. The lifetime based on an electrical load is easy to calculate. Simply divide the available battery capacity in milliamp hours by the current demand in milliamps to get the lifetime in hours. Determining the battery's lifetime as a function of electrical load also requires consideration of the power-on duty cycle. In a properly designed system, the battery is

electrically isolated while system power is applied. This eliminates any battery current draining or charging. The reduced duty cycle will effectively extend the lifetime of the battery in systems that are powered up a high percentage of the time and are relying on battery backup for only a short time.

Because these batteries are being used in very low or zero-current applications, users also need to look for other possible mechanisms that will deplete any of the reactive components. One such mechanism is electrolyte loss through the crimp seal. This mechanism has been shown to be temperature-accelerated with an activation energy of approximately 1.0eV. At room temperature the batteries will exhibit an electrical loss rate of less than 0.5% per year, and this mechanism can safely be ignored. However, at elevated temperatures the loss rate of the electrolyte can become significant and must be considered.

Because of the reactive components' balanced nature, it does not matter whether the electrical reaction consumes the electrolyte or it is expelled through the seal because of elevated temperatures. When the battery does not have enough electrolyte to continue the reaction, the battery will no longer provide current. Therefore, we recommend using a parallel model for lifetime predictions that considers the electrical demand and temperature when predicting the system lifetime (**Figure 3**). There are models that treat the electrical and temperature depletion legs as independent and predict a lifetime as if there were no interaction between the two components of electrolyte loss. Using such a model will overstate the true lifetime if the system is exposed to temperatures much higher than room temperature.

Calculating the lifetime of the battery is similar in concept to calculating the effective resistance of two parallel resistors. The user has control over whether the IC is consuming power from the battery or the system's power supply, so the current consumption leg is shown to include a switch. While the IC is being powered from the system power supply, the lifetime due to current consumption can be approximated as infinite.

The manufacturer of the IC/battery system has control over the selected components and manufacturing process. Properly selected components and manufacturing screens should result in adequate system-level lifetime. However, end users have control over the ultimate lifetime performance based on the actual use of the system. End users can control both legs of the model. The electrical load leg is controlled through the power-on duty cycle of the equipment. While system power is applied, the Dallas Semiconductor components include battery isolation circuitry that electrically isolates the battery and eliminates all current drain from the battery. Therefore, the electrical load leg of the reliability model is only active while the system is in battery backup. The system ambient temperature controls the temperature-accelerated leg. Providing adequate cooling and proper component placement can help reduce the temperature exposure of the battery and, thereby, extend the system's lifetime.

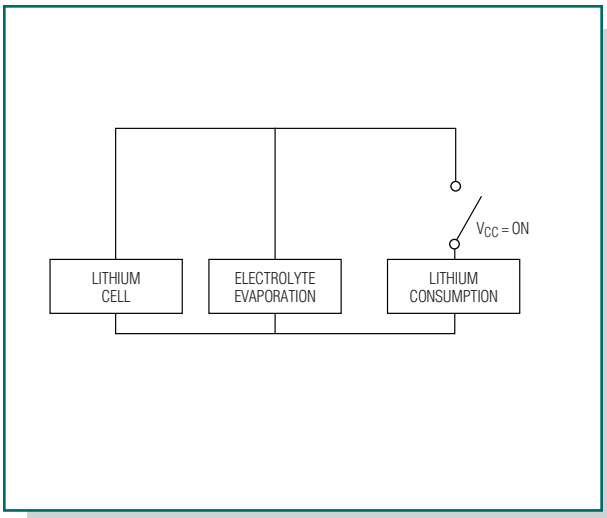

Figure 3. Battery lifetime based on electrolyte evaporation and electrical consumption.

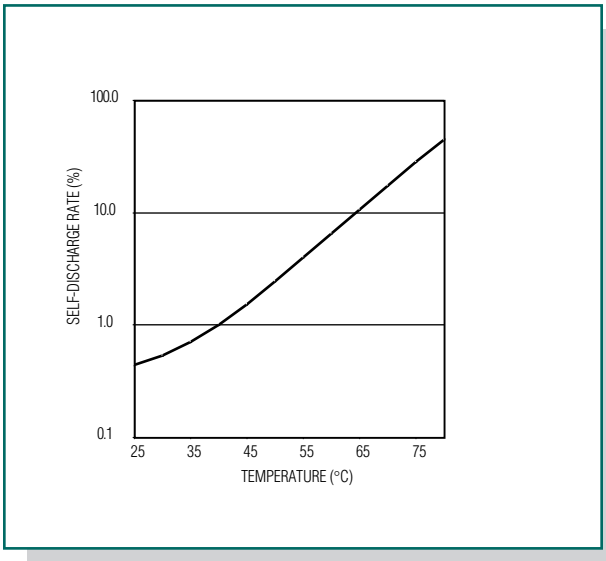

Figure 4. The self-discharge rate increases as temperature increases.

Sample lifetime calculations

Case I – The system is designed to be in battery backup 100% of the time at room temperature. The electrolyte evaporation at room temperature is so low that it can virtually be ignored. The lifetime is limited by the IC's current drain.

Electrical Consumption Leg

Battery capacity (BR1632) = 120mAh

IC current drain = 1.2µA

Duty cycle = 100%

Battery lifetime = (0.12Ah) / (1.2 x 10^{-6}A) = 100,000 hours = 11.4 years

Electrolyte Evaporation Leg

Battery lifetime at +25°C = 230 years

Calculation : (230 x 11.4) / (230 + 11.4) = 10.9 years

Case II – The system is designed to be in battery backup 50% of the time at +60°C. The lifetime due to either the electrical consumption or electrolyte evaporation would appear to be approximately 20 years. The combination of the two mechanisms will cause the electrolyte to be consumed in 10 years.

Electrical Consumption Leg

Battery capacity (BR1632) = 120mAh

IC current drain = 1.2µA

Battery lifetime = (0.12Ah x 50%) / (1.2 x 10^{-6}A) = 200,000 hours = 22.8 years

Electrolyte Evaporation Leg

Battery lifetime at +60°C = 19.1 years

Calculation: (19.1 x 22.8) / (19.1 + 22.8) = 10.4 years

Integrated battery controllers

If a system is to contain battery-backed SRAM or RTC, it is important to use an appropriate battery controller. These controllers handle the switching from system power supply to the battery in the event of power failure. They also provide the on-chip reverse-charging protection required by Underwriters Laboratory or other testing agencies. Dallas Semiconductor sells standalone battery controllers that allow the system designer to customize a system based on battery-capacity demands or layout constraints.

While the standalone battery controllers are well suited for certain applications, their use comes with some additional costs. Not only must end users select and acquire an appropriate battery, but the manufacturing process must also accommodate the particular battery requirements. Because of the limited available capacity in a battery, the manufacturing process must ensure that no inadvertent loads are placed on the battery. This requires that the batteries be handled with insulated or nonconductive tools while many other components in the design are ESD sensitive and should be handled with conductive tools.

The materials used in lithium battery construction limit their temperature exposure capabilities. A single pass through a reflow solder operation destroys the battery, which raises the question of whether the battery should be attached to the PCB with a mechanical holder or soldered to the PCB. A mechanical holder can be attached to the PCB using automated equipment and reflow solder. The battery is then inserted after the high-temperature processing is complete. The mechanical holder eliminates any temperature exposure to the battery, but the resulting system depends on the mechanical contacts holding the battery in place. Attaching the battery to the PCB with solder requires purchasing a tabbed battery and hand soldering that component after all reflow solder operations have been completed.

A final concern with using a battery controller and separate battery is the cleanliness of the manufacturing process. Even trace amounts of ionic contaminants can result in electrical leakage paths that can place loads on the batteries equal to the designed IC load. This will greatly shorten the system's effective life.

Battery module products

Using a module product that contains the battery controller and battery will avoid some of the problems discussed above. The module manufacturer will have the required processes to handle the batteries without degradation, and the module construction will also help isolate the battery from the end user's environment, thereby avoiding some of the ionic contamination issues. The end result can maximize battery lifetime.

In addition, many of the Dallas Semiconductor modules incorporate a "Sleep Mode" function that isolates the battery until system power is first applied. This feature allows the module products to be assembled and fully tested; the electrical load is then removed from the battery. Thus, the parts can be left in inventory for an extended period without removing any charge from the battery.

Conclusion

Dallas Semiconductor's battery-backup products are designed and manufactured to provide end users with a specified lifetime. This lifetime has been calculated under "worst case" conditions and assumes that the part will be in battery-backup 100% of the time. By understanding the mechanisms involved in the depletion of the battery, end users can reasonably and accurately predict system lifetimes based on the power-on duty cycle and the battery temperature exposure.

If users decide to select one of the battery controllers sold by Dallas Semiconductor and provide their own battery in the system, they should consider the battery's nature in the selection process. Proper IC screening and battery testing are required to ensure the available capacity is adequate to provide the desired lifetime.

Using a software interface with a 1-Wire temperature sensor in a microcontroller environment

There are several methods available for interfacing 1-Wire® devices such as the DS18B20, DS18S20, or DS1822 to a microcontroller. These methods range from simple software solutions to using a serial interface chip such as the DS2480 to incorporating Dallas Semiconductor's VHDL 1-Wire master controller in a custom ASIC. This article presents the most simple software solution for basic 1-Wire communication between a microcontroller and any number of DS18x20 or DS1822 temperature sensors.

Detailed timing and operation information for the DS18B20, DS18S20, and DS1822 is available in their respective data sheets, which can be obtained from the Maxim/Dallas website at www.maxim-ic.com.

Hardware configuration

The block diagram in **Figure 1** illustrates the simplicity of the hardware configuration when using multiple 1-Wire temperature sensors. A single-wire bus provides both communication access and power to all devices. Power to the bus is provided through the 4.7kΩ pullup resistor from a 3V to 5.5V supply rail. An almost unlimited number of 1-Wire devices can be connected to the bus because each device has a unique 64-bit ROM code identifier.

Interface timing

Communication with the DS18x20/DS1822 is achieved through the use of time slots, which allow

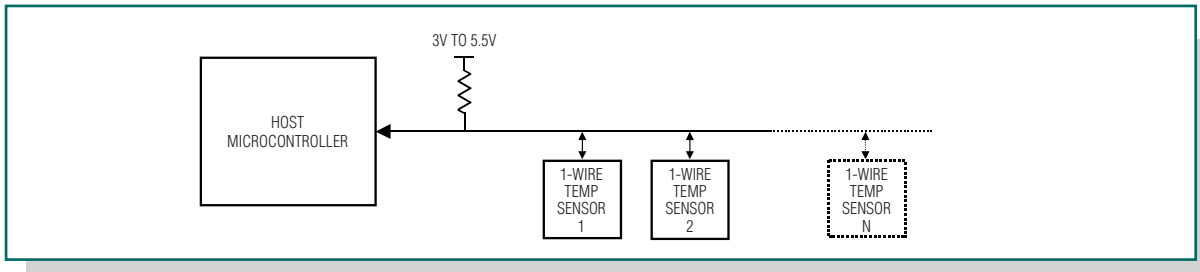

Figure 1. Multiple 1-Wire temperature sensors can be connected to a single-wire bus.

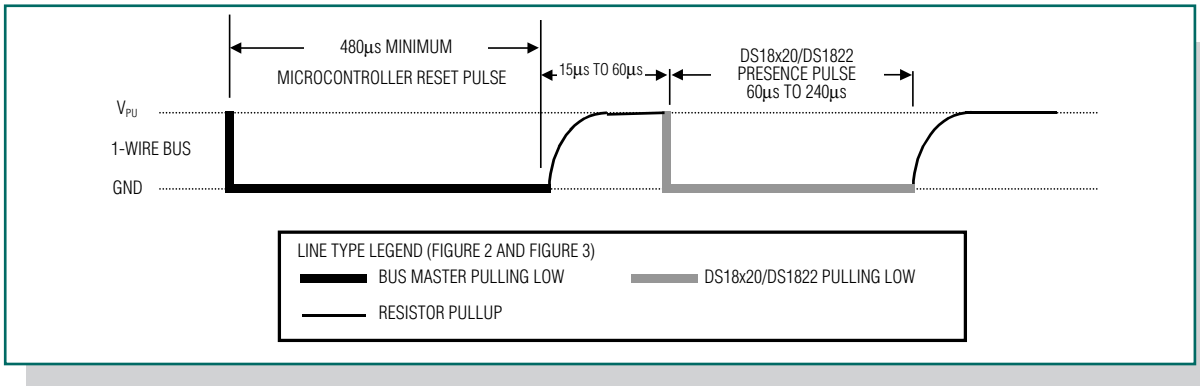

Figure 2. Every communication cycle begins with a reset pulse from the microcontroller followed by a presence pulse from the DS18x20/DS1822.

1-Wire is a registered trademark of Dallas Semiconductor.

data to be transmitted over the 1-Wire bus. Every communication cycle begins with a reset pulse from the microcontroller followed by a presence pulse from the DS18x20/DS1822 as shown in **Figure 2**.

A write time slot is initiated when the bus master pulls the 1-Wire bus from logic high (inactive) to logic low. All write time slots must be 60µs to 120µs in duration with a 1µs minimum recovery time between cycles. Write 0 and Write 1 time slots are illustrated in **Figure 3**. During the Write 0 time slot, the host microcontroller pulls the line low for the duration of the time slot. However, during the Write 1 time slot, the microcontroller pulls the line low and then releases the line within 15µs after the start of the time slot.

A read time slot is initiated when the microcontroller pulls the bus low for 1µs, then releases it so the DS18x20/DS1822 can take control of the line and present valid data (high or low). All read time slots must be 60µs to 120µs in duration with a minimum 1µs recovery time between cycles (Figure 3).

Software control

To accurately control the special timing requirements of the 1-Wire interface, certain key functions must first be established. The first function created must be the delay function, which is integral to all read and write control. This function depends entirely on the microcontroller's speed. For the purpose of this article, the DS5000 (8051 compatible) microcontroller is used, which runs at 11.059MHz. **Figure 4**'s example illustrates the C prototype function for creating the timing delay.

Since each communication cycle must begin with a reset from the microcontroller, the reset function is the next most important function to be implemented. The reset time slot is 480µs. By setting a delay of 3, followed by 25 (**Figure 5**), the reset pulse will last for the required duration. Following the reset, the microcontroller must release the bus so the DS18x20/DS1822 can indicate its presence by pulling the line low. If multiple temperature sensors

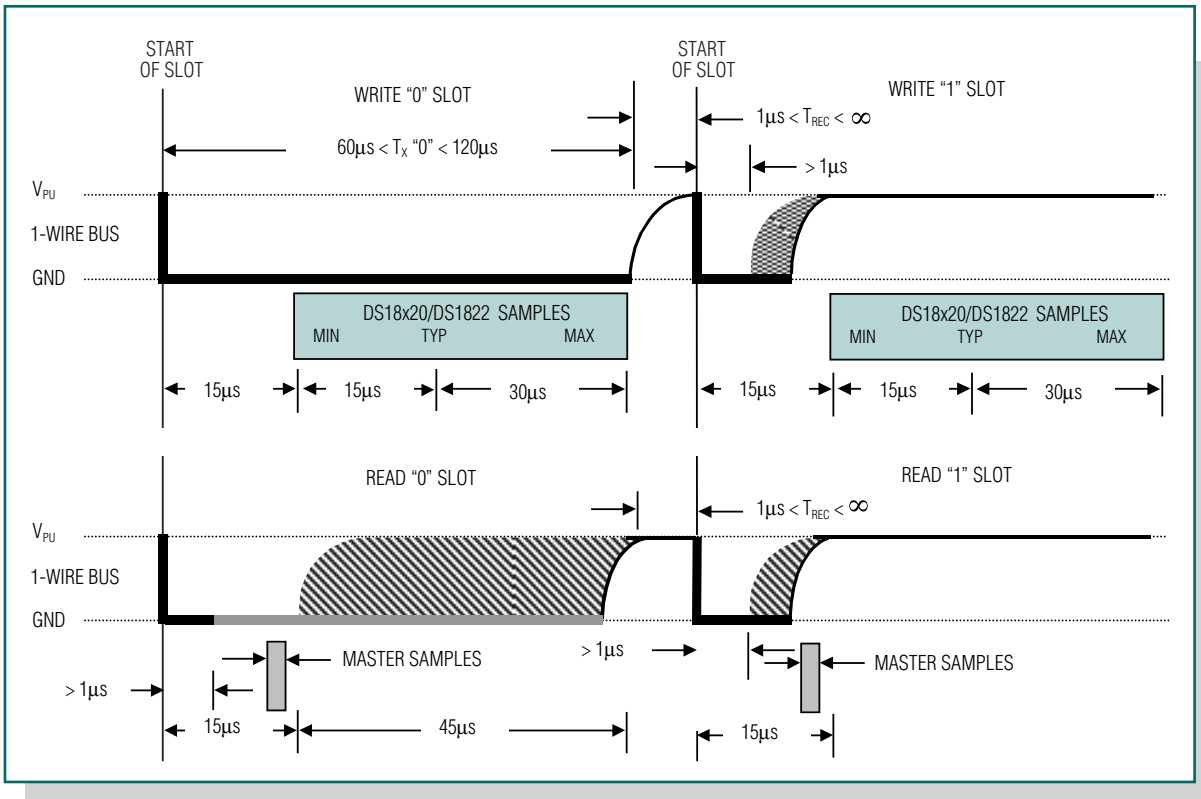

Figure 3. C prototype function for creating the timing delay.

are on the bus, they will all respond simultaneously with a presence pulse.

The read and write function examples shown in **Figures 6**, **7**, **8**, and **9** provide the basic structure needed for all data bit and data byte read and write operations.

```
// DELAY - with an 11.059MHz crystal
//  Calling the routine takes about 24µs, and then
//  each count takes another 16µs
//
void delay (int µs)
{
        int s;
        for (s = 0; s < µs; s++);
}
```

Figure 4. Delay example

```
unsigned char ow_reset(void)
{
    unsigned char presence;

        DQ = 0;             //pull DQ line low
        delay(29);          // leave it low for 480µs
        DQ = 1;             // allow line to return high
        delay(3);           // wait for presence
        presence = DQ;      // get presence signal
        delay(25);          // wait for end of timeslot
        return(presence);   // presence signal returned
}                   //    presence = 0,  no part = 1
```

Figure 5. Reset example

```
unsigned char read_bit(void)
{
        unsigned char i;

        DQ = 0; // pull DQ low to start timeslot
        DQ = 1; // then return high
        for (i = 0; i < 3; i++); // delay 15µs from
         start of timeslot
        return(DQ); // return value of DQ line
}
```

Figure 6. Read bit example

```
void write_bit(char bitval)
{
        DQ = 0; // pull DQ low to start timeslot
        if(bitval==1) DQ =1; // return DQ high if write 1
        delay(5);// hold value for remainder of timeslot
        DQ = 1;

}// Delay provides 16µs per loop, plus 24µs
   Therefore, delay(5) = 104µs
```

Figure 7. Write bit example

```
unsigned char read_byte(void)
{
        unsigned char i;
        unsigned char value = 0;

        for (i = 0; i < 8; i++)
        {
                if(read_bit()) value| = 0 x 01<<i;
        // reads byte in, one byte at a time and then
        //      shifts it left
                delay(6); // wait for rest of timeslot
        }
        return(value);
```

Figure 8. Read byte example

```
void write_byte(char val)
{
unsigned char i;
unsigned char temp;

for (i = 0; i < 8; i++)   // writes byte, one bit at a time
{
        temp = val>>i;    // shifts val right 'i' spaces
        temp &= 0x01;   // copy that bit to temp
        write_bit(temp);  // write bit in temp into
}
        delay(5)
}
```

Figure 9. Write byte example

Evaluating the DS80C320 as a drop-in replacement for the 8032

The DS80C320 high-speed, 8051-instruction-set-compatible microcontroller was designed with the same pinout and basic resources as a conventional 8032 but has significantly enhanced performance capabilities and a number of additional resources. Because the instruction set and pinout are the same, the DS80C320 can be used as a drop-in replacement. However, before doing so, users should consider the following issues.

Processor speed

While the DS80C320 is 100% compatible with the 8051 instruction set, the execution of the instructions has been streamlined for increased performance. A single byte instruction that previously required 12 clocks to complete now executes in 4 clocks. In addition, the DS80C320 can accept clocks up to 33MHz, whereas the maximum was 12MHz in some versions of the 8032. Because of this higher performance, processor speed must be considered when evaluating the DS80C320 as a drop-in replacement for the 8032.

Since the basic instruction execution time has been streamlined in the DS80C320, the time available to transfer data to and from memory has also been reduced. This means that for the same frequency crystal, there is less time available for memory access. A simple example illustrates this point. The data sheet for the 8032[1] stipulates that, when using a 12MHz crystal, the program memory must have an address access time faster than 302ns (neglecting any address latch overhead). A DS80C320 also using a 12MHz crystal requires a memory with an address access time faster than 230ns. While this is not a tremendous difference, it is something that must be considered and can be important in some systems. See Dallas Semiconductor's Application Note 57, "DS80C320 Memory Interface Timing," for details about selecting correct speed-memory devices.

Software timing must also be considered. Typically, software writers will use the presumed constant execution speed of a processor as a real-time reference. Often a tight loop that requires a known number of clocks to execute will be used for generating delays. Since the DS80C320 executes instructions much more quickly than the standard 8032, these previously designed timing loops will no longer produce the originally intended results. While using software timing loops is generally accepted as undesirable software design, in practice they are used rather frequently in embedded applications. The DS80C320 was designed so that the internal timers default to a condition where they behave exactly as the timers in the 8032. If application code is written to make use of these timers rather than software delays, the code will run as originally intended.

Power-on reset

The DS80C320 incorporates circuitry to generate its own power-on reset function. While the RST pin might still be connected to an external reset-generating circuit, this on-board feature is provided as a convenience for new designs. The fact that the processor has its own reset function is a benefit in most cases; however, there are situations where the on-board reset is not exactly what the user wants. What if the reset cannot be at the desired voltage level or what if it can't last for a desired time period, as in using battery-backed RAM for storage? If the RAM contains its own voltage-detection circuitry and does not become unprotected at the same voltage as the DS80C320 leaves reset (4.0V), then the processor could be accessing protected RAM. While these cases are not common, they remain something to consider for each specific application.

Power consumption

In addition to being a higher performance device, the DS80C320 is also a lower power device than the 8032

when equivalent work is considered. All CMOS devices consume more power as their speed increases. Since the DS80C320 is a higher speed part, it will consume more power for a given crystal frequency. However, if an equivalent amount of work is considered, it consumes slightly less power than a conventional 8032 as shown in **Figure 1**. This difference in power consumption is probably only important for battery-powered applications, in which case stop-mode power is likely to be more important.

Note 1. Intel *8-Bit Embedded Controllers* data book, 1991, taken from data for the 8032.

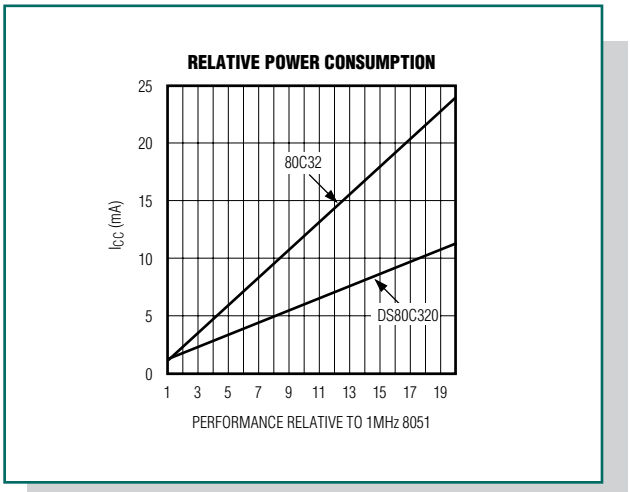

Figure 1. Reduced clock cycle core uses less current for same throughput.

Incorporating the 1-Wire master into an ASIC design

The 1-Wire Master (DS1WM) was created to facilitate host CPU communication with devices over a 1-Wire bus without concern for bit timing. This article shows how to incorporate the DS1WM into a user's ASIC design. The DS89C200 referred to in this document is a theoretical microcontroller. It is assumed the reader has knowledge of the DS1WM and Dallas Semiconductor's 1-Wire protocol. For more detailed information, refer to the "Book of iButton® Standards" (www.ibutton.com) and the DS1WM data sheet.

Structure

The DS1WM is arranged as a top-level harness that connects four submodules together to form a complete unit. There is no HDL code in the top-level harness. The four submodule files consist of the one_wire_interface, the one_wire_master, the clk_prescaler, and the one_wire_io. For applications that do not need the clock prescaler, this module can be left out if an external 1MHz clock source for the clk_1µs signal is supplied. (Noted as τ in the DS1WM data sheet, the input clock is specified from 0.8MHz to 1.0MHz.)

The one_wire_io module provides the bidirectional signals for the DATA and the DQ signals. In most applications, the DQ signal will be an I/O pin. If this is the case, the pad driver for DQ must be an open-drain pad with the proper ESD protection (**Figure 1**). Also, if the peripheral devices use a pull-up voltage that is greater than the DS1WM supply, a pad driver must be chosen that can tolerate the extra voltage; diode clamps must not be used. An output driver of 100Ω is recommended for Q1 and an external pull-up of 4.7kΩ to chip V_{CC} for DQ. Chip V_{CC} must be greater than V_{IH} of the 1-Wire slave for proper communication.

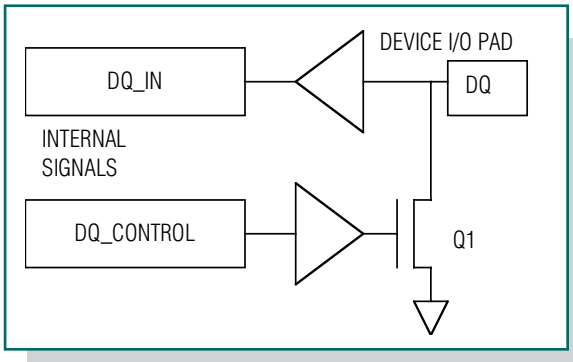

Figure 1. DQ pad driver (one_wire_io) must be an open-drain pad with the proper ESD protection.

No external libraries are required to compile the Verilog source. The VHDL source version requires both IEEE.std_logic_1164 and work.std_arith libraries.

Connections

Table 1 lists the wires that need to be connected for proper DS1WM operation.

If no address strobe is available in the system, the ADS_bar can be tied low, making the address latch transparent. The EN_bar signal should be generated by address-decode logic external to the DS1WM module. If the DS1WM is the only instance on the data bus, EN_bar can be tied low. The system clock wired to CLK must be between 3.2MHz and 128MHz.

Table 1. Wires for proper DS1WM operation

Pin	Operation
DQ	Open-drain, bidirectional 1-Wire bus connection
DATA	Bidirectional, 8-bit data bus
ADDRESS	3-bit address bus
ADS_bar	Address strobe
EN_bar	Instance enable
RD_bar	Read data strobe
WR_bar	Write data strobe
INTR	Interrupt detection
CLK	System clock
MR	Master reset

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Figure 2 shows how to create a DS1WM instance in Verilog.

```
module DS89C200 (...top level list...);
wire [7:0] DB;
wire [2:0] ADDR;
wire sysclk, read_bar,
    write_bar, master_reset,
    interrupt, addr_strobe;
wire DQ_OUT;

supply1 Tie1;
supply0 Tie0;

cpu xcpu(.CLK(sysclk),
        .DB(DB),
        .EXTRD_BAR(read_bar),
        .EXTWR_BAR(write_bar),
        .EXTADDR(ADDR),
        .RESET(master_reset),
        .EXTINTR(interrupt),
        .ADDR_ST(addr_strobe),
        ... other I/O signals ...);

onewiremaster xonewiremaster(
        .ADDRESS(ADDR),
        .ADS_bar(addr_strobe),
        .EN_bar(Tie0),
        .RD_bar(read_bar),
        .WR_bar(write_bar),
        .DATA(DB),
        .INTR(interrupt),
        .CLK(sysclk),
        .DQ(DQ_OUT),
        .MR(master_reset) );
... rest of design ...
```

Figure 2. Creating a DS1WM instance in Verilog

All signals generated by xcpu meet the DS1WM timing requirements. The EN_bar signal is tied low because there is no other addressable logic on the data bus. The DQ_OUT signal is wired directly to an I/O pad.

Synthesis

Synthesis of this design is very straightforward. A bottoms-up approach is recommended to compile the submodules individually and afterward to optionally compile the top level. Timing constraints need to be placed on the clk_1µs signal along with sysclk signal. Further timing constraints might be necessary for some of the asynchronous control signals such as WR_bar, RD_bar, EN_bar, ADS_bar, and MR. Additional constraints might be necessary for clk_1µs to keep buffers from being inserted on the clock signal. In most cases, it will be necessary to have a clock distribution strategy, such as a clock tree.

Included with the source code are example synthesis scripts and a Makefile that can be used with a Synopsys design compiler. It is necessary to create a .synopsys_dc.setup file that defines the target synthesis library. In addition, it is necessary to modify the included environment file (named “environment”) to specify the device from the target library to be used for specifying output-drive strengths and input loads. These example scripts are very generic. The actual scripts and constraint files are generated by the engineer to meet the timing requirements of the specific design. One thing to keep in mind is that the timing in the DS1WM block is not entirely synchronous by design. The DQ output is synchronized to CLK, but the bus read/write timing will only be synchronous to CLK if the CPU uses CLK to generate RD_bar, WR_bar, and ADS_bar. See the specification for the timing relationships for these signals.

This example design is fully self contained. It has been successfully compiled to FPGA and ASIC targets with success. When synthesized to a typical ASIC target library, the design uses about 110 flip-flops, three latches, and 1492 gates.

Building a 1-Wire pick-to-light system

A key cabinet provides an interesting example of a common requirement, i.e., the need to select a single key (or item) from a column and row array. For example, suppose one wanted the key to the supply cabinet. In the precomputer era, each key probably would have a handwritten label and a designated place to hang in the cabinet. The desired key was found by reading the tags or knowing the proper position in the cabinet where the key was stored. After use, the key would be returned to its original location. If the key became misplaced in the cabinet, it was necessary to examine each key's tag until the key in question was located and returned to its proper place.

Today, a computer or µP bus master can keep track of "keys" regardless of where they are placed in the array. The system is based on each key having a unique ID. For example, each key could have a computer-readable 1-Wire chip such as a DS2401 Silicon Serial Number permanently attached or embedded in it. When a particular key is required, the master turns on an LED at the position where it is located. When the key is returned to the cabinet, it can be placed in any arbitrary location because the bus master can determine its current location by reading its unique ID. The spatial array to hold the keys is designed around the DS2409 MicroLAN coupler and DS2406 dual addressable switch. The DS2409 selects the rows and the DS2406 selects the columns. This article provides the basics of a 1-Wire pick-to-light system.

Figure 1 shows two DS2409 high-side switches being used to select one of two rows, while a single

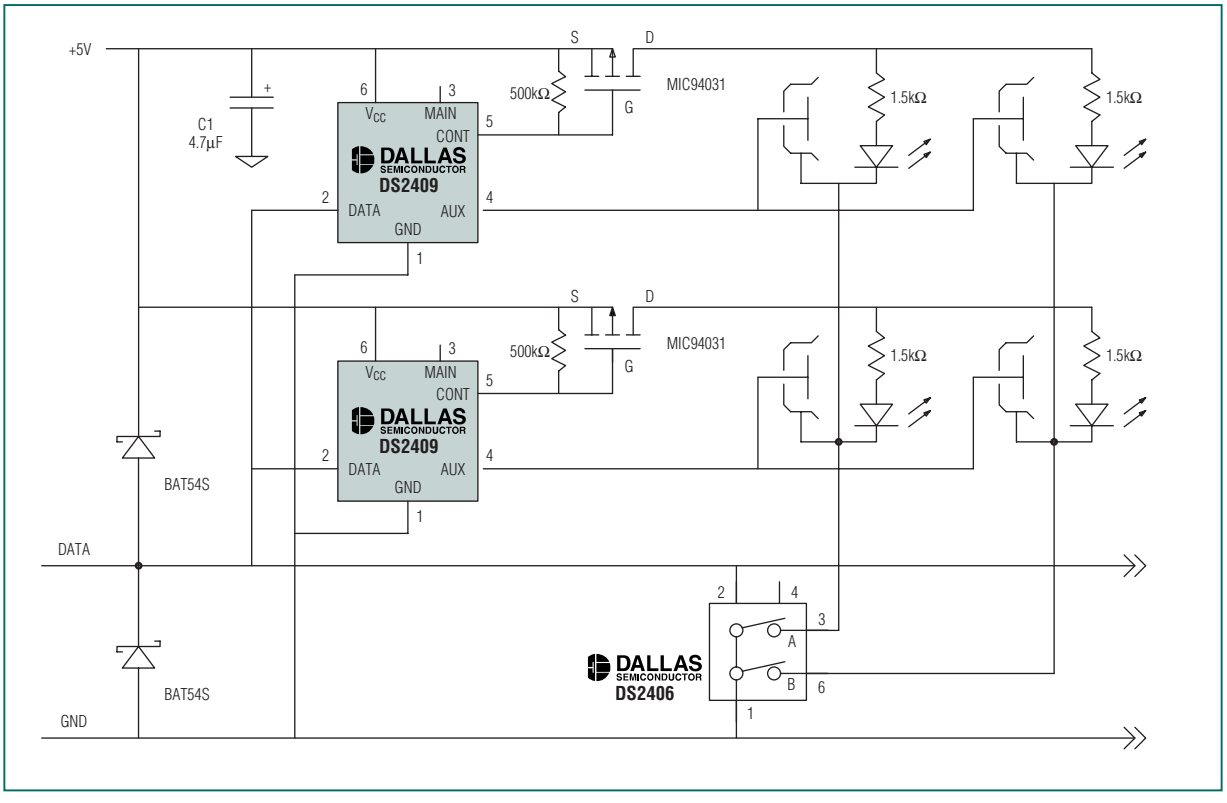

Figure 1. A combination of DS2409s and DS2406s can be used to build a pick-to-light system.

DS2406 dual low-side switch performs the same function for column selection. As shown, they form a simple 2 x 2 array with LEDs to visually provide indication of the specific intersection being addressed by the bus master. However, the array can be easily expanded in either the X or Y dimension by adding additional DS2409s and/or DS2406s to generate more rows or columns, respectively. In this manner, an M x N array of any required size can be implemented limited only by net loading. Where the schematic shows an iButton port, a blue-dot receptor or even solder-mount connectors such as the board mount DS9098P can be substituted.

In operation, the master selects the auxiliary output of the DS2409 that controls the row of interest and the column output of the corresponding DS2406 that intersects that row at the required key. For example, if the auxiliary output of the top DS2409 and the B output of the DS2406 are both turned on, the position in the upper right-hand corner is selected. This connects the iButton port at the intersection of the selected row and column to the master so the serial number ID of the 1-Wire chip on the key at that position can be read if present. To visually indicate which intersection is being addressed, the master switches the selected DS2409 from its auxiliary output to its main output. By default, this causes the CONT pin to turn on, grounding the gate of the associated PMOS transistor and turning it on. With the pass transistor on, power is supplied to the LED at the selected intersection and turns it on. If desired, the DS2409 can be repeatedly switched between main and auxiliary outputs, causing the selected LED to blink for greater visual impact. If the main output of all DS2409s are turned on, the LEDs in the entire column of the selected DS2406 output are turned on. Alternatively, if the outputs of all DS2406s are turned on, the LEDs in the entire row of the selected DS2409 are turned on. Consequently, it follows that turning on all column and row switches will illuminate the entire array, which serves as a convenient test to verify that the system is fully functional.

Although this article uses the idea of the familiar key cabinet as an example, the pick-to-light system is broadly applicable to stocking and warehousing, in which case the columns and rows of the given example relate to aisles and shelves. The concept applies equally to halls and corridors of a building where the doors and entry ways would be the “keys” of our example. Other applications such as a digital display will become obvious as the fundamental nature of the pick-to-light concept is appreciated. For improved tracking, a 1-Wire device with memory such as the DS2430 can be used instead of the DS2401, which permits documentation to be stored with the item to minimize the probability of handling errors.