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# Benefits of Ultralow Noise Switching Regulator in Noise-Sensitive RF Applications

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## Abstract

Featuring ultralow noise, high efficiency, small size, and high current, the novel ultralow noise switching regulator is very suitable for noise-sensitive RF applications, including 5G/wireless, defense, instrumentation, etc. The advanced switching regulator family with ultralow output noise, known as Silent Switcher® 3, has even lower noise than most low dropout (LDO) regulators in the low frequency range (0.1 Hz to 100 kHz). This article investigates the challenges and system benefits of applying the ultralow noise switching regulator in noise-sensitive RF systems, compared to a traditional buck + LDO regulator solution. The investigation is based on two representative case studies of RF applications: a high performance phase-locked loop (PLL) clock and an advanced high speed ADC system. With proper control loop and filter design, the novel single-stage solution based on an ultralow noise switcher saves PCB space and cost for customers and features a smaller solution size, simplified structure, and higher efficiency, while still supporting excellent system performance.


## Introduction

RF systems are imposing stricter requirements on the noise performance of power solutions, which are used in a variety of applications including aerospace and defense, 5G wireless applications, medical equipment, instrumentation, etc. Ensuring low output noise from power solutions is one of the key aspects of maintaining superior system performance. The market share of noise-sensitive RF applications is hence expanding rapidly. Traditionally, buck + LDO regulator power tree solutions dominate these noise-sensitive applications. However, as the load consumes increasingly high current in next-generation products, the buck + LDO regulator solution becomes the system bottleneck, suffering from large solution size, high solution cost, and high loss due to the limited current capability of LDO regulators.

In recent years, the ultralow noise switching regulator has been developed with superior electromagnetic interference (EMI) performance and ultralow low frequency (LF, 0.1 Hz to 100 kHz) noise.[1,2,3] The LF noise of the state-of-the-art ultralow noise switching regulator is comparable with the best ultralow noise LDO regulator in the market. The advanced ultralow noise switching regulator is a game changer in noise-sensitive applications, providing ultralow noise, high current capability, high efficiency, and small size simultaneously.

The innovative ultralow noise switching regulator family, Silent Switcher 3, features industry-leading performance in all four aspects.[1] ADI's Silent Switcher 1 and 2 families have been the pioneering switching regulator with high efficiency, low EMI noise, and small solution size, supporting input voltages up to 65 V and output currents up to 30 A. Based on successful Silent Switcher 1 and 2 technologies, Silent Switcher 3 technology has been designed to efficiently deliver much higher current than LDO regulators, with one single IC delivering up to 16 A current with a small 4 mm × 4 mm package. Compared to the Silent Switcher 2 family, the Silent Switcher 3 family adopts an innovative circuit and structure design to achieve ultralow LF output noise.[1] As shown in Table 1, the output noise of the Silent Switcher 3 regulator at low frequency range is lower than LDO regulators without ultralow noise design. As a result, a single-stage power solution based on a single ultralow noise switching regulator is highly competitive to replace the traditional buck + LDO regulator solution in noise-sensitive RF applications. This article will use several case studies to introduce the superior system performance and system benefits of leveraging the ultralow noise switching regulator, Silent Switcher 3, in noise-sensitive applications. Details will also be presented to cover how to make the best of the superior device-level performance of the Silent Switcher 3 regulator to achieve the desired system-level performance.

## Powering PLLs with Ultralow Noise Switching Regulator

Numerous components and systems in RF systems are sensitive to noise, such as PLLs, high speed ADCs/DACs, mixed-signal front ends MxFE®, etc. Particularly, the high performance PLL is one of the most essential components in a RF system, as it provides the high quality clock signal required by ADCs, DACs, FPGAs, and other digital and mixed-signal ICs. This section investigates how to leverage a single-stage solution based on Silent Switcher 3 technology to power the high performance PLL and realize excellent PLL performance. The ADF4372, a popular high performance PLL frequency synthesizer rated at 5 GHz, is selected for this investigation.[4] The detailed power supply structure is displayed in Figure 1, as well as the demo board used for the experimental investigation.

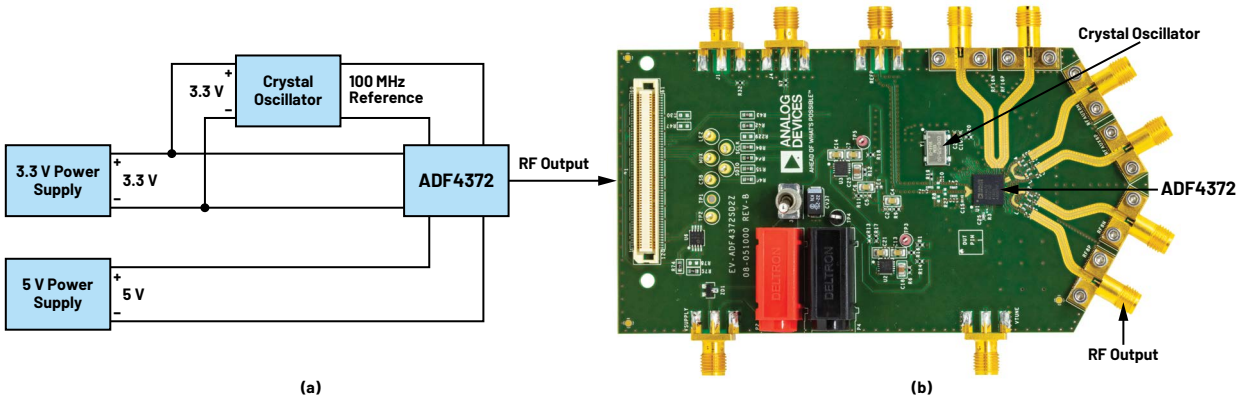


*Figure 1. (a) A detailed power supply structure of ADF4372; (b) A demo board of the ADF4372.*

## Table 1. Comparison of Output Noise of Different Power Supplies

| Power Supply | Integrated Noise (10 Hz to 100 kHz) |
|---|---|
| Ultralow noise LDO regulator (LT3045) | 0.8 µV rms |
| Li-Ion battery | 2.7 µV rms |
| Silent Switcher 3 regulator (LT8625S, high bandwidth) | 2.7 µV rms |
| Silent Switcher 3 regulator (LT8625S, low bandwidth) | 4 µV rms |
| LDO regulators without ultralow noise design | 20 µV rms to 100 µV rms |

In RF applications, the performance of high performance PLLs is evaluated with a key specification, phase noise. Phase noise is calculated as the power of noise in 1 Hz bandwidth normalized based on the power of the main RF signal, with a detailed definition shown in Equation 1.

$$Phase\ Noise = 10 \times log_{10}\left(\frac{Noise\ Power\ Density\ in\ 1\ Hz\ Bandwidth}{Carrier\ Power}\right) \quad (1)$$

Hence, phase noise is always a negative number, and it should be as low as possible. The unit of phase noise is dBc/Hz, where c means it is normalized based on the carrier power. As displayed in Figure 1, the ADF4372 requires two power rails, 3.3 V and 5 V, and 5 V is the most sensitive one as it powers the voltage-controlled oscillator (VCO) inside the PLL.[4] In this case study, 3.3 V is always provided by an ultralow noise LDO regulator (LT3045), while 5 V is powered by the Silent Switcher 3 regulator to study the impact the Silent Switcher 3 regulator on the phase noise of the RF output signal.

Figure 2 offers a baseline evaluation of the PLL phase noise performance with its 5 V rail supplied by a single-stage solution based on the Silent Switcher 3 regulator (LT8625S).[2] The baseline evaluation is conducted with an LT8625S demo board with minimal changes made to supply 5 V. In this case, the ADF4372 can still achieve excellent phase noise, as shown in Figure 2. From 10 Hz to 100 kHz, the measured phase noise is almost the same as the case where 5 V is powered by the ultralow noise LDO regulator. Yet there is a spike at ~250 kHz, leading to slightly higher phase noise at 100 kHz to 500 kHz. The phase noise spike at ~250 kHz is caused by the output noise of the Silent Switcher 3 regulator, which also has a plateau in such frequency range. The output noise of the Silent Switcher 3 regulator propagates to the phase noise of the output RF signal because the VCO output is highly sensitive to its power supply noise.

The output noise spike of the Silent Switcher 3 regulator results from the low control loop gain (~0 dB), which is too weak to drive down the output noise in this frequency range. The mechanism is well explained in the data sheet of the Silent Switcher 3 family.[2] Therefore, the noise spike can be decreased by tuning the compensation to increase the control bandwidth of the Silent Switcher 3 regulator. Hence, the phase noise can be further reduced by optimizing the control loop of the Silent Switcher 3 regulator for higher control bandwidth, as demonstrated in Figure 3. The baseline phase noise evaluation result in Figure 2 is obtained with the Silent Switcher 3 regulator with slow compensation and low control bandwidth. By optimizing the control loop and achieving high bandwidth, the phase noise spike at ~250 kHz is almost eliminated with a reduction of over 10 dBc/Hz. Still, the single-stage solution based on the Silent Switcher 3 regulator leads to slightly higher phase noise than the 2-stage solution with ultralow noise LDO from 100 kHz to 500 kHz.

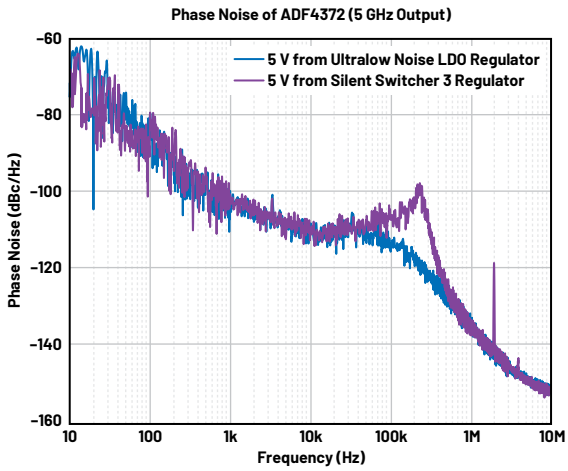


*Figure 2. Baseline comparison of phase noise with 5 V from ultralow noise LDO regulator (LT3045) and Silent Switcher 3 regulator (LT8625S).*

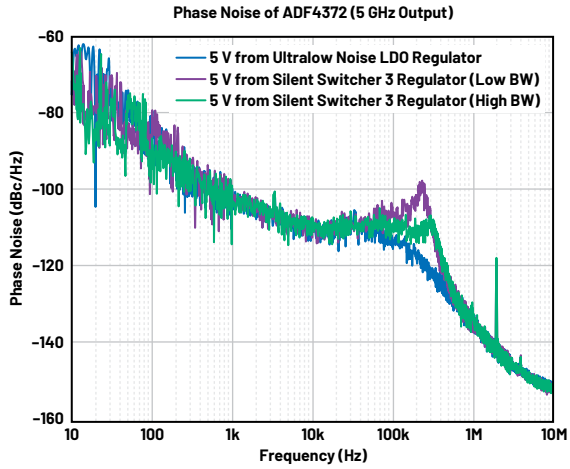


*Figure 3. Impact of the Silent Switcher 3 regulator control bandwidth on phase noise of a high performance PLL.*

To further enhance phase noise performance powered by the Silent Switcher 3 regulator, a secondary (second) LC filter can be designed and added to the output of the Silent Switcher 3 regulator. A detailed circuit diagram is displayed in Figure 4 to illustrate a single-stage solution based on the Silent Switcher 3 regulator with a second LC filter used to power the 5 V rail. With a second LC filter, the output voltage can be sensed from either the local output or the remote output side after the second LC filter. In this case, the local output is selected for output voltage sensing to simplify the control loop design. Since the high performance PLL consumes low current (typically lower than 1 A), the voltage drop across the second LC filter is small, which makes it reasonable to only sense the local output voltage. The local output capacitance is hence selected to guarantee the stable operation of the Silent Switcher 3 regulator. Then, the general design guidelines recommend the remote output capacitance should be higher than the local output capacitance to make system stability less sensitive to the load capacitance.[5]

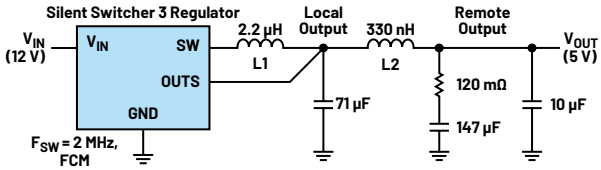


*Figure 4. A circuit diagram of the Silent Switcher 3 regulator with a second LC filter to provide 5 V for the PLL.*

With both the local and remote output capacitance determined, the second inductor L2 can be selected based on the cutoff frequency, or the resonance frequency of the second LC filter. Based on Figure 3, the design target is to achieve >10 dBc/Hz attenuation at 250 kHz, which requires the second LC filter to produce at least 20 dB attenuation at 250 kHz. 30 dB attenuation at 250 kHz is used to provide a higher margin, and hence the second LC filter (with –40 dB/dec attenuation) should have a cutoff frequency of 44.6 kHz. The calculated inductance of the second LC filter is thus 260 nH. The final inductance is selected as 330 nH with the inductance tolerance (typically ±20%) considered. Last but not the least, sufficient damping should be achieved in the second LC filter design, where the design rule of thumb is the quality factor Q should be lower than 1.[5] So, 120 mΩ damping resistance is added and in series with the remote output capacitor, leading to a valid Q of 0.7.

Equipped with the designed second LC filter in Figure 4, the Silent Switcher 3 solution supports almost the same phase noise performance as the 2-stage solution with an ultralow noise LDO regulator. As shown in Figure 5, the designed second LC filter further elevates the phase noise performance powered by the Silent Switcher 3 regulator, leading to almost the same result from 10 Hz to 10 MHz as the ultralow noise LDO regulator. Although the phase noise result powered by the Silent Switcher 3 regulator still has a small spur at 2 MHz due to its switching frequency, the small spur has a predictable frequency that is far away from the carrier frequency and hence not difficult to tackle.

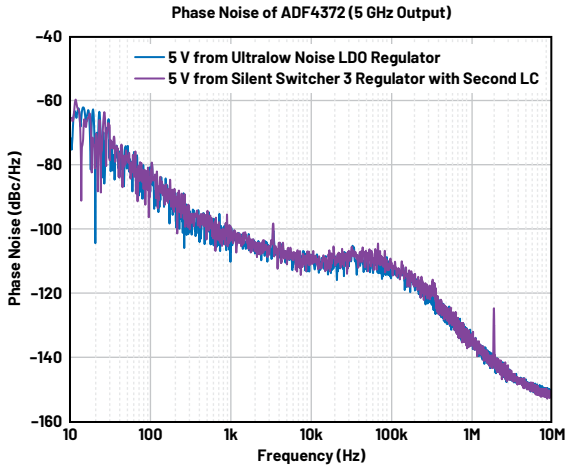


*Figure 5. A comparison of the ADF4372 phase noise with 5 V from ultralow noise LDO regulator (LT3045) and the Silent Switcher 3 regulator (LT8625S) with a second LC filter.*

Moreover, with or without the designed second LC filter, the Silent Switcher 3 solution supports much lower phase noise than the Silent Switcher 2 regulator (LTM8024) and the regular switching regulator from a different vendor. As demonstrated in Figure 6a, as an ultralow noise step-down switching regulator, the Silent Switcher 3 regulator supports substantially lower phase noise from 1 kHz to 500 kHz, compared to the Silent Switcher 2 regulator and the regular switching regulator. At <1 kHz, there is no difference in measured phase noise powered by different power supplies. This is because the phase noise of the high performance PLL at such a low frequency is dominated by the reference clock of the PLL, instead of its power supply. Furthermore, the Silent Switcher 3 regulator can achieve lower phase noise than an LDO regulator without a special design for ultralow noise, as shown in Figure 6b. The phase noise difference is >10 dBc/Hz from 5 kHz to 100 kHz, where the Silent Switcher 3 regulator outperforms LDO regulators without ultralow noise design in output noise (shown in Table 1). In summary, with proper control loop and filter design, a single-stage solution based on the Silent Switcher 3 regulator can support almost the same PLL performance as the 2-stage solution with an ultralow noise LDO regulator. A single-stage solution based on the Silent Switcher 3 enables better PLL phase noise than the 2-stage solution with an LDO regulator without ultralow noise design.

## Powering ADC Systems with Ultralow Noise Switching Regulator

This section focuses on the ADC system benefits of leveraging the single-stage power solution based on the Silent Switcher 3 regulator. ADC systems are widely used in numerous RF applications, such as 5G/wireless, defense, etc. An ADC system is typically composed of a PLL clock, an ADC, and a digital processor. In this

case study, an advanced high speed ADC is selected, the AD9208 with 9 GHz bandwidth.[6] The ADF4372 demo board is still used to provide clock signals for the system. An analog signal (1.23 GHz with a magnitude of –10 dBFS) is generated as the input signal of the ADC. On the digital side, a high speed FPGA board (ADS7-V2EBZ board) and ACE software are used to examine the digital signal and evaluate the ADC performance. Details of the ADC system can be seen in Figure 7.

In the first part of this ADC case study, ADC system performance and benefits of the Silent Switcher 3 regulator as the PLL clock power supply are studied. Again, the 3.3 V rail of the ADF4372 is always from an ultralow noise LDO regulator (LT3045), while the 5 V rail is supplied by the Silent Switcher 3 solution or other power solutions. Also, the AD9208 is always powered by the default power solutions installed on the standard demo board. Under the same analog input signal, Figure 8 shows the average fast Fourier transform (FFT) result of the ADC output signal near 1.23 GHz with a frequency span of 2 MHz under different PLL clock power supplies. Compared to other switching regulators, the Silent Switcher 3 regulator enables the best ADC performance with the lowest noise near 1.23 GHz, although its FFT waveform still has a plateau at ~250 kHz frequency offset.

ADC system performance is sensitive to the quality of its sampling clock signal, that is, the phase noise. This plateau at ~250 kHz coincides well with the small spike at the same frequency in the phase noise plot of the ADF4372 output signal (green curve in Figure 3). As revealed in the PLL case study, this small spur in the phase noise plot can be eliminated by adding a filter. Therefore, the ADC performance enabled by the Silent Switcher 3 regulator as the clock power supply can be elevated by adding a second LC filter, which is well supported by experimental results. Figure 9 displays the FFT result of ADC output under the Silent Switcher 3 solution with the second LC filter design in Figure 4. The resulting output FFT waveform of the ADC output features exceptionally low noise near the main 1.23 GHz signal, which is almost the same as the ultralow noise LDO regulator result. Not surprisingly, Figure 9 also reveals that the FFT result under the Silent Switcher 3 regulator with the designed second LC filter outperforms that under the LDO regulator without ultralow noise design at <100 kHz frequency offset, owing to its lower LF noise and the resulting PLL clock signal with lower phase noise.

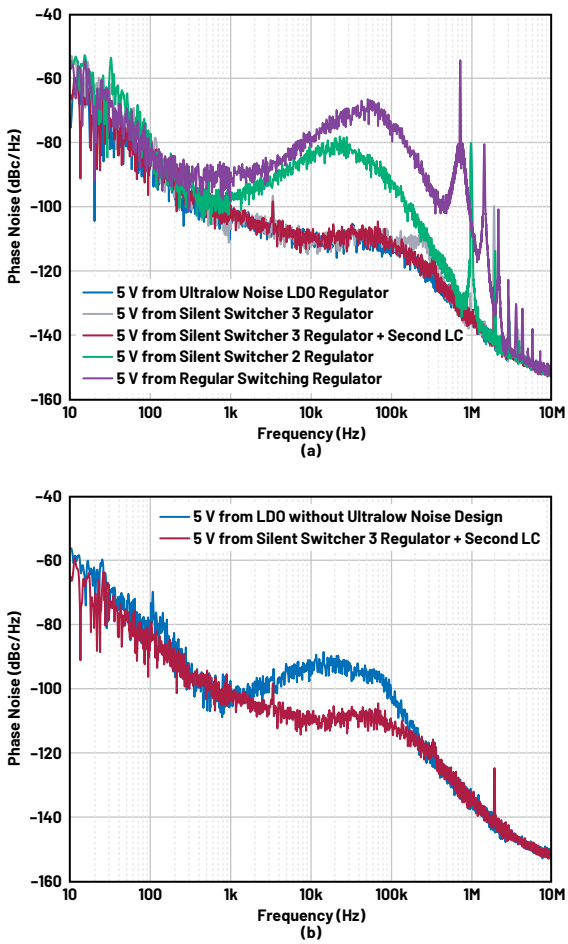


*Figure 6. Phase noise of PLL clock (ADF4372) under different power supplies: (a) phase noise of ADF4372 (5 GHz Output); (b) phase noise of ADF4372 (5 GHz output).*

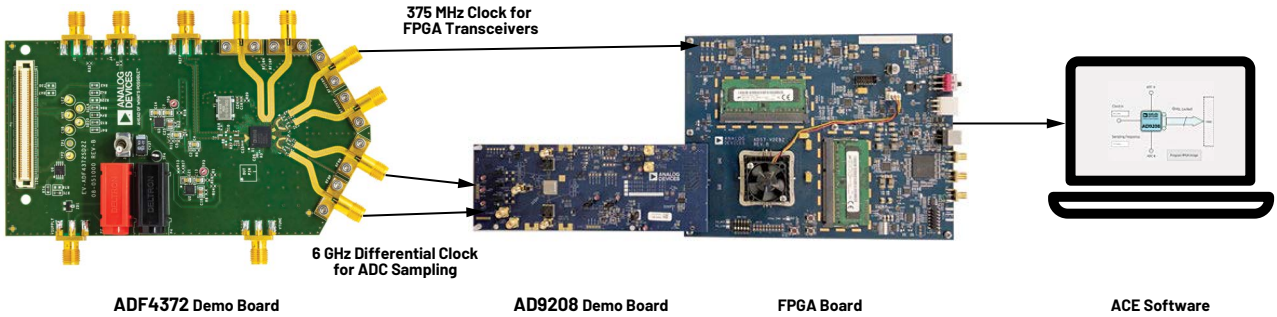


*Figure 7. A detailed structure of the advanced ADC system under study.*

In addition to the FFT result of ADC output, two important ADC parameters, signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR), have also been evaluated to assess the ADC system performance more comprehensively.[6] The definition of SNR is straightforward; while SFDR is defined as the rms magnitude of the input signal over the highest rms magnitude of any spurious noise signal. Instead of a narrow frequency span near the frequency of the input signal, the calculation of both SNR and SFDR takes into account noise over a wide frequency range. As shown in Table 2, the Silent Switcher 3 solution without any LDO regulator for postregulation results in the same SNR and SFDR of the AD9208 as those supported by the traditional 2-stage solution with an ultralow noise LDO regulator. The second LC filter has little impact on the measured SNR and SFDR. Moreover, the Silent Switcher 3 solution results in much higher SNR and SFDR than other switching regulator solutions: ~20× the SNR (in decimal) and ~45× the SFDR (in decimal) caused by the regular switching regulator. As for the comparison with the LDO regulator without ultralow noise design, the Silent Switcher 3 solution results in slightly better SNR and the same SFDR, because its advantage only lies in the noise near the input frequency accounting for a small part of the noise used for SNR calculation.

**Table 2. Comparison of SNR and SFDR of the AD9208 with Different Power Supplies for ADC Sampling Clock**

| Power Supply of ADC Sampling Clock | SNR of ADC in Decimal | SNR of ADC in dBFS | SFDR of ADC in Decimal | SFDR of ADC in dB |
|---|---|---|---|---|
| Ultralow noise LDO regulator (LT3045) | 794.3 | 58 dBFS | 922.6 | 59.3 dB |
| Silent Switcher 3 Regulator with second LC filter (LT8625S) | 794.3 | 58 dBFS | 922.6 | 59.3 dB |
| Silent Switcher 3 Regulator without second LC filter (LT8625S) | 758.6 | 57.6 dBFS | 922.6 | 59.3 dB |
| LDO without ultralow noise design | 767.4 | 57.7 dBFS | 922.6 | 59.3 dB |
| Silent Switcher 2 Regulator | 126 | 42.0 dBFS | 56.2 | 35.0 dB |
| Regular Switching Regulator | 43.2 | 32.7 dBFS | 20.9 | 26.4 dB |

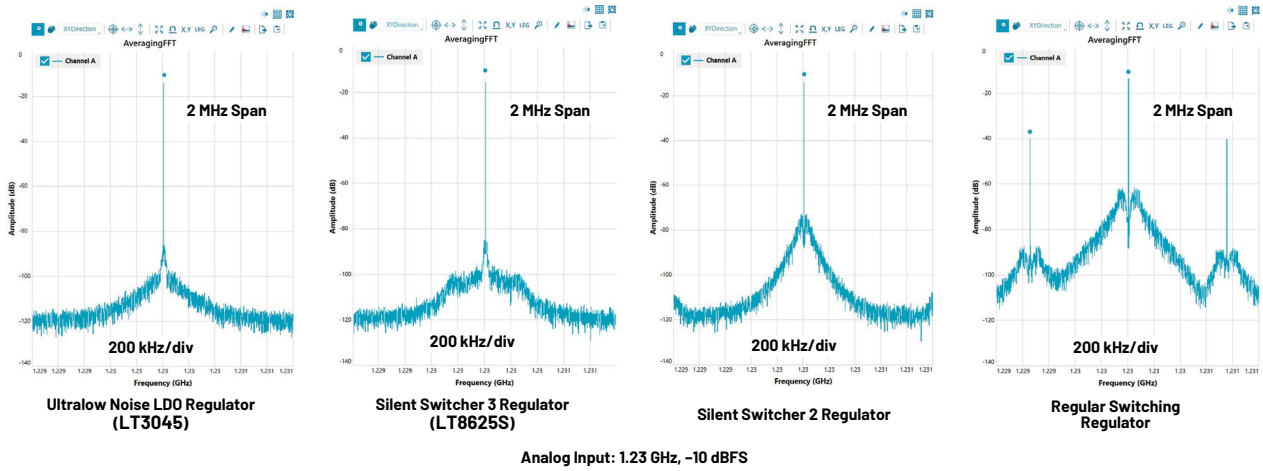


*Figure 8. An average FFT result of ADC output signal under different power supplies for ADC sampling clock (ultralow noise LDO regulator, Silent Switcher 3 regulator, Silent Switcher 2 regulator, and regular switching regulator).*

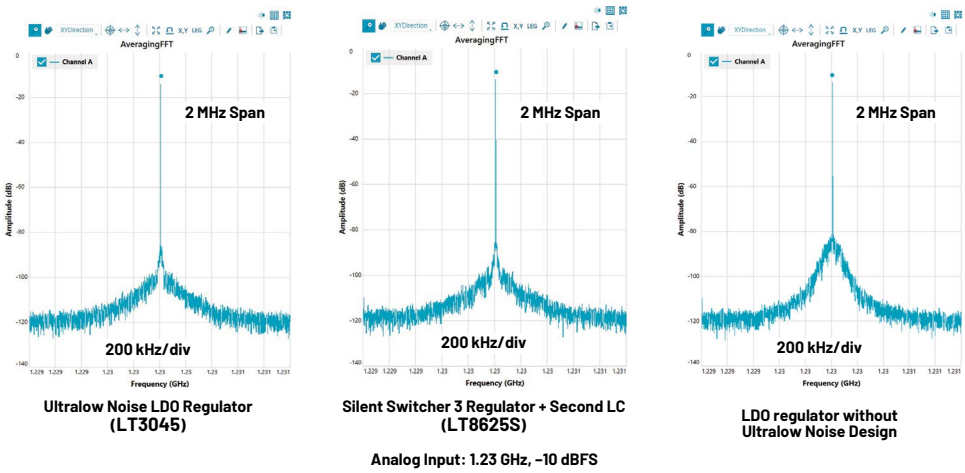


*Figure 9. An average FFT result of ADC output signal under different power supplies for ADC sampling clock (Silent Switcher 3 regulator with second LC filter, LDO regulator without ultralow noise design).*

The other aspect of this case study is to explore the ADC system performance and benefits when using the Silent Switcher 3 regulator to power the ADC. In this part, the PLL clock is always powered by the default 2-stage solution with an ultralow noise LDO regulator (LT3045) to focus on the impact of the ADC power supply. In particular, an analog rail of the AD9208, AVDD1, is selected as an example to simplify the investigation. Accounting for 19% of total power, the 0.975 V AVDD1 rail consumes 640 mA nominal current and provides power for the clock domain.[6] It is sensitive to power supply noise and hence selected based on both theoretical and empirical analysis. All other rails are still powered by the default power solutions installed on the standard demo board.

Experimental results prove that the single-stage Silent Switcher 3 solution can replace the traditional 2-stage solution to power the ADC without compromising ADC performance. The average FFT result of the ADC output is analyzed thoroughly to evaluate ADC performance with a Silent Switcher 3 solution (LT8625S) serving as AVDD1. It should be noted that the second LC filter is not installed. As displayed in Figure 10, the FFT result of the ADC output with the Silent Switcher 3 regulator powering the AVDD1 is almost ideal, as satisfactory as the FFT result with the AVDD1 from the 2-stage solution (buck + ultralow noise LDO regulator). There is no spike at ~250 kHz frequency offset even if the second LC filter is not installed.

Also, the ADC performance is not very sensitive to the low frequency noise of the ADC power supply. Instead, its performance is more sensitive to the switching ripple of ADC power supplies. With a 2 MHz switching frequency, the single-stage solution based on the Silent Switcher 2 regulator also led to an almost ideal ADC output waveform near the fundamental frequency (1.23 GHz), although the Silent Switcher 2 regulator does not have optimized low frequency noise performance. This is because the ADC output noise near the fundamental frequency is dominated by the phase noise of its sampling clock, as demonstrated in the first part of this case study. In other words, the output noise of a high speed ADC near the fundamental frequency is not very sensitive to the ADC power supply noise. Still, using a regular switching regulator with too high LF noise as the AVDD1 will make the ADC output noise worse near the fundamental frequency, as shown in Figure 10. Figure 10 also reveals that the switching ripple of the ADC power supply will propagate to the ADC output, leading to considerable spurs at the FFT result of the ADC output. For example, the regular switching regulator with 750 kHz switching frequency as the AVDD1 results in >30 dB spur at 750 kHz frequency offset. This is well supported by previous literature investigating the impact of switching ripple noise on the performance of high speed data converters (ADCs and DACs).[7, 8] Hence, with proper filter design, a single-stage solution based on the Silent Switcher 3 technology is well qualified to meet the power supply requirements of ADCs and support satisfactory performance.

In conclusion, the single-stage power solution based on the Silent Switcher 3 technology can replace the traditional 2-stage solution with an ultralow noise LDO regulator to power both the PLL clock and the high speed ADC in an advanced ADC system. The single-stage solution based on the Silent Switcher 3 technology can still support satisfactory ADC system performance, with key ADC parameters not compromised compared to the traditional buck + LDO regulator solution, including SNR, SFDR, noise performance, etc. Also, ADC performance is more sensitive to the power supply noise of its sampling clock source, compared to its own power supply noise. Therefore, proper control loop and output filter design are required for the Silent Switcher 3 technology to power the advanced ADC system with satisfactory system performance, especially its PLL clock.

## Ultralow Noise Switching Regulator-Based Power Tree for ADC System

The previous sections have proven that the Silent Switcher 3 technology is very suitable for powering the high performance PLL and the high speed ADC of an advanced ADC system. The Silent Switcher 3 technology is capable of meeting the power supply requirements of an advanced ADC system without compromising the system performance. Hence, a brand new and simplified power tree can be designed for the ADC system without any LDO regulators, which is purely based on Silent Switcher 3 ICs. In other words, the traditional 2-stage solution (buck + LDO regulator) is completely replaced by the single-stage solution based on an ultralow noise switching regulator, Silent Switcher 3. Based on the ADC system case study in the previous section, Figure 11 compares the original power tree of the ADC system (ADF4372 + AD9208) and the new simplified power tree based on Silent Switcher 3 technology. The original power tree structure is based on the power solutions used in the standard demo boards of the AD9208 and ADF4372; while the new power tree is designed based on the latest Silent Switcher 3 parts for low current applications (the LT8622S and LT8624S).

Without any LDO regulators, the new power tree can facilitate significant and comprehensive system benefits. As shown in Figure 11, the power tree based on Silent Switcher 3 technology is a simplified structure with only five Silent Switcher 3 ICs, while the original power tree requires two switching regulators and six LDO regulators. The new power tree can hence save plenty of PCB area and cost. Also, the new power tree structure can substantially boost efficiency, with efficiency increasing from 61.7% to 84.8%. The total power loss is reduced by 71%, from 3.919 W to 1.136 W. The LDO regulator stage of the traditional power tree structure consumes 2.305 W power loss by itself. Such a significant reduction in total power loss is not only attributed to the elimination of LDO regulators, but also the high efficiency of Silent Switcher 3 ICs even with a 2 MHz switching frequency. The

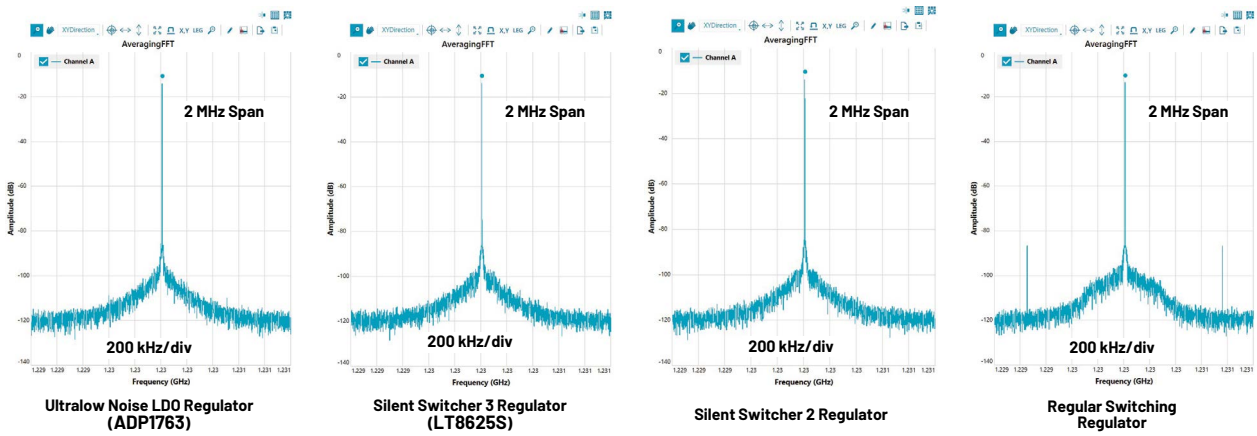


*Figure 10. An average FFT result of ADC output signal under different power supplies providing AVDD1 (ultralow noise LDO regulator, Silent Switcher 3 regulator, Silent Switcher 2 regulator, and regular switching regulator).*

efficiency of the power tree based on Silent Switcher 3 technology can be further improved with future ultralow noise switching regulators specifically developed for <1 A applications.

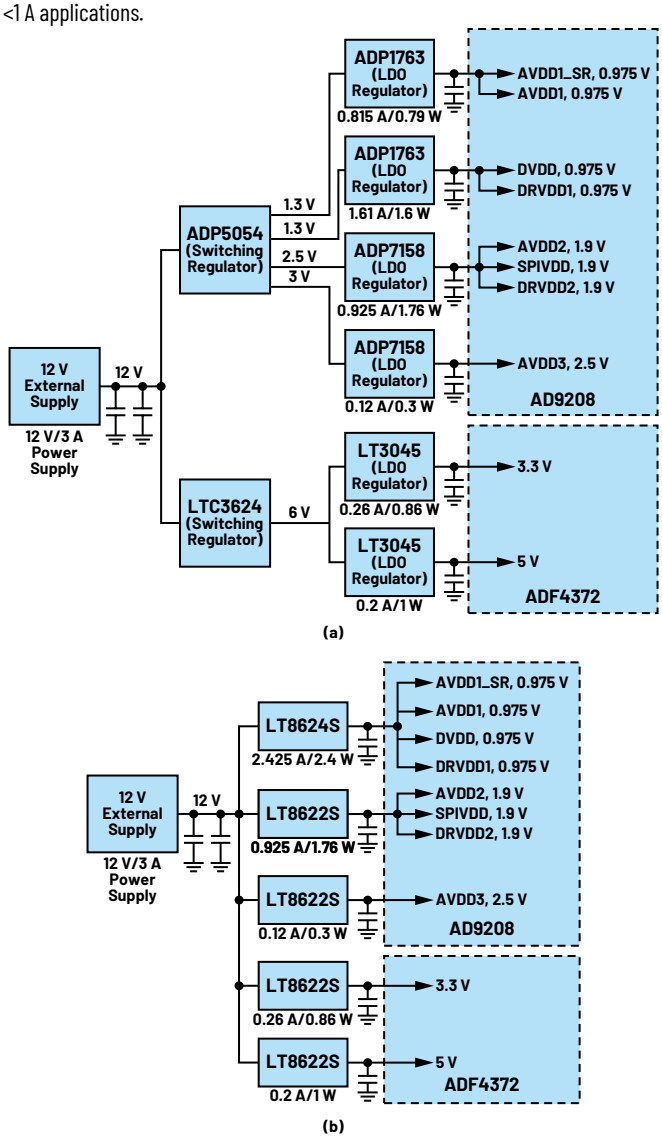


*Figure 11. A comparison of the original and new power tree of ADC system (AD9208 + ADF4372): (a) original power tree (2-stage Buck + LDO regulator solution); (b) new power tree (single-stage solution based on Silent Switcher 3 technology).*

## Conclusion

The ultralow noise switching regulator can achieve ultralow output noise over a wide frequency range and still possess high efficiency and output current capability. With breakthrough noise performance, ADI's Silent Switcher 3 technology even features lower LF noise than most LDO regulators. As a result, a single-stage power solution based on Silent Switcher 3 technology is attractive and promising for noise-sensitive RF applications. This article comprehensively showcases the benefits of the Silent Switcher 3 family in noise-sensitive RF applications. Two case studies successfully demonstrate that the single-stage power solution based on Silent Switcher 3 technology can replace the traditional 2-stage solution with an ultralow noise LDO regulator and still support uncompromised system performance.

When powering a high performance PLL clock, the Silent Switcher 3 technology can achieve almost the same phase noise as the 2-stage solution with an ultralow noise LDO regulator. The Silent Switcher 3 technology even outperforms the 2-stage solution based on a typical LDO regulator without ultralow noise design regarding PLL performance. In the other case study of an ADC system, the Silent Switcher 3 technology with proper filter design can achieve superior ADC performance, with key ADC parameters almost the same as buck + ultralow noise LDO regulator solution. A simplified power tree structure based on the Silent Switcher 3 technology can hence be developed for the ADC system without any LDO regulators. Compared to the original buck + LDO regulator solution, the Silent Switcher 3 solution without any LDO regulators not only has fewer components and a smaller solution size, but also reduces power loss by 71%.

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