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# A Test Method for Synchronizing Multiple GSPS Converters

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## Abstract

Synchronization of multiple converters is useful for such applications such as radar, electronic warfare (EW), ultrasound, and other multichannel applications that use digital beamforming technology in order to manipulate a large field of data. It is important to note that when using GSPS analog-to-digital converters (ADCs), the same requirement is needed to facilitate the synchronization of multiple converters within the same system. However, the speed and interface make this more difficult to achieve.

In this article, two methods will be described: the use of deterministic latency and the use of control bits within the JESD204B interface data word. Both methods are features of JESD204B Subclass 1. The newly released AD9625 (12-bit, 2.5 GSPS ADC) was used as a test vehicle to provide baseline results on the design rules required to follow for the synchronization of multiple converters.

### **Overview and Methods**

Synchronizing multiple ADCs is an essential requirement in the aerospace and defense industry. The AD9625 is a 12-bit, 2.5 GSPS ADC that was designed to facilitate synchronizing multiple converters as one of its standard features. Synchronization is defined as the ability to match each converter to an accuracy equal to or less than a single clock cycle dependent only upon the aperture jitter of the ADC, clock jitter, and clock distribution accuracy. The AD9625 utilizes high speed serial data lanes conforming to the standard JESD204B interface technology. JESD204Bbased converters are still relatively new in the market and many users are adopting this technology for the first time with concerns over the ability to synchronize multiple devices. This article should suppress some or all of these concerns as a relatively simple bench test setup was used to successfully synchronize two converters and show scalability.

There are two unique options for synchronizing multiple AD9625s together. One approach would be to use deterministic latency, where the latency would then have to be adjusted for each individual data path in order to correct the timing mismatch. This method will not be described in this article for this reason. This article focuses on a second option using what is commonly referred to as the time stamping method. Keep in mind that both methods are features of JESD204B Subclass 1, which is used as part of the AD9625 design. In this article, the time stamping method will be the focus, primarily because there is no need to measure the time delay from every converter to every FPGA. For larger systems this is especially important because of the potential employment of hundreds of converters that could be used in applications like ground-based radar systems.

Before we move on, one key application that will benefit from synchronization is radar. In this case, absolute time measurements are not needed. The designer only needs to concern themselves with the relative time from one receiving element to the next. Finally, the data processing is less intensive when using time stamping because the FPGA or processor is only looking for a time marker in each data set. Using this time marker allows the designer to align the data and run algorithms from a defined and synchronous point for each converter path. There are no worries about the distance in trace length from each converter to its respective FPGA across an indefinite number of converter/FPGA pairs. This routing is likely to cross over multiple boards, making it all the more helpful in the application design. This article gives guidance on basic design rules to follow when synchronizing high speed GSPS converters, the test steps needed to be taken, and the end results to expect.

## A Note About JESD204B

The AD9625 is a 12-bit, 2.5 GSPS high speed ADC with serial outputs that follow the JESD204B standard. Within the JESD204B standard there are multiple subclasses that are optimized for varying purposes. Please refer to the full list of the subclasses for more detail on JESD204B.

The AD9625 uses Subclass 1, which is critical to how this method of synchronization is performed. Subclass 1 uses a SYSREF signal for aligning the serial output data. The SYSREF signal gets clocked into the output data of the converter. This arrangement allows for the SYSREF to be synchronous to the conversion clock and ensures that each distributed SYSREF signal arrives at each converter at the same time. This generates a marker or time stamp to be placed in the JESD204B serial output data showing the exact point where the synchronized data analysis should start.

The AD9625 provides two options for using this marker. The designer can use a separate control bit that is part of the entire 16-bit JESD word or replace the LSB of the converter with the SYSREF time stamp. It should be noted that the test described in this article used the LSB option. It is also important to note that implementation of these control bits and the manner in which these are used to synchronize multiple converters is not part of the JESD specification. The designation of each control bit in a JESD word is left to the discretion of each individual converter design and may vary from converter to converter.



## **The Test Setup**

The setup in Figure 1 shows how to synchronize two converters. In theory, there is no limit to the number of converters that can be synchronized. Starting with a properly designed AD9625 board, as shown in Figure 2 and Figure 3, the test setup requires the following equipment:

- Two standard desktop/laptop computers running a Windows<sup>®</sup> operating system
- Two Xilinx<sup>®</sup> VC707 development kits
- Two AD9625 FMC boards, AD-FMCADC2-EBZ
- Tektronix HFS 9009 pulse generator and stimulus system
- Two Rohde & Schwarz<sup>®</sup> SMA100A signal generators with B22, low phase noise option
- Two 24 GHz matched RF cables for the clock and SYSREF connections



Figure 1. A block diagram of the test setup and its major interconnects.



Figure 2. AD9625 FMC board with synchronization connections (AD-FMCADC2-EBZ).



Figure 3. AD-FMCADC2-EBZ connected to FMC1, HPC slot on the VC707 Xilinx development.

The signal generator (SMA100A) provides the 2.5 GHz sampling clock for each converter. A single output was then split into two clocks by using a 5350–244 Picosecond Pulse Labs power divider. From the two divided outputs, a pair of phase and length matched cables are then connected to each AD9625 board. This ensures that the clock will be synchronous when arriving at each converter.

The task of the pulse generator (HFS 9009) is to generate the SYSREF signals. The pulse generator was specifically chosen for this task because it provides multiple differential outputs with reasonably low jitter and the ability to skew one differential output relative to another differential output, allowing for the ability to move the placement of the SYSREF signal relative to the sampling clock as needed to ensure setup and hold times were not violated.

Next, the analog input must also be split in the same way as the sample clock. Using another power divider with a pair of phased matched cables ensures that both analog input signals arrive at each converter's input at the same time.

The AD9625 (AD-FMCADC2-EBZ) board connects to the VC707 evaluation platform via an HPC FMC connector. The Xilinx ChipScope and SDK software tools were used to interface with the VC707 and implement the time stamping procedure and capture the data.

## **The Test Procedure**

To manually trigger SYSREF, the pulse generator is activated to align the SYSREF signals for each converter. Upon detection of a SYSREF marker, each FPGA will perform a data capture as shown in Figure 4.



Figure 4. Xilinx ChipScope screen capture displaying a triggered data capture with SYSREF.

Each red line represents an LSB SYSREF marker while the blue waveform shows the actual captured data. Once the data is successfully captured as shown above the data is then exported for processing in MATLAB.®

## **Synchronized Results**

After analyzing the exported raw data in MATLAB, the time domain reconstructed data from each ADC can be plotted on top of each other (Figure 5).



Figure 5. MATLAB reconstruction of raw data in the time domain.

Figure 6 shows the rising edge of Figure 5 in a magnified view. The horizontal axis represents samples. The delta between the blue and red lines representing the two separate and synchronized ADC/FPGA data sets visually looks to be less than one sample deviation.



Figure 6. Magnified view of Figure 5, rising edge.

Table 1 reviews a subset of the sample phase deltas as it relates to the test configuration setup in Figure 1 with a 710 MHz analog input.

#### **Table 1: Subset of Sample Phase Deltas**

Sample Set	Phase 1	Phase 2	Phase Delta	Samples Delta
1	-2.5598	-2.2897	-0.2701	-0.1513
2	2.5860	2.8579	-0.2719	-0.1523
3	0.0940	0.3648	-0.2708	-0.1517

The test results in Table 1 show an analog input running at 710 MHz and three separate captures yielding similarly accurate results. Again, each result is synchronized to within  $\pm 0.5$  samples. Note that it is very important to phase-lock the two sources in the test setup to provide synchronous sample clock and SYSREF inputs. If those two edges were to move freely in time relative to each other, not phase-locked, then statistically the expectation would be to eventually violate the setup and hold times every so often.

With new and upcoming JESD204 clock distribution ICs on the market, like the HMC7044, AD9525, and AD9528, this will automatically take care of phase-locking of each clock and SYSREF input.

### Conclusion

Using this test setup method proves that two AD9625, 12-bit, 2.5 GSPS ADCs can be synchronized with a JESD204B high speed serial digital interface to better than one sample accuracy by using the SYSREF and time stamping method. While this method used plenty of benchtop testing equipment, which is cumbersome, it will soon be possible to implement this same synchronization setup using newly released Analog Devices clocking devices, thus allowing for a simpler solution.

In addition to proving synchronization between two converters, this article has also outlined that this concept can be scaled to incorporate multiple converters, where applications such as radar, electronic warfare, and military communication applications would benefit greatly from this new capability at GSPS speeds.

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