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A Measurement Summary of Distributed Direct Sampling S-Band Receivers for Phased Arrays

Peter Delos, Technical Lead
Mike Jones, Principal Electrical Design Engineer
Hal Owens, Aerospace and Defense System Intern

Abstract

This article details performance measurements vs. predictions of a 16-channel S-band direct sampling receiver design. The design is based on recently released direct sampling analog-to-digital converters (ADCs) clocked at 4 GSPS and sampling in the second Nyquist zone of the converter. The design configuration is first described with pointers to online references that provide further description. Next, the receiver is shown for both the RF components and the configuration of the embedded digital signal processing (DSP) that is now integrated into modern data converters. Calculations for single-channel performance predictions are presented and compared against measurements. With the single-channel performance understood, a set of measurements combining data from 16 channels evaluates the dynamic range improvements for noise density, spurious signals, and intermodulation products. The article concludes with a set of observations for the multichannel performance trends that can be used for extrapolation to models of large phased arrays implemented with many distributed receivers.

Introduction

Increased ADC sample rates currently enable direct sampling RF systems through S-band and beyond. Advancements in ADC technology have enabled the proliferation of digital beamforming phased arrays. With these advancements, industry questions remain both on the single-channel performance capability of a direct sampling receiver and also the dynamic range improvements possible when many direct sampling receivers are distributed in large phased arrays.

Despite the significant industry effort by both semiconductor companies developing the latest data converters and large company system integrators improving phased array architectures, there remain limited published data quantifying the achievable performance improvements from high channel count direct sampling receiver systems, which coherently combine data from multiple distributed receivers.

Our intention is to help provide quantifiable measurements that system engineers can use to inform their own large phased array models. Our data collection is merely one set of basic measurements to consider when creating a much more complicated phased array system model.

The Receiver Design Evaluated

A 16-channel direct S-band radio frequency (RF) sampling platform was developed to evaluate the latest high speed data converters in a multichannel environment.[1] The platform (see Figure 1) contains four AD9081 mixed-signal front-end (MxFE®) integrated circuits (ICs). Each AD9081 contains four RF digital-to-analog converters (DACs) and four RF ADCs, providing a total of 16 RF transmit and 16 RF receive channels. The Quad-MxFE Platform product page provides a detailed description of the platform along with the software used.

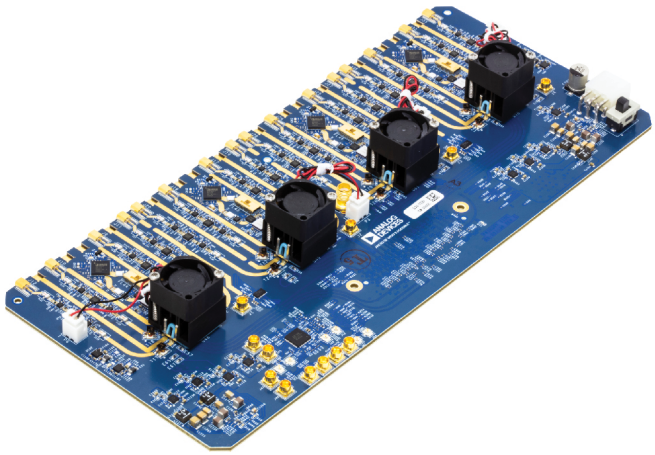


Figure 1. The Quad-MxFE 16-channel direct sampling platform.

The receiver design details are shown in Figure 2. The RF components at the receiver front end are shown along with the ADC and the configuration of the embedded DSP inside the AD9081.

As the sample rates of modern ADCs increase to enable direct sampling receiver architectures, much of the consideration in the design configuration shifts from the RF domain to the embedded DSP. Note the RF chain is quite simple: there are a couple of amplifiers for gain, a gain control function using a digitally controlled attenuator, and filters for antialiasing purposes. The embedded DSP configuration, however, has many more programmable attributes compared to receiver designs utilizing previous generation data converters. This trend of increased embedded processing will continue with future data converters. Therefore, it becomes necessary for the receiver designer to understand the implications of options selected inside the embedded processing from two standpoints. The first is to be aware of the ADC data preprocessing relative to system expectations. Secondly—and possibly more importantly—is to optimize use of the embedded DSP inside the data converters to offload processing previously accomplished in field programmable gate array (FPGA) fabric and thus optimize system processing power efficiency.

Based on this trend, it becomes necessary to describe the DSP configuration when comparing any measurements vs. calculated predictions. The dataset presented in this article configures the AD9081 ADCs to sample at 4 GSPS. The ADCs are followed by programmable finite-impulse response (pFIR) filters used to equalize amplitude and phase across the band. This is followed by the coarse digital downconverters (DDCs), inside which the numerically controlled oscillators (NCOs) are configured in the band center of interest and a decimate-by-4 block is utilized. The fine DDCs are configured to bypass the NCOs, and an additional decimate-by-4 block is used along with 6 dB of digital gain. The result of this configuration is a total decimation of 16 for a data rate of 250 MSPS, 0 dB digital gain, and a single nonzero NCO frequency setting in the coarse NCOs to select the band center.

The component configuration is enabled through an application programming interface (API) available from the AD9081 product page. A summary of the pertinent primary receiver API functions used for this article is shown in Table 1.

Table 1. Summary of Primary Receiver API Functions Used

API Function Call	Bitfield	Register	Value
adi_ad9081_adc_ddc_coarse_nco_mode_set(..., ..., AD9081_ADC_NCO_VIF)	COARSE_MXR_IF	0x282<7..6>	0x00
adi_ad9081_adc_ddc_fine_nco_mode_set(..., ..., AD9081_ADC_NCO_ZIF)	FINE_MXR_IF	0x283<7..6>	0x01
adi_ad9081_adc_ddc_coarse_gain_set(..., ..., 0)	COARSE_GAIN	0x282<5>	0x0
adi_ad9081_adc_ddc_fine_gain_set(..., ..., 1)	FINE_GAIN	0x283<5>	0x1

Single-Channel Performance Measurements Compared to Calculated Predictions

A spreadsheet calculation of the receiver performance is shown in Figure 3. This analysis is kept simple to include only the primary receiver terms of gain, noise, and third-order intercept. Noise is shown for both noise figure and noise

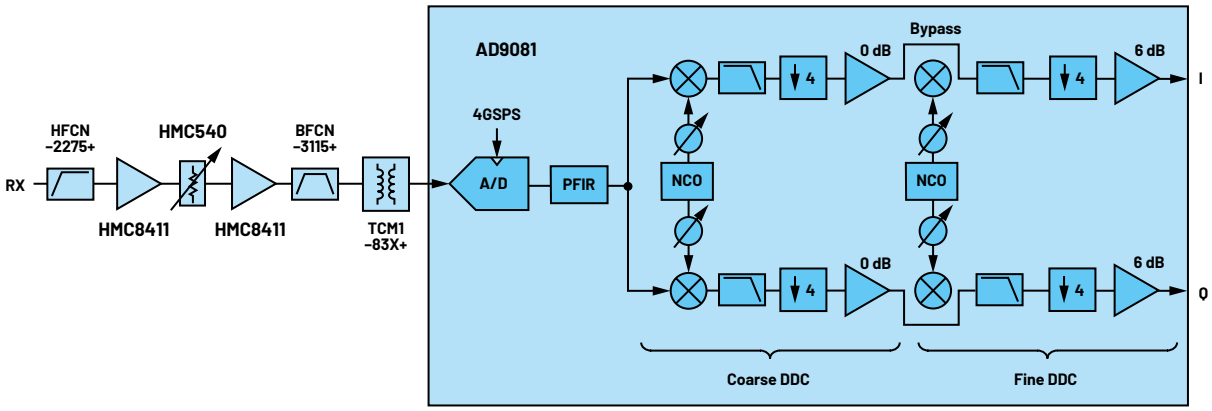


Figure 2. The receiver block diagram. The configuration of the embedded DSP inside the AD9081 is shown along with the front-end RF components.

power. First, a cascaded analysis is shown for the RF components. This is added to the ADC performance next. Details of cascaded calculations containing both RF components and ADCs are included in "A Review of Wideband Receiver Architecture Options."[2] Finally, the performance is reflected back to the receiver RF connector input and summarized at the bottom of Figure 3.

	Component Specs			Cumulative Parameters				
	Gain/Loss	Noise Figure	OIP3	Gain/Loss	Cum Noise Out	Cum_NF	Cum IIP3	Output at AD Full Scale
	(dB)	dB	dBm	(dB)	(dBm/Hz)	(dB)	dBm	(dBm)
Components								-21.0
Front End Loss	-1.0	1.0	50.0	-1.0	-174.0	1.0	51.0	-22.0
HPF	-1.0	1.0	50.0	-2.0	-174.0	2.0	48.5	-23.0
Amp	15.0	1.7	34.0	13.0	-157.3	3.7	21.0	-8.0
DSA	-1.0	1.0	50.0	12.0	-158.3	3.7	20.9	-9.0
Amp	15.0	1.7	34.0	27.0	-143.2	3.8	6.8	6.0
BPF	-1.5	1.5	50.0	25.5	-144.7	3.8	6.8	4.5
Balun	-0.5	0.5	50.0	25.0	-145.2	3.8	6.7	4.0

RF Section Total	Cum Gain	Cum Noise Out	Cum_NF	Cum IIP3
	(dB)	(dBm/Hz)	(dB)	(dBm)
	25.0	-145.2	3.8	6.7

A/D Specs	Full Scale	SNR	IIP3	NF
	(dBm)	(dBFs/Hz)	(dBm)	(dB)
	4	147	36	31.0

Receiver Total	RX Full Scale Input	NSD	Cum NF	Cum IIP3
	(dBm)	(dBFs)	(dB)	(dBm)
	-21.0	**-145.0**	**8.0**	**5.3**

Figure 3. Receiver performance calculations: The RF cascade alone is shown first. The RF performance is then added to the ADC performance for the full receiver performance predictions. The performance is then referred back to the receiver connector input representing an effective ADC directly at the RF input.

Measurements of the full-scale input power and the input third-order intercept point (IIP3) are shown in Figure 4. Starting on the left with the full-scale input power, the predictions in Figure 3 estimated –21 dBm, whereas the measurements of Figure 4 are nominally –20 dBm ±1 dB in the band center. The increase at the band edges is due to the antialiasing filter, and in fact the filter shape can be seen in this data. The gain matching within a dB or two is deemed reasonable, as there is likely an additional dB or so loss not accounted for in the spreadsheet. In comparing the IIP3 data on the right of Figure 4 with the predictions in Figure 3, we see that the IIP3 is slightly better than predicted by about 1 dB, with the exception of the dip in Channel 2 at 2.8 GHz. The IIP3 data are also deemed reasonably close to the cascaded predictions.

Next, a description of the fast Fourier transform (FFT) analysis is warranted. All data provided in our descriptions are based on FFTs and processing to produce measurements from the FFT data. Figure 5 shows example FFTs. The top plot is for a single channel, whereas the bottom plot is for combined and calibrated channels.

Using the single-channel FFT in Figure 5, we can compare noise density with the prediction in Figure 3. The cascade calculation in Figure 3 estimated a noise density of –145 dBFS/Hz when the RF section is cascaded with the ADC. The single-channel measurement of Figure 5 measured –144.3 dBFS/Hz, so the cascaded calculations appear validated to be closely aligned to measurements again.

For the combined FFTs in the bottom of Figure 5, a calibration is performed as described in "Integrated Hardened DSP on DAC/ADC ICs Improves Wideband Multichannel Systems" and "Power-Up Phase Determinism Using Multichip Synchronization Features in Integrated Wideband DACs and ADCs"[3,4] and the data are summed. Then the full scale is adjusted to accommodate the bit growth from

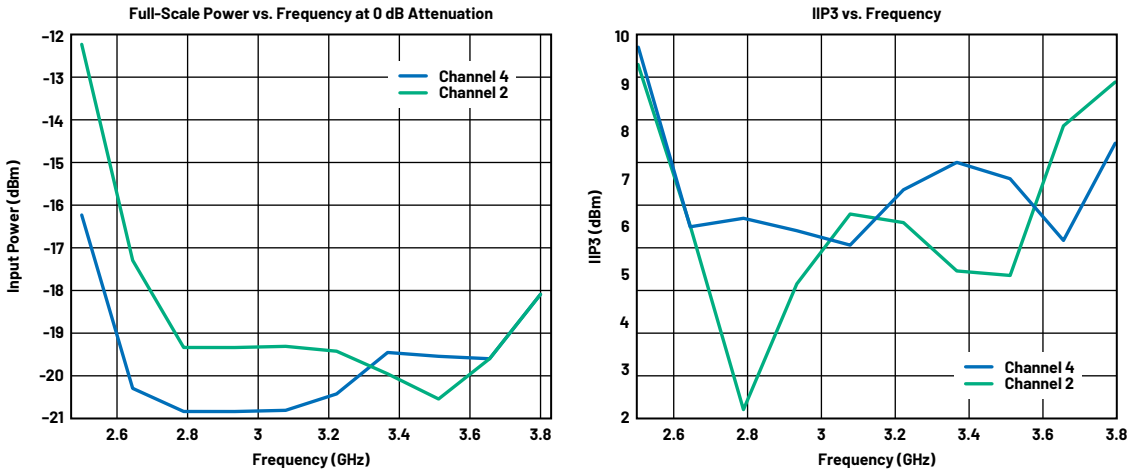
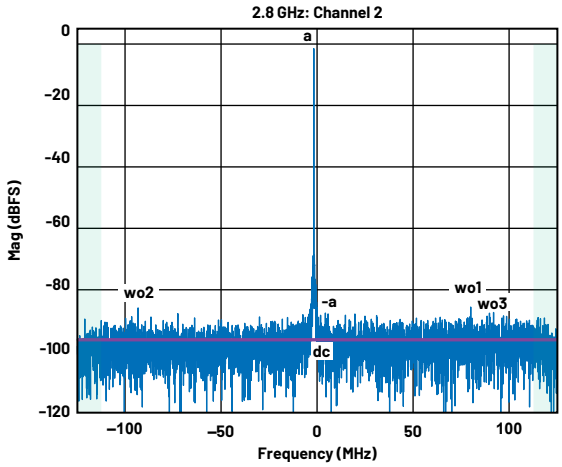


Figure 4. Single-channel measurements for full-scale power and input IP3. Measurements are calibrated to the receiver RF connector input.

Single-Channel Example

	1	2	3
1	aMag	-1.482	dBFS
2	aFreq	-1.953	MHz
3	NSD	-144.383	dBFS/Hz
4	SFDR	84.143	dB
5	wo2Freq	-93.445	MHz
6	wo2Mag	-85.912	dBFS
7	wo3Freq	91.675	MHz
8	wo3Mag	-87.386	dBFS



Combined Output Example

	1	2	3
1	aMag	-1.832	dBFS
2	aFreq	-1.953	MHz
3	NSD	-154.424	dBFS/Hz
4	SFDR	90.114	dB
5	wo1Freq	-64.453	MHz
6	wo1Mag	-91.946	dBFS
7	wo2Freq	60.547	MHz
8	wo2Mag	-92.309	dBFS

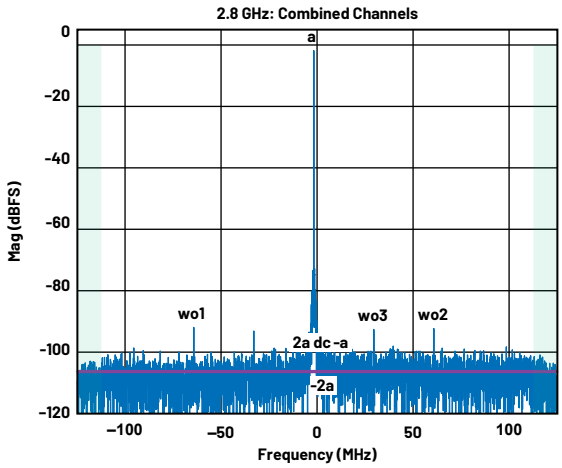


Figure 5. Example FFT measurements.

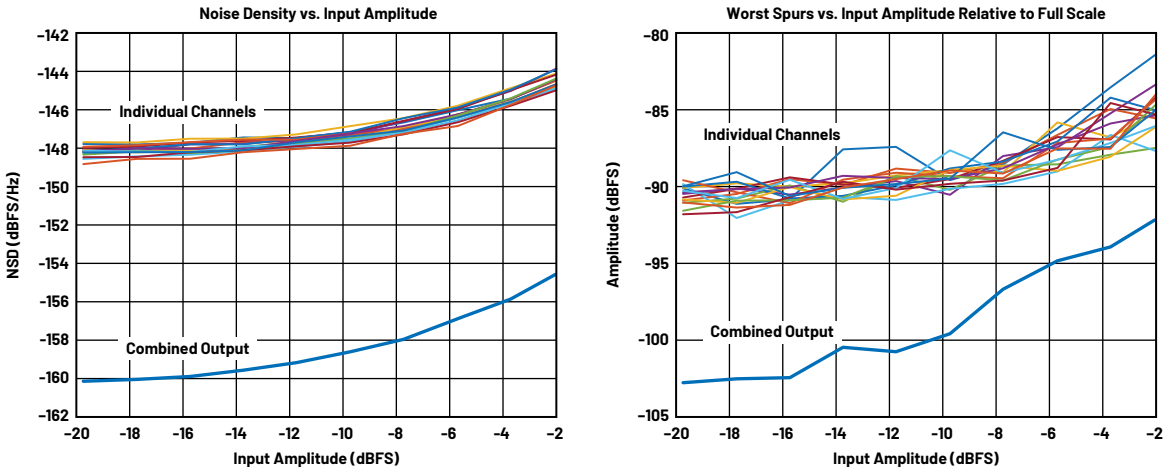


Figure 6. Both noise density and spurious improvements are observed when combining channels. These datasets were taken at 2.8 GHz.

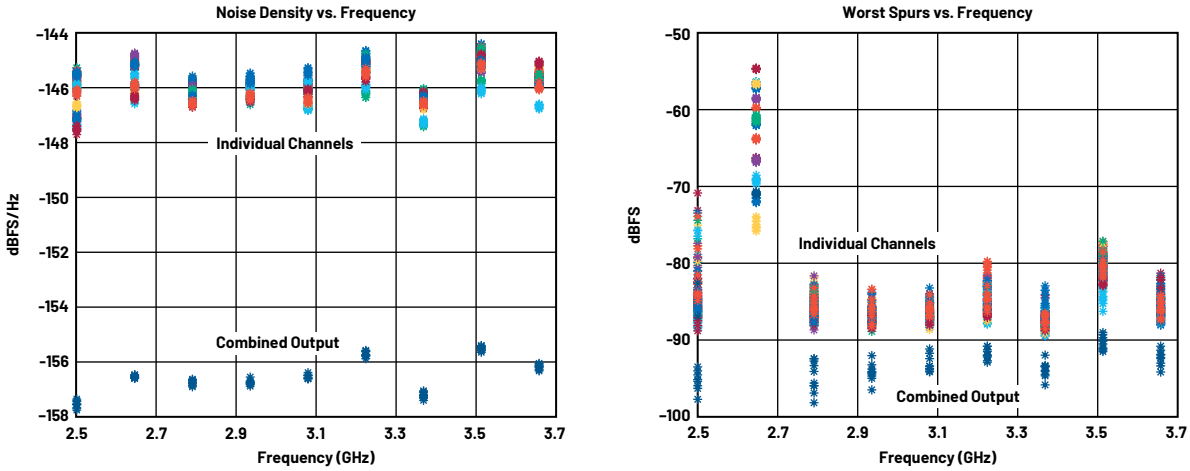


Figure 7. Single-channel and combined-channel noise density and spurious vs. frequency: Ten captures were taken at each frequency. Every dot on the plot represents a single FFT.

the combined data, and finally the same FFTs are performed. With this approach, the full-scale combined level approaches the average channel level and the dynamic range improves, as will be seen next due to the combining gain.

Single-Channel vs. Combined Receiver Measurements

Noise Density and Spurious Signals

We wanted to investigate both noise and spurious improvements when combining channels. Also of interest was to observe the combined-channel impact vs. input power level and frequency. The results are shown in Figure 6 and Figure 7.

Starting with the left side of Figure 6, the effect of noise density vs. input power can be observed. At low power levels, a 10log(N) improvement of 12 dB is achieved for the N = 16 channels in the system. As power is increased, note the combined output noise density increases at a slightly faster rate than the individual channels. This is an indicator of correlated noise terms across channels. In the case of these datasets, the degradation is only approximately 1 dB, so there is still significant improvement when combining channels. The correlated source is believed to be either the phase-locked loops (PLLs) that are common to four channels in a single AD9081 or possibly the RF input source used. No further investigation has been pursued since a 10 dB improvement measured is still quite significant.

The right side of Figure 6 details the spurious performance of the system. There is also a significant improvement in the spurious performance when combining channels, indicating that the spurs are uncorrelated across channels. The spur improvement is quite a positive result. During these data captures, significant effort has been spent evaluating specific spurs at particular frequency offsets. An unexpected observation was that the spurs appeared quite random. The worst spurs in single channels are not the same across channels and do not show up as the worst spurs in the combined data, except for a specific second harmonic case described in Figure 7. There are two explanations for the random nature of the spurs. First, the starting point is quite good, as shown in the FFTs of Figure 5. A secondary effect is that the test setup had limited data capture sizes for all 16 channels and the FFT length for these data captures was limited to 4096 points when capturing all 16 channels. In spite of the data capture length, spurs of <90 dBc are still able to be observed. Future multichannel test platforms will look to extend the FFT length.

Figure 7 illustrates similar single- and combined-channel performance vs. frequency. For these datasets, 10 captures were taken at each frequency. Every dot on the plot represents a single FFT. The power level for these data was nominally –5 dBFS.

The noise density data on the left of Figure 7 show that the individual channels are fairly consistent with the estimates of Figure 3 for all channels and all frequencies. The combined data show a fairly consistent improvement of ~11 dB across the frequencies of interest, which is consistent with Figure 6 at the pertinent power level.

The spurs on the right of Figure 7 also show a fairly consistent combined-channel improvement. The spurs located at 2.65 GHz are worthy of comment. At this frequency, there is a second harmonic that falls in-band and causes the single-channel spurs to be elevated. This frequency point is included in the data because it is relevant to evaluate the impact of spurs due to folded harmonics when channels are combined. Two interesting observations are made. The first is that the spurs do not appear correlated, and second is that there exists a wide range of spur levels across channels. This is a positive result and appears to indicate that the combined output can still approach a 10log(N) improvement beyond the worst channel spurs. It also indicates that through improved layout design, it's possible the spurs at the channel level could be improved. We did not investigate this further but pointed out the observation here to document the result.

Amplitude and Phase Stability

The data of Figure 7 lend themselves to evaluating amplitude and phase stability since multiple datasets are taken at each frequency. The results are shown in the whisker or MATLAB® box plots of Figure 8.

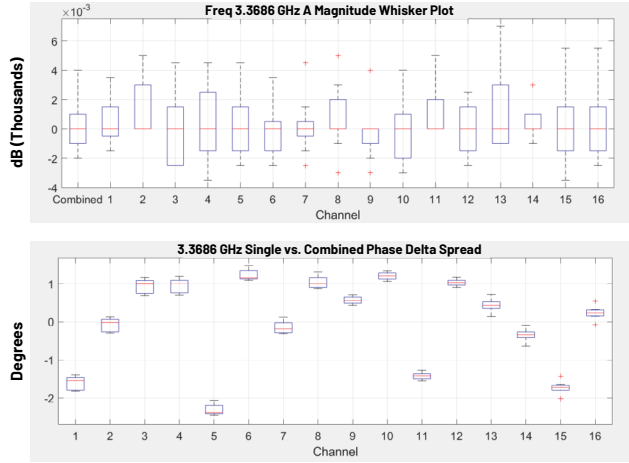


Figure 8. Amplitude and phase stability measurements: whisker plots of the data taken in Figure 7. Datasets are of 10 captures that are nominally over a 5-second period. Amplitude stability in the upper figure shows consistency within a thousandth of a dB. Phase stability in the lower figure shows phase stability within tenths of a degree.

The MATLAB box plot was chosen due to the limited amount of data available. The box-and-whisker plot is a graph designed to provide quick dataset distribution information. There are five main components to a box-and-whisker plot. The red line represents the median of the dataset, whereas the blue box that surrounds the red line represents the first and third quartiles of the dataset. This range is referred to as the interquartile range (IQR). The box contains 50% of the dataset. Above and below the box are the black lines that represent the deemed maximum and minimum of the dataset. Any datapoint that lies outside the range of 1.5 × IQR (the first quartile to third quartile + 1.5 IQR) is considered an outlier and is represented by an individual red cross datapoint. In the amplitude stability plot of Figure 8, amplitudes are compared for all channels and the combined output. For phase stability, the phase of the single channels were compared with the phase at the combined output. This was required because the data captures were asynchronous in this test setup. It is interesting to note the clock distribution can be seen from the results of the phase stability data. Note how the shape of the box in the phase stability data matches in groups of four: channels 1-4, 5-8, 9-12, and 13-16. These channels represent the four channels inside each AD9081, and each AD9081 has a dedicated ADF4371 PLL. The observation that the phase drift matches in this particular set of groups of four indicates the phase stability is dominated by the PLLs. This observation is consistent with our recent phase noise analysis.[5]

Combined 2-Tone Measurements

Our final datasets are 2-tone measurements evaluating the impact of intermodulation products when channels are combined. The results are shown in Figure 9 and Figure 10.

The results show the intermodulation products are correlated and they approach the average of the channel level intermodulation products. This result is consistent with data described in "Digital Arrays using Commercial Transceivers: Noise, Spurious, and Linearity Measurements."[6]

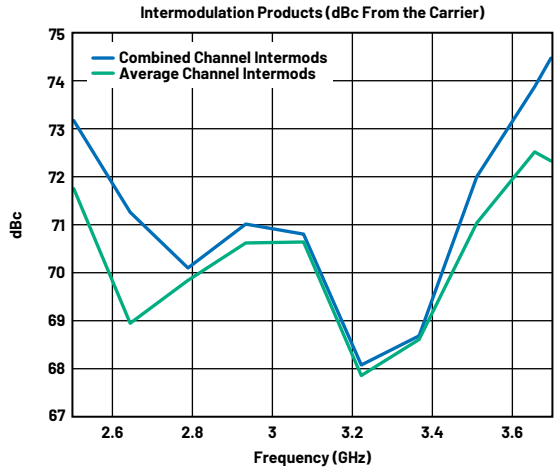


Figure 10. Combined intermodulation products vs. frequency: The combined intermodulation product level approaches the average of the individual channels.

Summary of Observations

Using this comprehensive set of measurements, a few key points can now be summarized.

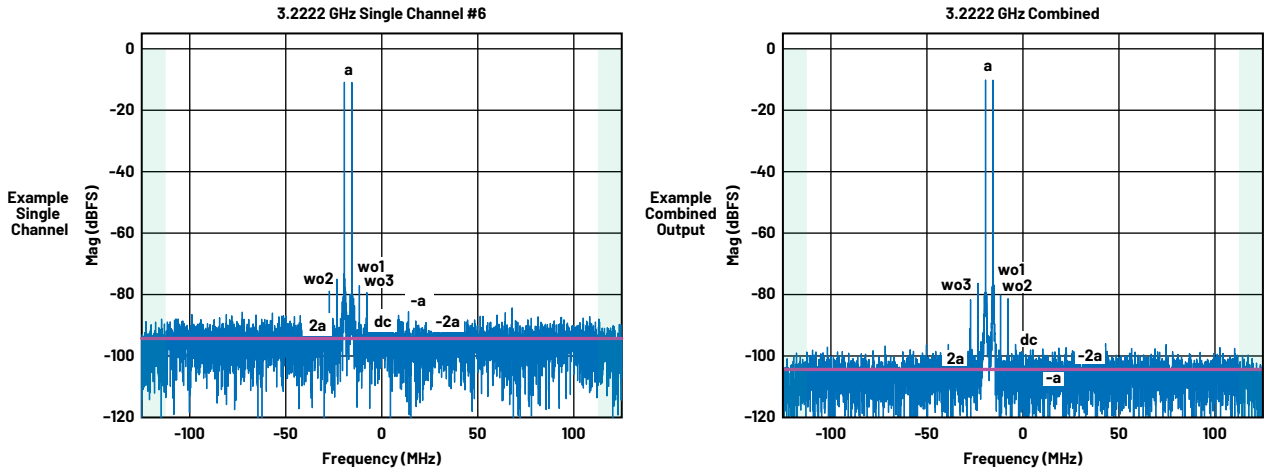


Figure 9. Representative 2-tone FFT measurements. Note the intermodulation product level in dBc relative to the carrier does not improve as channels combine.

For Combined Channels:

- Amplitude: The amplitude of the combined output approaches the average. This is a natural outcome as there is a calibration first to align channels in amplitude and phase.
- Noise density:
  - At low power, a 10log(N) improvement can be realized.
  - As power increases to near full scale, correlated terms can have an impact due to any shared circuitry. Measurements indicate only a 1 dB degradation for 16 channels.
- Spurious signals:
  - Spurs appear more random than initially anticipated. This is a positive result and enables the dynamic range improvements when channels are combined.
  - The worst spurs can generally be improved by 10log(N).
  - Combined 16-channel results show spurious signals at or below 90 dBc, which is quite good and again comparable with a single-channel high performance narrow-band receiver.
  - Larger FFT lengths should be considered for future evaluations to improve the FFT dynamic range for spurious analysis.
- Intermodulation: The intermodulation products are correlated, and no dynamic range improvement is expected. This is a known issue in the phased array community. Since other terms related to dynamic range get improvements as channels combine, it may be that future systems and specifications are linearity-limited by intermodulation products. This fact may drive innovation in nonlinear corrections and research into methods to force intermodulation products to be uncorrelated in large arrays.
- Amplitude and phase stability: Amplitude consistency within a thousandth of a dB and phase consistency within tenths of a degree is observed for data captures over approximately a 5-second duration. We believe the phase stability in this design is limited by the PLL used as the data converter clock source. If an improved phase stability is desired, an alternate clock source could be considered.

A closing observation: The 16-channel noise and spurious measurements appear quite remarkable and comparable to past high performance narrow-band receivers. The data are indicators that it may truly be possible to distribute many direct sampling receivers, enable digital beamforming array level programmability, and still maintain the high performance metrics of legacy narrow-band systems.

Conclusion

Our intention is to summarize and quantify a comprehensive set of receiver measurements in a representative multichannel environment that system engineers can use to extrapolate to models of larger phased arrays. To this aim, a particular direct sampling RF receiver design has been described in detail, measurements have been compared to calculated performance predictions, and single-channel vs. combined-channel noise density, spurious, and intermodulation performance improvements have been described. It is our hope that these datasets become useful for engineers evaluating their own designs when developing large systems based on the latest data converters released from the semiconductor industry.

References

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[2] Peter Delos. "A Review of Wideband Receiver Architecture Options." Analog Devices, Inc., February 2017.

[3] Michael Jones, Travis Collins, and Charles Frick. "Integrated Hardened DSP on DAC/ADC ICs Improves Wideband Multichannel Systems." Analog Devices Inc., May 2021.

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About the Authors

Peter Delos is a technical lead in the Aerospace and Defense Group at Analog Devices in Greensboro, North Carolina. He received his B.S.E.E. from Virginia Tech in 1990 and M.S.E.E. from NJIT in 2004. Peter has over 25 years of industry experience. Most of his career has been spent designing advanced RF/analog systems at the architecture level, PWB level, and IC level. He is currently focused on miniaturizing high performance receiver, waveform generator, and synthesizer designs for phased array applications. He can be reached at peter.delos@analog.com.

Mike Jones is a principal electrical design engineer with Analog Devices working in the Aerospace and Defense Business Unit in Greensboro, North Carolina. He joined ADI in 2016. From 2007 until 2016, he worked at General Electric in Wilmington, North Carolina, as a microwave photonics design engineer working on microwave and optical solutions for the nuclear industry. He received his B.S.E.E. and B.S.C.P.E. from North Carolina State University in 2004 and his M.S.E.E. from North Carolina State University in 2006. He can be reached at michael.jones@analog.com.

Hal Owens is an undergraduate student at Purdue University where he is studying computer engineering. He joined Analog Devices in 2021 as an intern in the Aerospace and Defense System Applications Group. He is primarily interested in software and embedded software development. He helped develop software platforms around phased array platforms such as the Quad-MxFE. After completing his undergraduate degree, he intends to pursue a Ph.D. in some domain of computation.