

Adam Winter
Senior Microwave
Design Engineer
Jerry Cornwell
Manager Product
Development

WIDEBAND HIGH DYNAMIC RANGE LIMITING AMPLIFIER

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Abstract

Wideband, high dynamic range microwave limiting amplifiers are critical components in electronic warfare (EW) systems where stable/compressed output power is required over a wide input power range. These EW systems often require high gain with a flat response and must operate over harsh thermal environments. Maintaining acceptable and reliable performance over multioctave bands requires careful design of the amplifier chain. Improperly cascading and saturating a chain of amplifiers can lead to unreliable and unpredictable performance. This article demonstrates a 2 GHz to 18 GHz design that achieves greater than 40 dB limiting dynamic range with less than 2 dB output power variation and 4 dB noise figure over -40°C to $+85^{\circ}\text{C}$ using ADI devices. By leveraging ADI's unique MMIC advantages and subsystem design capabilities, we are able to offer superior solutions to address customer's need for advanced applications. The test results of the performance achieved are presented below.

1.0 Introduction

Many modern EW systems require low noise receivers capable of withstanding wide input power variations over a multioctave bandwidth. These receivers are necessary to protect sensitive components from RF overdrive or to remove AM modulation from incoming signals. Further, multichannel system designs and proximity to the receiver antenna generate requirements for low power and small package size. Applications include IFM and direction finding front ends, DRFM, and jammer systems. These systems must operate over a wide thermal range and require a flat frequency response with low harmonic content under all operating conditions. ADI's limiting amplifiers are ideal for many of these applications due to industry-leading package size, electrical/RF performance, and ease of integration into higher level assemblies. A microwave limiting amplifier is a high gain, multistage amplifier that limits output power by successively compressing internal gain stages as input power increases. Gain stages compress from the output stage toward the input, with the design optimized to avoid overdriving individual gain stage under all operating conditions. Challenges associated with wideband limiting amplifier design include effective power limiting, thermal compensation, and frequency equalization over a multioctave bandwidth. In addition, system requirements for low noise, low power, and a small package size add to the complexity of the design.

This article reviews design considerations and techniques for a 2 GHz to 18 GHz limiting amplifier with requirements for 45 ± 1.5 dB gain, an operational temperature range -40°C to $+85^{\circ}\text{C}$, fewer than 1.5 W dc, and a 40 dB limiting dynamic range. Limiting dynamic range is defined as the input power range over which RF output power is fixed. ADI offers a wideband 2 GHz to 18 GHz limiting amplifier product, the [HMC7891](#), that meets these requirements. This amplifier includes internal voltage regulation in a hermetically sealed, connectorized package.

2.0 Construction and Amplifier Considerations

Microwave limiting amplifier design begins with down-selection of preferred construction methods and internal gain stage amplifiers. Hybrid chip-and-wire assemblies are often preferred over surface-mount designs for high frequency applications in order to minimize detrimental performance impacts caused by package parasitics, and the reliability of hybrid chip-and-wire assemblies is considered superior because hybrid assemblies are thoroughly inspected and are well suited to handle environmental stress. Further, these assemblies are small, lightweight, and easy to hermetically seal. Hybrid chip-and-wire assemblies consist of die form monolithic microwave integrated circuits (MMICs), thin film technology, and wire bondable passive components.

The primary considerations for selection of internal gain stages include the operational frequency range, gain vs. temperature, gain flatness, saturated harmonic content, and nonlinear performance. A successful limiting amplifier design minimizes gain stages and unique part count to reduce thermal compensation and flatness challenges. Also, success largely depends on device maximum input power ratings and the compression characteristics of the selected gain stages. To complete a design with a 40 dB limiting dynamic range requirement, a minimum of four gain stages is recommended so that ideally each amplifier stage will operate at no more than 10 dB compressed. Four gain stages should also be sufficient to achieve the 45 dB small signal gain requirement over temperature.

Wideband MMIC gain block amplifiers or low noise amplifiers (LNA) are good candidates for limiting amplifier designs due to their high gain and low power performance. A noise figure requirement will typically establish the need to utilize low noise amplifiers over gain block amplifiers. However, LNA gain stages can create design challenges due to their generally lower RF input power rating. An ideal gain stage device has a high maximum RF input power rating and can safely operate at high levels of compression.

Another important consideration is the saturated harmonic content of each gain stage. Harmonic content requirements depend on the limiting amplifier's application. For example, an application meant to generate a

square wave output waveform needs to utilize gain stage amplifiers with low even harmonic output and strong odd harmonic output. To avoid corrupting the output waveform it is useful to utilize the same part in all four gain stage locations. Finally, selected MMIC amplifiers must be unconditionally stable and ideally lack bias sequencing requirements to simplify the design.

The HMC462 is an ideal MMIC to complete a limiting amplifier design. The HMC462 is a self-biased LNA requiring a single 5 V supply with greater than 13 dB gain, excellent 2 GHz to 18 GHz gain flatness, and an average 2.5 dB noise figure. The device has an 18 dBm saturated output power level and can safely operate greater than 14 dB into compression across the frequency band. The maximum input power rating is nearly equivalent to the device's saturated output power making it ideal to operate in a cascaded series of gain stages. The second-order harmonics are low and the MMIC has a strong, flat third-order harmonic. The saturated dc power is less than 400 mW.

3.0 RF Budget Analysis

Following the selection of limiting amplifier gain stages, it is necessary to consider the RF system budget analysis. RF budget analysis examines the broadband frequency response and RF power levels at various test points within the limiting amplifier. Analysis must be completed to correct for worst-case operational temperatures, gain slope, and a wide RF input power range. As discussed in Section 2.0, the basic layout for a limiting amplifier with 40 dB limiting dynamic range is a cascaded series of four gain block amplifiers or LNAs. An ideal design utilizes only one or two unique amplifier part numbers to reduce power variations vs. frequency and to minimize thermal/slope compensation requirements.

Figure 1 illustrates the first pass preliminary limiting amplifier block diagram prior to temperature correction and slope compensation. One recommended technique to complete the wideband limiting amplifier design is to:

1. Manage the limiting power dynamic range and eliminate RF overdrive conditions.
2. Optimize performance over temperature.
3. Complete the design by correcting the power roll-off and flatten the small signal gain.
4. A final minor correction may be necessary to revisit temperature compensation after frequency equalization has been included in the design.

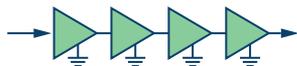


Figure 1. Preliminary block diagram.

3.1 Power Limiting

The primary issue with the preliminary design illustrated in Figure 1 is that RF overdrive will likely occur at the output gain stages as RF input power increases. RF overdrive will occur when the saturated output power of any gain stage exceeds the absolute maximum input of the succeeding amplifier in the lineup. Further, the design is susceptible to VSWR associated ripple and there is a strong potential for an oscillation to occur due to high, undamped gain within the small RF package.

To prevent RF overdrive, diminish VSWR effects, and decrease the risk of an oscillation, add fixed attenuators between each gain stage to reduce power and gain. An RF absorber may also be required on the RF cover to eliminate oscillations. Sufficient attenuation is required to reduce the maximum input power of each gain stage below the MMIC's rated input power level. It is necessary to include enough attenuation to accommodate top level input power margin and to account for thermal and part-to-part variations. Figure 2 illustrates the locations where RF attenuators are necessary within the limiting amplifier chain.

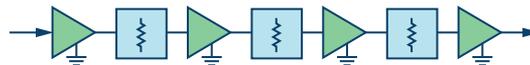


Figure 2. Block diagram, RF overdrive correction.

The ADI broadband limiting amplifier, HMC7891, utilizes four HMC462 gain stages and is designed to operate up to 10 dBm. The absolute maximum input power is 15 dBm. Each gain stage can withstand a maximum RF input of 18 dBm. Per the design step outlined in the preceding paragraph, attenuators were added between gain stages to ensure maximum amplifier input power levels do not exceed 17 dBm. Figure 3 illustrates the maximum power level at the input to each gain stage with fixed attenuators added to the design.

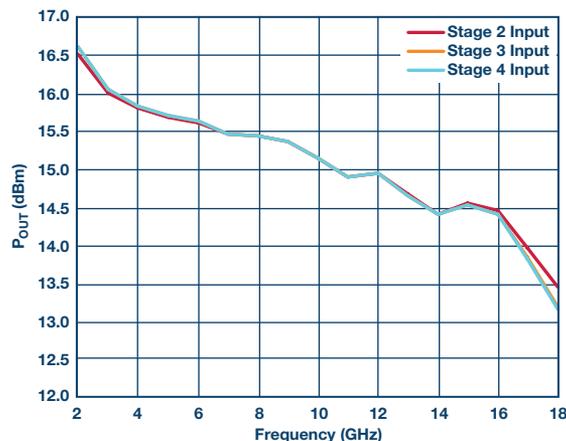


Figure 3. Simulated P_{OUT} vs. frequency, RF overdrive correction.

3.2 Thermal Compensation

The second step is to thermally compensate the design in order to increase the operational temperature range. A common thermal range requirement for limiting amplifier applications is -40°C to $+85^{\circ}\text{C}$. A rule-of-thumb gain variation formula of 0.01 dB/ $^{\circ}\text{C}$ /stage can be used to approximate the gain variability of a four stage amplifier design. Gain increases as temperature decreases and vice versa. Using ambient gain as a baseline, the total gain is expected to decrease 2.4 dB at 85°C and increase 2.6 dB at -40°C .

To thermally compensate the design, commercially available Thermopad[®] temperature variable attenuators can be inserted in place of the fixed attenuators. Figure 4 illustrates test results of a wideband commercially available Thermopad attenuator. Based on Thermopad test data and the approximated gain variation, it is clear that two Thermopad attenuators are necessary to thermally compensate a four stage limiting amplifier design.

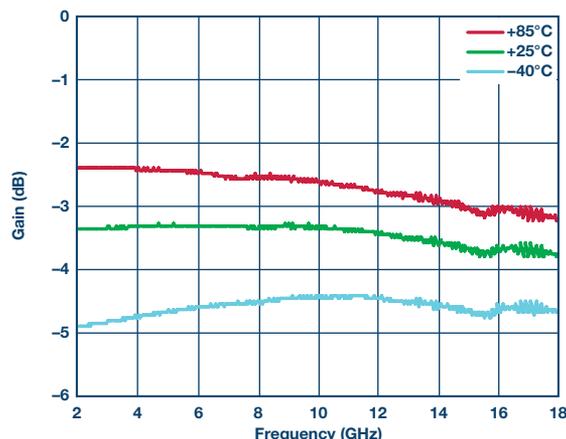


Figure 4. Thermopad loss over temperature.

Deciding where to insert the Thermopads is an important decision. Due to the increased loss of Thermopad attenuators, especially at cold temperatures, it is good practice to avoid adding the components near the output of the RF chain in order to maintain a high limiting output power level. Ideal Thermopad locations exist between the first three amplifier stages as highlighted in Figure 5.

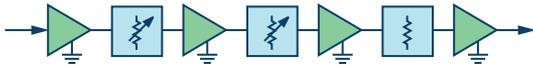


Figure 5. Block diagram, thermal compensation.

Simulation results of ADI's thermally compensated HMC7891 small signal performance is illustrated in Figure 6. Gain variation is reduced to a maximum of 2.5 dB prior to frequency equalization. This is within the ± 1.5 dB gain variation requirement.

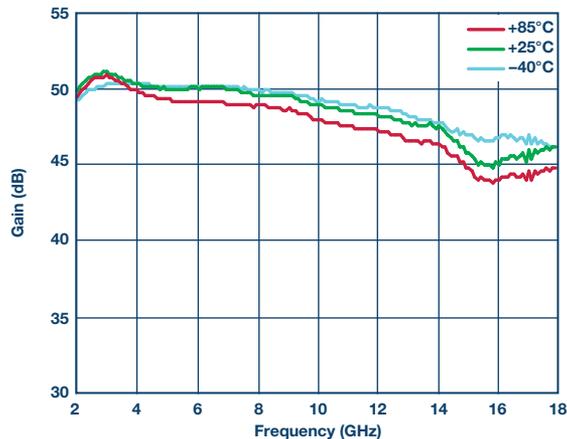


Figure 6. HMC7891 simulated small signal gain over temperature.

3.3 Frequency Equalization

The final design step is to improve gain flatness by incorporating frequency equalization. Frequency equalization compensates for the natural gain roll-off found in most wideband amplifiers by introducing a positive gain slope to the system. Various equalizer designs exist including passive GaAs MMIC die. Passive MMIC equalizers are ideal for limiting amplifier designs due to their small size and lack of dc and control signal requirements. The number of required frequency equalizers depends on the uncompensated gain slope of the limiting amplifier and the response of the selected equalizer. A design recommendation is to slightly overcompensate the frequency response to account for transmission line loss, connector loss, and package parasitics that have a greater impact on gain at higher frequencies than lower frequencies. Test results for a custom ADI GaAs frequency equalizer are found in Figure 7.

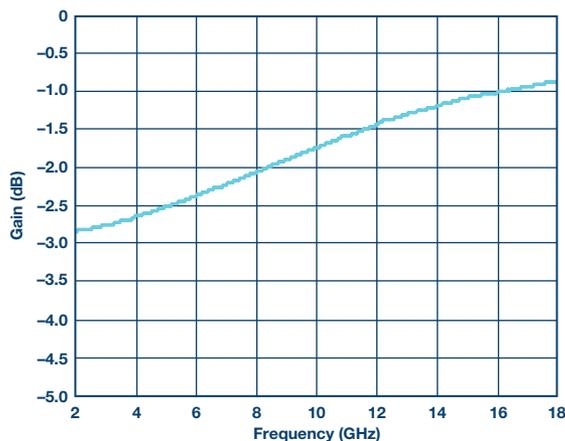


Figure 7. Measured frequency equalizer loss.

ADI's HMC7891 limiting amplifier requires three frequency equalizers to correct the thermally compensated small signal response. Figure 8 illustrates the thermally compensated and frequency equalized simulation results of the HMC7891. Deciding where to insert the equalizers is critical for a successful design. Prior to adding any equalizers it is important to remember that an ideal limiting amplifier evenly distributes maximum amplifier compression across all gain stages in order to avoid oversaturation. In other words, each MMIC should be equally compressed under worst-case conditions.

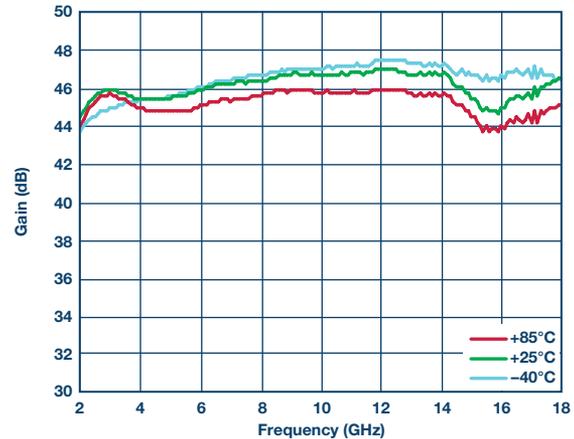


Figure 8. HMC7891 simulated frequency equalized small signal gain over temperature.

At the current stage of the design, shown in Figure 5, equalizers can be added at the device input, in series with Thermopad attenuators, in place of the fixed attenuator or at the device output. Adding equalizers to the limiting amplifier input decreases power at the first gain stage. As a result, Stage 1 compression decreases. A decrease in gain stage compression is equivalent to a decrease in limiting dynamic range. Further, due to the equalizer's attenuation slope the limiting dynamic range disperses over frequency. Dynamic range decreases more at lower frequencies than at higher frequencies. To compensate for the decreased limiting dynamic range the RF input power must increase. However, uniformly increasing input power adds to the risk of overdriving an amplifier gain stage due to the equalizer's slope. It is possible to add an equalizer at the device input, but this is not an ideal location.

Next, adding an equalizer in series with the Thermopad will reduce the compression of the succeeding amplifier. This creates an uneven distribution of amplifier compression among gain stages and decreases overall limiting dynamic range. Equalizers in series with Thermopad attenuators are not recommended.

Third, substituting an equalizer (or equalizers) in place of the fixed attenuator changes only the compression level of the output stage amplifier. To minimize this change and avoid RF overdrive, the equalizer loss should be approximately equal to the fixed attenuation value being removed from the system. Further, as discussed earlier, adding equalizers prior to gain stages creates dispersion in limiting dynamic range vs. frequency. To minimize this effect substitute the minimum number of equalizers possible.

Finally, equalizers can be added to the device output. Output equalization reduces output power, but will not create limiting dynamic range dispersion. Output equalization does create a slightly positive output power slope, but this slope is offset by high frequency package and connector loss. A completed four stage limiting amplifier layout is illustrated in Figure 9.



Figure 9. Block diagram, frequency equalization.

Figure 10 illustrates the output power vs. temperature simulation result for ADI's HMC7891. The final design achieves 40 dB limiting dynamic range and has a simulated worst-case output power variation of 3 dB under all operating conditions.

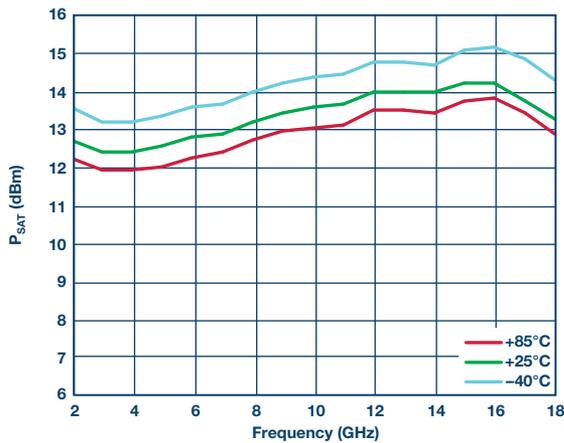


Figure 10. HMC7891 simulated P_{SAT} vs. frequency over temperature.

4.0 ADI Limiting Amplifier Test Results

Test results for the HMC7891 are illustrated in Figure 11 through Figure 18. Results demonstrate the design was able to achieve 47 dB gain with a saturated output power of 13 dBm. The amplifier's input power range is -30 dBm to +10 dBm, for a limiting dynamic range of 40 dB. The unit was tested over an operational temperature range of -40°C to +85°C. A photograph of the HMC7891 is shown in Figure 19 below. Though the HMC7891 was primarily designed as a limiting amplifier the small size and superior RF performance enable utility in various applications, including use as a frequency tripler or as an LO amplifier. The design technique described herein can be used for future limiting amplifier designs with modifications to spec requirement such as frequency, output power, gain, NF, or limiting dynamic range.

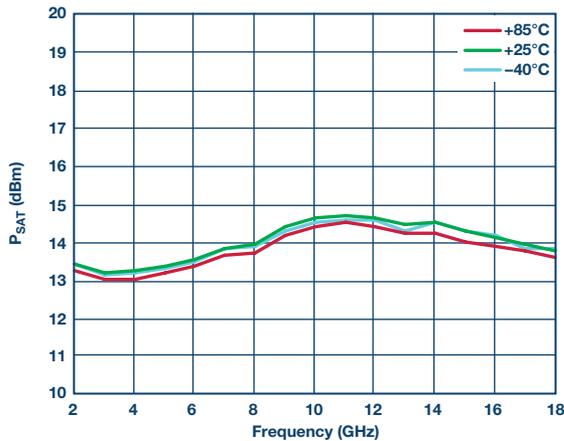


Figure 11. HMC7891 measured P_{SAT} vs. frequency over temperature.

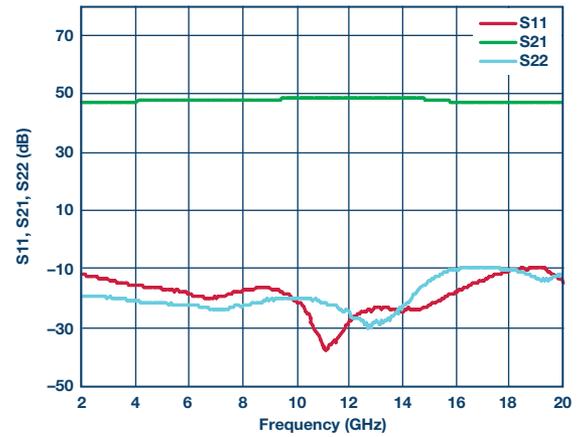


Figure 12. HMC7891 measured gain and return loss.

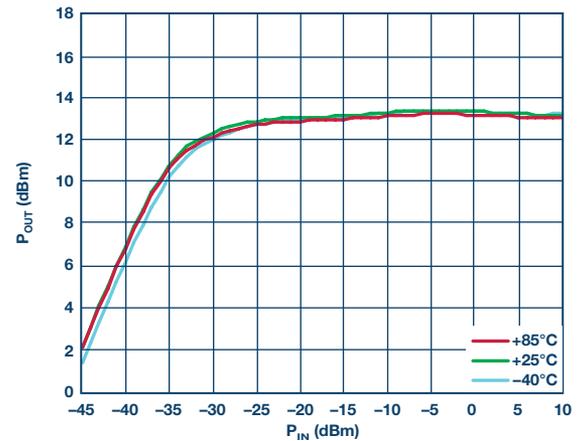


Figure 13. HMC7891 measured P_{OUT} vs. P_{IN} at 2 GHz over temperature.

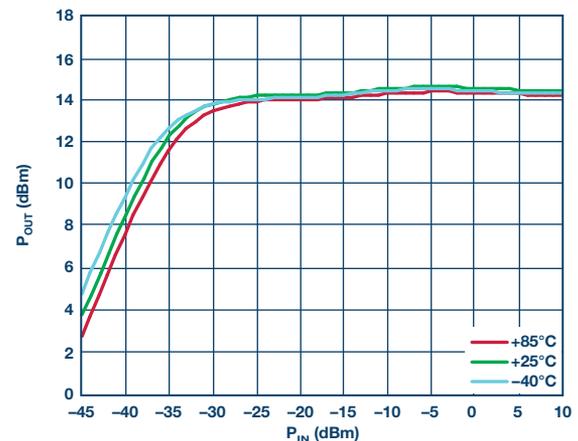


Figure 14. HMC7891 measured P_{OUT} vs. P_{IN} at 10 GHz over temperature.

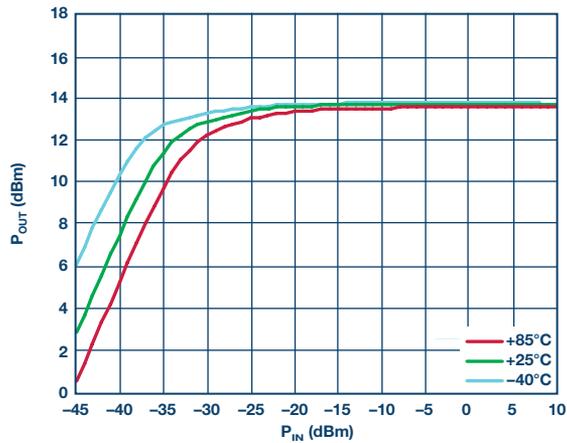


Figure 15. HMC7891 measured P_{OUT} vs. P_{IN} at 18 GHz over temperature.

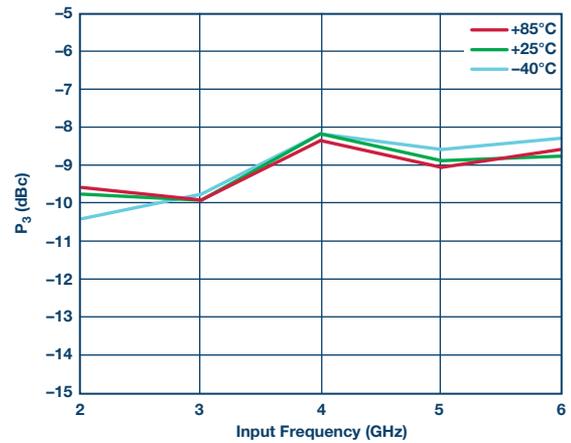


Figure 18. HMC7891 measured third-harmonic vs. frequency at P_{SAT} .

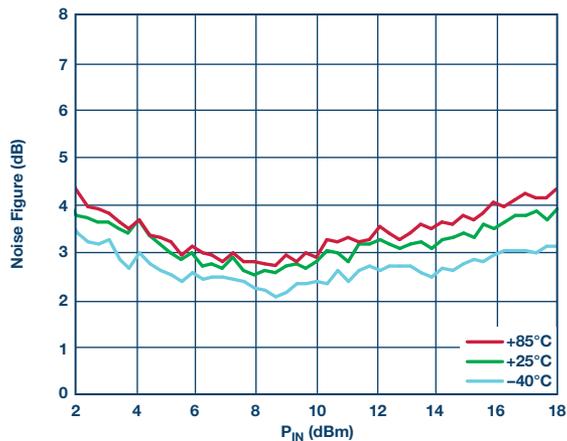


Figure 16. HMC7891 measured NF vs. frequency over temperature.

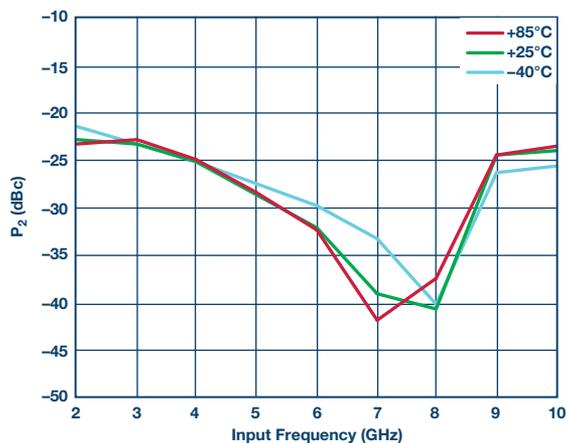


Figure 17. HMC7891 measured second-harmonic vs. frequency at P_{SAT} over temperature.

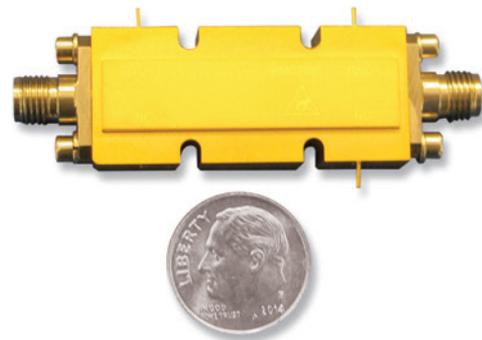


Figure 19. HMC7891 photograph.

About the Authors

Adam Winter received a B.S.E.E. from Johns Hopkins University and an M.Eng.E.E. from the University of Colorado Boulder. He is a senior microwave design engineer at ADI. Prior to joining ADI, Mr. Winter worked for Lockheed Martin Space Systems. He has nearly 10 years of experience on design, development, and production of military/space RF components, modules, and custom assemblies, including high power GaN amplifiers, millimeter wave frequency converters, transmitter/receiver modules, SSPAs, and LNAs.

Gerald Cornwell received his B.S.E.E. from The New Jersey Institute of Technology. He has over 40 years of experience in this industry addressing all aspects from design and development to production. Prior to joining ADI, he had been at Raytheon working on EW systems, at M/A-COM as vice president of engineering of the Microwave Subsystems Group serving the EW, radar, and missile markets, chief technologist of the Aerospace and Defense Division, and at Cobham Sensor Systems as director of technology in the Business Development Group. Mr. Cornwell joined ADI as senior business development manager for Modules and Subsystems.

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**Analog Devices, Inc.
Worldwide Headquarters**

Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643, U.S.A. only)
Fax: 781.461.3113

**Analog Devices, Inc.
Europe Headquarters**

Analog Devices, Inc.
Ott-Aicher-Str. 60-64
80807 München
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

**Analog Devices, Inc.
Japan Headquarters**

Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

**Analog Devices, Inc.
Asia Pacific Headquarters**

Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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