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TECHNICAL ARTICLE

WHY ISOLATE LVDS?

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Galvanic isolation of external interfaces is required in harsh environments for safety, functionality, or improved noise immunity. This includes analog front ends used in data acquisition modules for industrial measurement and control, as well as digital interfaces between processing nodes.

In the past, bandwidths of up to a few Mbs were sufficient for convertor interfaces or industrial backplanes, allowing isolation of protocols such as serial peripheral interface (SPI) or RS-485 using optocouplers. Digital isolators have improved the safety, performance, and reliability of such isolated interfaces, as well as offering integrated isolation and I/O. However, trends such as Industry 4.0 and the Internet of Things (IoT) demand far more ubiquitous measurement and control, with greater speed and precision, resulting in greater demands for increased bandwidth.

The need for galvanic isolation also proliferates as these increased digital interactions with the physical domain demand protection from motor and power systems, human operators, and electrostatic discharge, as well as external factors like surges due to lightning strikes. Precision measurements can also need isolation from noise sources such as more localized and miniature power circuits and high speed digital processing.

Low voltage differential signaling (LVDS) is a ubiquitous high speed interface for higher performance convertors and high bandwidth FPGA or ASIC I/O. The differential signaling offers high immunity to external electromagnetic interference (EMI) due to the mutual coupling between the inverting and noninverting signals, which also correspondingly minimizes any EMI created by the LVDS signaling. Adding isolation to LVDS interfaces provides a transparent solution that can be inserted into existing signal chains for high speed and precision measurement, as well as control applications.

What Options Exist Today?

Standard digital isolators remain a much faster, robust, and more reliable solution than optocouplers for galvanic isolation of converter and processor interfaces. However, typical LVDS data rates to support high speed or precision converters are in the hundreds of Mbs, while the fastest standard digital isolators support up to 150 Mbps.

To support isolating at higher bandwidths, system designers (until now) have turned to custom design intensive solutions, such as deserialization or discrete solutions using transformers or capacitors. These add cost and design time, with deserialization potentially even requiring an extra simple FPGA just for that function. Transformers and capacitors require careful signal conditioning of LVDS signals, resulting in application and data rate specific solutions requiring ac balanced encoding. A further solution is the use of fiber communication links, but this is better suited to multigigabit requirements due to the cost and increased complexity. The spectrum of options for isolating at high speed are shown in Figure 1, with the value proposition (depending on the ease of design and cost) plotted against the maximum speed of the implementation.

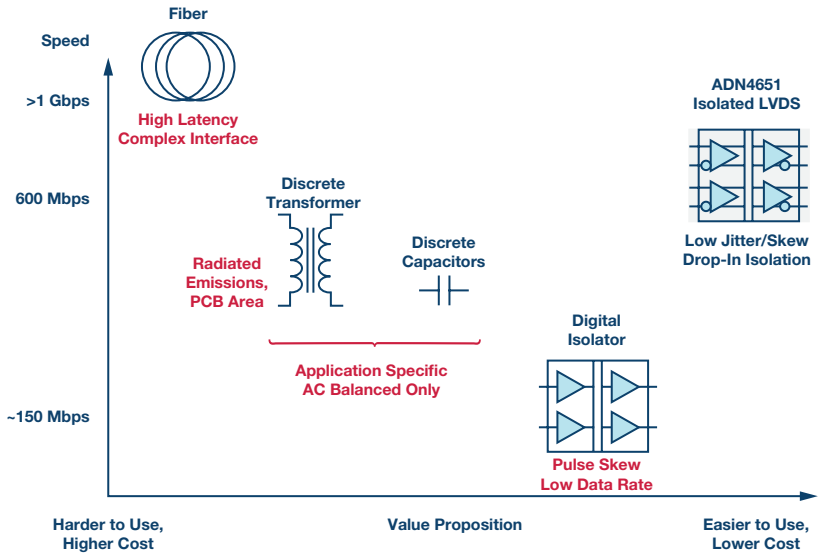

Figure 1. Value proposition of isolator implementations vs. isolator speed.

By contrast, as shown in Figure 2, Analog Devices has introduced a family of drop-in LVDS isolators: ADN4650/ADN4651/ADN4652, using *i*Coupler® technology enhanced for operation up to 600 Mbps. In addition to TIA/EIA-644-A LVDS compliant I/O, the complete isolator signal chain is fully differential, realizing a high immunity and low emissions solution. Two isolated LVDS channels are provided, one transmit and one receive (ADN4651, or vice versa for ADN4652) or two transmit or receive (ADN4650). The internal high speed circuits operate at 2.5 V, which may not be present in industrial systems as a power rail, so internal low dropout regulators (LDOs) are provided (as shown in Figure 3) to allow a single wide-body SOIC solution even when powering from 3.3 V supplies.

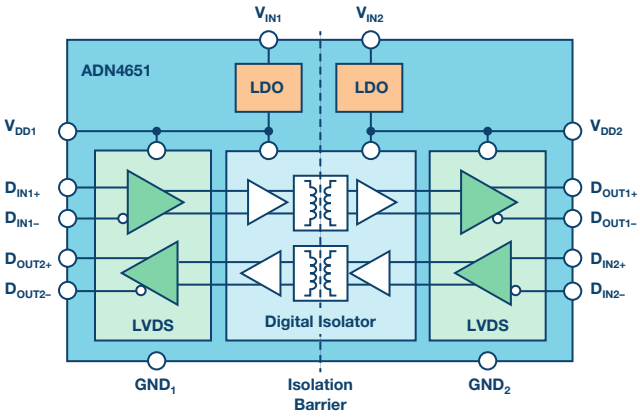

Figure 2. ADN4651 600 Mbps LVDS isolator block diagram.

Are These New LVDS Isolators a Drop-In Solution?

In order to guarantee these LVDS isolators can be inserted into converter to processor interfaces, or intraprocessor links that operate up to 600 Mbps—the ADN465x family has precision timing with ultralow jitter. This is important because at 600 Mbps, the unit interval (UI, such as the bit time) is only 1.6 ns, so any jitter on the edges must still allow enough time for the receiving component to sample the bit. Typical total jitter is 70 ps for the ADN465x, or <5% UI at 600 Mbps, assuming a bit error rate of 1×10^{-12}.

How to Quantify Jitter

The most basic method of viewing jitter is to measure an LVDS signal pair with a differential probe and trigger on both rising and falling edges, with the oscilloscope set to infinite persistence. This means that high-to-low and low-to-high transitions are superimposed, allowing measurement of the crossover point. The width of the crossover corresponds to the peak-to-peak jitter or time interval error (TIE) measured so far (compare the eye diagram and histogram shown in Figure 3). Some jitter is due to random sources (like thermal noise) and this random jitter (RJ) means that the peak-to-peak jitter seen on the oscilloscope is limited by the run time; the tails on the histogram will grow as the run time increases.

By contrast, sources of deterministic jitter (DJ) are bounded, such as jitter due to pulse skew, data rate dependant jitter (DDJ), and intersymbol interference (ISI). Pulse skew arises due to a difference between high-to-low and low-to-high propagation delays. This is visualized by an offset crossover such that at 0 V, the two edges are separated (easily seen by the separation in the histogram in Figure 3). DDJ arises from a difference in propagation delay across operating frequency, while ISI arises due to the influence of previous transition frequencies on the current transition (edge timing will typically be different after a train of 1 sec or 0 sec vs. a 1010 pattern).

In order to fully estimate the total jitter for a given bit error rate (TJ@BER), RJ and DJ can be calculated based on model fitting to a TIE distribution from measurement. One such model is the dual Dirac model, which makes an assumption of a Gaussian random distribution convolved with a dual Dirac delta function (the separation between the two Dirac delta functions corresponding to the deterministic jitter). For TIE distributions with significant deterministic jitter, the distribution will visually approximate this model. One complication is that some deterministic jitter can contribute to the Gaussian component, meaning that dual Dirac can underestimate deterministic jitter and overestimate random jitter. However, the two combined will still allow an accurate estimate of the total jitter for a given bit error rate.

RJ is specified as a one sigma rms value from the modelled Gaussian distribution, meaning to extrapolate longer run lengths (low BERs), one simply chooses the appropriate multiple sigma to move far enough along the tails of the distribution (14 sigma for 1×10^{-12} bit errors). DJ is then added to provide the TJ@BER estimate. For multiple elements in a signal chain, rather than adding multiple TJ values, which will overestimate jitter, RJ values can be geometrically summed and DJ values algebraically summed allowing a more reasonable complete TJ@BER estimate for a complete signal chain.

RJ, DJ, and TJ@BER are all specified separately for ADN4651, with maximums provided for each based on statistical analysis of multiple units to guarantee these jitter values across power supply, temperature, and process.

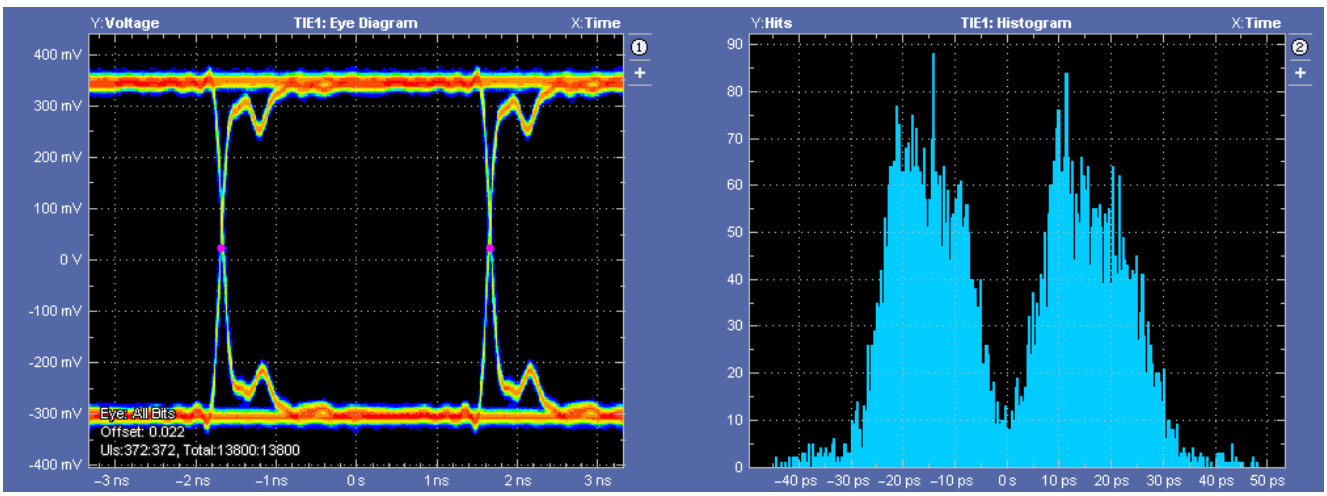

Figure 3. Eye diagram and histogram for ADN4651.

How Do Different LVDS Interfaces Rely on Precise Data Transitions?

A typical receiver may tolerate 10% or 20% UI of jitter, so isolating external LVDS ports with ADN465x allows industrial backplanes to safely be extended over cable between PLCs and I/O modules, for example. The maximum cable distance will depend on the allowable data rate, cable construction, and connector type, but at lower data rates such as 200 Mbps when using high speed connectors and appropriate shielded twisted pair cable, several meters of cable may be possible.

Analog-to-digital converter (ADC) interfaces typically utilize source synchronous data transmission with LVDS. This means that an LVDS clock is transmitted in parallel with one or more data bit streams on other LVDS channels. This is facilitated by the low channel-to-channel and part-to-part skew of the ADN4650, ≤300 ps and ≤500 ps respectively. These skew values specify the maximum difference between the high-to-low (or low-to-high) propagation delays across multiple channels, as statistically guaranteed for all ADN4650 devices across supply, temperature, and process. Low pulse skew of ≤100 ps allows for clock synchronisation when clocking data on both rising and falling clock edges for double data rate (DDR) as used by some convertors to increase output bandwidth.

Isolation of ADC sample clocks may be required in order to successfully fully isolate an analog front end that uses an external clock source—for example, a bank of multiple data acquisition channels all clocked together. This poses a challenge for any isolator, as any jitter on the clock will directly add to aperture jitter, reducing the measurement quality. In common with clock sources, LVDS signal chain components for clock distribution, such as fanout buffers, will typically specify this jitter as additive phase jitter. This means that the phase noise of the input clock is compared to the phase noise of the output clock with the difference integrated across a relevant range of frequencies—12 kHz to 20 MHz is common. The ADN465x family are essentially LVDS buffers with integrated isolation, so the same perspective is useful for analyzing the effect on the ADC sampling. By ensuring typical additive phase jitter of only 376 fs when using ADN465x, it's possible to maintain the original measurement quality even when adding galvanic isolation, especially as adding isolation may remove noise from digital circuits at the processor side.

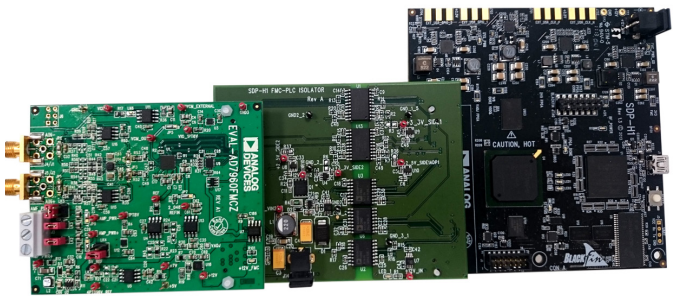

Figure 4. ADN4651 isolation circuit for AD7960 and SDP-H1.

Error-free transmission at 600 Mbps, synchronized to a 300 MHz clock, and full ADC performance and resolution when isolating the sample clock has been validated with the AD7960 18-bit, 5 MSPS, SAR ADC in a reference circuit, CN-0388 (shown in Figure 4). The existing ADC evaluation platform was isolated between the ADC circuit board and the high speed SDP-H1 evaluation platform using an interposer that transparently isolates the analog front end. The software is unchanged and evaluation to data sheet specifications using a precision analog source confirms the same performance as the nonisolated platform.

What Other Applications Can Use LVDS Isolation?

Isolated analog front ends or isolated industrial backplanes are two useful application examples to illustrate the opportunities offered in isolating LVDS, but there are many other applications for this technology. Video signals to flat panel displays commonly use LVDS signals, and HDMI® signaling uses similar differential signaling, common-mode logic (CML). These would not commonly need isolation, but for some applications such as medical imaging or external display ports in industrial PCs, galvanic isolation may protect humans or equipment, respectively.

About the Author

Dr. Conal Watterson is an applications engineer in the Interface and *i*Coupler® Digital Isolator Group at Analog Devices in Limerick, Ireland. A Ph.D. and M. Eng. graduate of the University of Limerick, since 2010, Conal has published a number of papers and articles on industrial fieldbus networks, diagnostics/reliability, and high speed signaling and isolation. His current focus topics are integrated isolated communication solutions and isolated power, high speed interfaces, and standards compliance for EMC and isolation.

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