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TECHNICAL ARTICLE

TAMING THE WIDEBAND CONUNDRUM WITH RF SAMPLING ADCS

Rob Reeder,
Duncan Bosworth,
Ronak Shah,
and Dan Pritsker

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Abstract

Modern electronic warfare (EW) system developers are facing multiple challenges including increased spectral congestion and surveillance of wider bandwidths at a greater level of detection sensitivity. In addition, the push on system developers to reduce development times strains many of the existing development models, resulting in custom hardware and firmware designs to achieve improved levels of performance within size, weight, and power constraints.

New gigasample per second (GSPS) high speed converters, high performance FPGAs, and FPGA IP cores are now changing the status quo, providing designers with off-the-shelf solutions and configurable building blocks to meet the next generation of challenges. A reference design, featuring Analog Devices GSPS ADCs with Altera® FPGAs and channelization IP, will show how designers can achieve faster time to market with state-of-the-art solutions for electronic intelligence and digital RF memory systems.

EW Overview

EW systems identify and counter electronic threats such as surveillance and tracking radars. EW systems are commonly categorized as either electronic support (ES), electronic attack (EA), or electronic protect (EP).

ES systems intercept and measure signal parameters to identify the signal's sources and perform threat analysis. The EA systems generate jamming signals to overpower the true pulse. Digital RF memory (DRFM) is a spoofing technique to deceive radars. The EP systems concentrate on processing and storing the incoming signals to construct a signal database. This database is a continuously updated lookup table used to identify future radar systems. Traditionally, these systems were developed on an analog platform. Modern systems are significantly more digital to take advantage of the signal processing capabilities available in the programmable logic devices.

Threat detection from unknown targets in these systems requires a receiver, which can operate over a wide frequency band to identify and initiate countermeasures to the threats. Typical EW systems may operate over a range from dc to 20 GHz. Beyond wide bandwidth requirements, practical EW systems require high dynamic range, high sensitivity, and accurate pulse characterization as new systems are being pushed to examine the bandwidths of interest faster with greater levels of detection sensitivity. More complicated situations arise when incoming signals to the EW system may be from numerous sources, each of which needs to be identified and distinguished. Independent of intentional interference from adversaries, increased spectral congestion, particularly from the rapid expansion of communications infrastructure, has made effective detection even more challenging.

Complex systems with even lower size, weight, and power targets are driving longer development cycles. However, next-generation, off-the-shelf solutions coupled with programmable building blocks provide solutions to these challenges. Two of the key building blocks critical for any EW system, the analog-to-digital converter and real-time channelization IP, will be examined further to illustrate how these challenges are being addressed.

ADC Bottleneck in EW Systems

In many instances, the high speed ADC transition from the analog to the digital domain is the limiting factor in ES, EA, and EP systems, where the system architect is often faced with a conundrum. While minimizing cost and system size are usually the top priority, the system designer must also strike an optimal balance between the need to increase instantaneous surveillance bandwidth to maximize the probability of interception, and how to minimize the effects of in-band, high power signals that desensitize the system. These requirements pose challenges in the converter design and the front-end design that couples the signal content to the converter. Even if the converter itself has excellent performance, the front end must be capable of preserving the signal quality, which results in the relentless push for performance and cost on the limits of high speed ADCs.

Figure 1 illustrates a simple EW system. The key features of the system are an RF receiver, used to downconvert and select the band of interest for interrogation, the ADCs used to transition the data from the analog-to-digital domain and the digital signal processing engine, which is typically an FPGA configured to detect, determine, analyze, and manage the storage of signals of interest. DRFM and EA systems also include a corresponding transmit chain utilizing a high speed DAC.

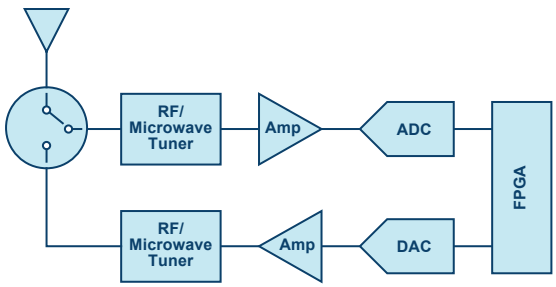

Figure 1. Typical EW architecture signal chain.

Historically, increasing the instantaneous bandwidth while maintaining the required linearity required using either multiple overlapping receivers or an interleaved architecture. The overlapped receivers each digitize a portion of the required bandwidth with digital signal processing used to recombine the data and observable spectrum from each channel. For interleaved architecture, it is often used with calibration required to minimize the phases, offset, and gain differences between the converters. Both options are generally expensive to implement but the digital signal processing is often customized to the implementation.

ADI's new RF sampling ADCs, such as the AD9625, offer solutions to the next generation of systems providing greater instantaneous bandwidth but with higher linearity to maintain the sensitivity levels required. The AD9625 is a 2.5 GSPS, 12-bit ADC that was designed to facilitate high bandwidth ac performance that offers unprecedented typical wideband SNR/SFDR of 57 dB/80 dB respectively with a 1 GHz input. This ADC also supports synchronizing of multiple converters, often required for angle of arrival determination, and has integrated digital downconverters (DDC) to decimate and observe a smaller portion of the frequency spectrum on the output.

The AD9625 is capable of a small signal analog bandwidth of over 3 GHz, and provides the system designer with significant IF location flexibility. With first and second Nyquist sampling options and over 1 GHz of usable bandwidth, the designer is able to maximize the front-end receiver architectures to achieve the optimal balance of filtering and system complexity.

ADI has devices that support parallel and serial interfaces including the JESD204B standard. This is important to support the high data rate and low latency requirements in many of the EW systems.

To facilitate rapid prototyping and system developments, the AD9625 is provided as a VITA 42/FPGA mezzanine card (FMC) platform (see Figure 2). This platform provides reference designs on how to optimize the signal conditioning in front of the ADC to optimize the performance, and ensures that the data processing interfaces between the ADC and processing units have sufficient bandwidth to support real-time, full rate data from the converter while still using a CoTs architecture. The result is an efficient architecture integrating 2.5 GSPS ADC COTS solution providing high speed conduit with minimum footprint.

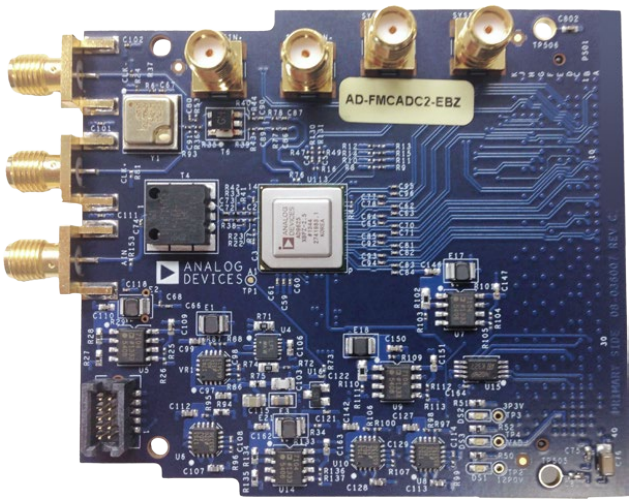

Figure 2. AD9625, 2500 MSPS, 12-bit FMC board with synchronization support. (PN: AD-FMCADC2-EBZ)

Channelizer Overview

Despite particular signal characteristics in EA, ES, and EP systems, a common component is the digital channelized receiver, or channelizer. The channelizer splits a wide bandwidth into smaller ones to separate signals of interests from noise and interferers so that low SNR and time sensitive signals can be reliably detected in individual subchannels. Most digital channelized receivers consist of a filter bank and fast Fourier transform (FFT).

As a design engineer, one of the challenges here is that every new EW design or upgrade usually requires developing a more complex channelizer. This is because new designs usually bring about necessary upgrades in hardware, providing for higher speed converters and more processing performance essential to keep up with ever changing global threats. To accelerate the development of the channelizer and reduce internal research and development (IRAD) cost, Altera has developed a super sample rate FFT IP and FIR filter IP core capable of handling multi-GSPS converter inputs. These IP cores will optimize a solution for you based on a wide set of input parameters, as shown in Figure 3.

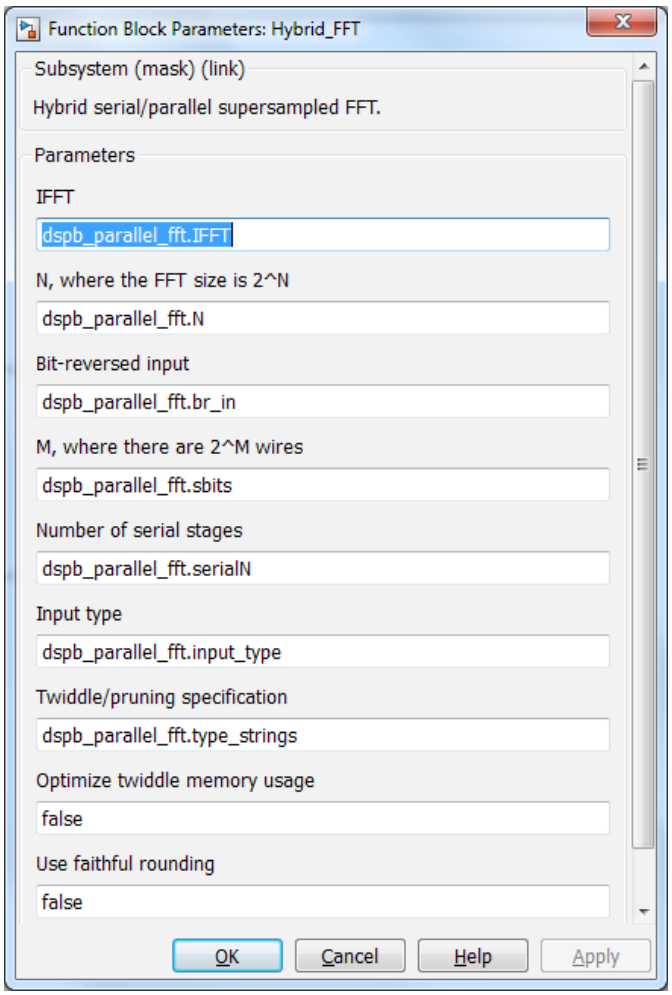

Figure 3. Altera super sample rate FFT configuration.

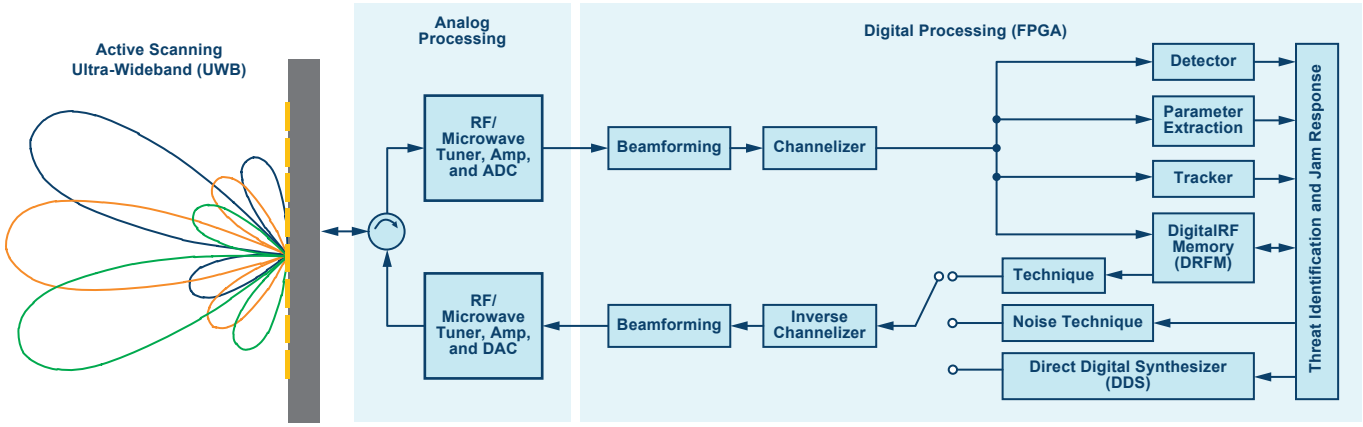

Figure 4. General electronic warfare system block diagram.

Figure 4 depicts the role of the channelizer in a general EW system block diagram, in which the digitized incoming radio frequency (RF) wideband signal is downconverted, and digitized before feeding into the channelized receiver. Signal detection and estimation are performed on individual channel outputs to discern threats from neutral and friendly signals. Once threats are identified and data based, certain EW systems will counter the threats through jamming. In this process, the receiver may produce various jamming signals. These jamming signals can appear in the forms of notched white noise or regenerated false reflection signals, that is, DRFM, to the hostile transmitter. The jamming signal passes through the inverse channelizer, whose role is to reconstruct a wideband reflection signal. The reflection signal is emitted after upconversion back to the hostile transmitter.

Hardware Demonstration

The project demonstrates the ADC interface and the channelizer function. A signal generator produces a sinusoidal tone as the AD9625 input. The AD9625 ADC output is connected to the Arria-V SoC development kit using the industry-standard FMC interface. The JESD204B standard defines data rates to logic devices in various lane configurations. The JESD204B interface in this demonstration is configured to use the 8-lane transceiver mode, as shown in Figure 5A and Figure 5B.

The samples received over JESD204B interface are fed into the channelizer IP, which is configured to receive 16 samples concurrently using 16 input wires (Parameter M in Figure 4). Depending on the number of FFT points, a full FFT frame is divided into multiple time slots. For example, a 1024-point FFT requires 1024/16 = 64 time slots to complete. Filter bank coefficients and FFT processing stages switch automatically according to the time slot.

Channelizer IP was developed using DSP builder advanced (DSPBA), which is a model-based design flow tool from Altera. It enables the signal processing engineers to design, evaluate, and verify their algorithms in MATLAB/Simulink environment. Once the algorithm is optimal, DSPBA generates a code that can be deployed on Altera FPGAs.

The channelizer output is stored in on-chip memory and is verified through the Altera system-in-the-loop (SIL) tool. The SIL uses a MATLAB API to trigger on-chip registers to start logging for data visualization. Once triggered, a single iteration of FFT processing is executed and the resultant data is stored into on-chip SRAM. The MATLAB API extracts data through the Altera Avalon memory map from SRAM to a MATLAB host. Once uploaded to MATLAB, the samples are plotted on the screen.

The integration of the IPs is done in Qsys. Qsys is an Altera's integration tool, which can significantly accelerate the development process by providing an integration framework. It enables hierarchical IP reuse and interconnect infrastructure using a graphical user interface.

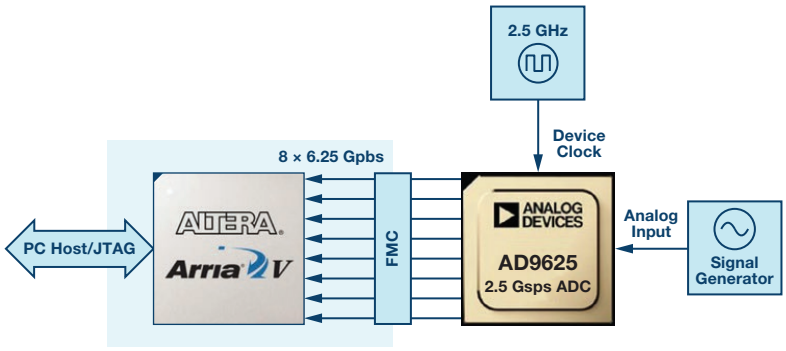

Figure 5A. AD9625 connects Altera Arria V via JESD204B interface.

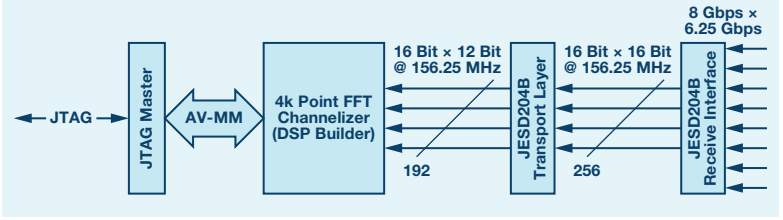

Figure 5B. Channlizer JESD204B input and Avalon memory map for Altera system-in-the-loop.

A Qsys project is created to integrate the channelizer IP and JESD204B IP. In addition to channelizer IP integration, the project incorporates control functionality to support SPI configuration interface to ADC.

The channelizer can switch to different FFT size easily through a MATLAB setup script. Such flexibility ensures a future upgrade path and potential design reuse across different system configurations. As an example, Figure 6 shows a 4096-point FFT output from the SIL.

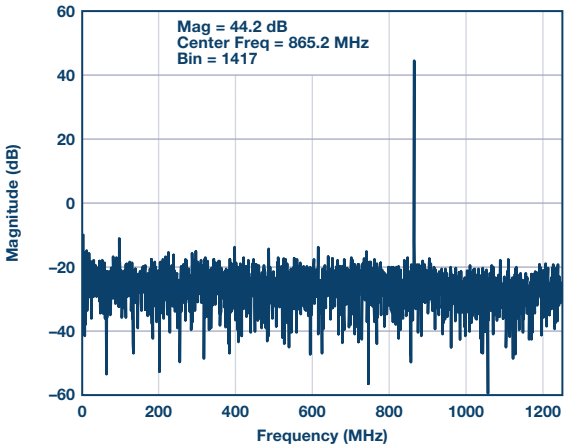

Figure 6. An example 4k-FFT channelizer output display through SIL.

Conclusion

Next-generation high speed converters offer solutions to provide higher instantaneous bandwidth without compromises on system sensitivity, and provide more flexibility in frequency planning or relieve a mix downstage on the front-end RF strip. However, achieving bandwidth data analysis in the 1 GHz range can pose challenges to designing a high performance system.

To solve this problem, channelizers can be used to analyze these wide bandwidths while maintaining high performance. These new GSPS RF ADCs coupled with new configurable channelizer IP cores provide next-generation system designers a faster solution to the ever changing electronic warfare environment.

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About The Authors

Rob Reeder is a senior system applications engineer at Analog Devices in the Aerospace and Defense Applications Group in Greensboro, N.C. He has published numerous papers on converter interfaces, converter testing, and analog signal chain design for a variety of applications. Formerly, Rob was an applications engineer for the high speed converter product line for eight years. His prior experience also includes test development as an analog design engineer for the MultiChip Products Group at ADI designing analog signal chain modules for space, military, and high reliability applications for five years. Rob received his M.S.E.E. and B.S.E.E. from Northern Illinois University in DeKalb, Illinois, in 1998 and 1996, respectively. When Rob isn't writing papers late at night or in the lab hacking up circuits, he enjoys crossfit workouts, building furniture out of old pallets, and most importantly, chilling out with his two boys.

Duncan Bosworth is the director of marketing and applications in the Aerospace and Defense Business Unit at Analog Devices. Prior to his role at Analog Devices, Duncan held senior defense focused engineering roles for over 17 years. Duncan received his M.Eng. from University of York, U.K., in 2001 and is a U.K. chartered engineer. Readers may reach him at *duncan.bosworth@analog.com*.

Ronak Shah manages a team of systems engineers focused on developing complex algorithms to market the capabilities of our chips and tools. Prior to joining Altera, Ronak spent seven years at Raytheon working on electronic warfare products. At Raytheon, Ronak lead research and development projects developing new systems with a focus on digital signal processing. Ronak has a bachelor's in electrical engineering from Calpoly, San Luis Obispo, and a master's in electrical engineering from University of California, Santa Barbara, with a focus in digital signal processing.

Dan Pritsker is a senior system design engineer in Altera Corporation. Dan joined Altera in 2010. Since then he has been working on a variety of projects and programs related to radar, guidance and control, electronic warfare, and hardware platforms design. Prior to Altera, Dan spent over 10 years in different engineering roles, working on the design of multidisciplinary systems. Dan has a master's degree in electrical engineering from Tel-Aviv University in Israel.

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Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643, U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Asia Pacific Headquarters
Analog Devices
5F, Sandhill Plaza
2290 Zuchongzhi Road
Zhangjiang Hi-Tech Park
Pudong New District
Shanghai, China 201203
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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