System-Level LO Phase Noise Model for Phased Arrays with Distributed Phase-Locked Loops

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Abstract

For digitally beamformed phased arrays, a common implementation method considered for the LO generation is to distribute a common reference frequency to a series of phase-locked loops distributed within the antenna array. With these distributed phase-locked loops, a method for assessing the combined phase noise performance is not well documented in current literature.

In a distributed system, common noise sources are correlated and distributed noise sources, if kept uncorrelated, are reduced when RF signals are combined. This is intuitive to assess for most components in the system. For a phase-locked loop there are noise transfer functions associated with every component in the loop, and their contribution is a function of the control loop and also any frequency translation. This adds complexity when attempting to assess a combined phase noise output. By building upon known phase-locked loop modeling methods, and an assessment of correlated vs. uncorrelated contributors, an approach to track distributed PLL contributions across frequency offsets is presented.

Introduction

In any radio system, careful design effort is placed on the implementation of the local oscillator (LO) generation for the receivers and exciters. With the proliferation of digital beamforming in phased array antenna systems, the design becomes additionally complicated with the distribution of LO signals and reference frequencies to a large number of distributed receivers and exciters.

A trade-off at the system architecture level is to distribute the LO frequencies needed or to distribute a lower frequency reference and to create the LO needed in close physical proximity to the point of use. A readily available and highly integrated option to create the LO locally is through a phase-locked loop. The next challenge is to assess a system-level phase noise from a variety of distributed components, as well as centralized components.

A system with distributed phase-locked loops can be considered as in Figure 1. A common reference frequency is distributed to many phase-locked loops each creating an output frequency. The LO outputs of Figure 1a are assumed to be the LO inputs to the mixers in Figure 1b.
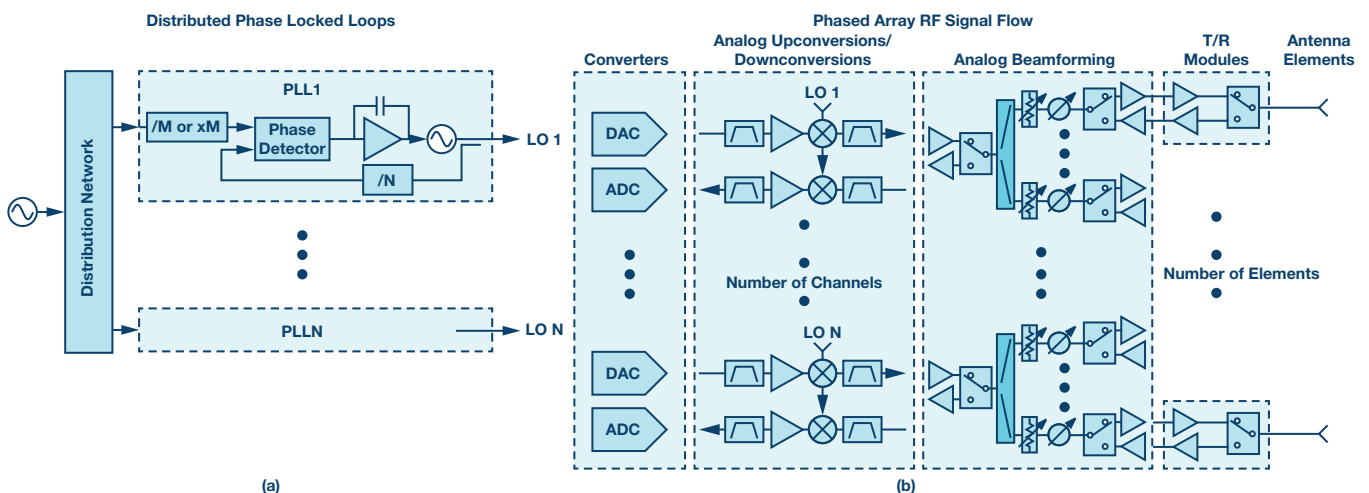

Figure 1. A system of distributed phase-locked loops. Each oscillator is phase-locked to a common reference oscillator. The LO signals, 1 to N, are applied to the LO ports of the mixers shown in the phased array.

A challenge for the system designer is tracking the noise contributions of the distributed system, understanding correlated vs. uncorrelated noise sources, and making an estimate of the overall system noise. In a phase-locked loop this challenge is compounded by noise transfer functions that are both a function of the frequency translation and loop bandwidth settings in the phase-locked loop.

Motivation: A Measured Example of Combined Phase-Locked Loops

An example measurement for combined phase-locked loops is shown in Figure 2. This data was taken by combining transmit output from multiple ADRV9009 transceivers. Cases for a single IC, two combined ICs, and four combined ICs are shown. In the case of this data set, there is a visible 10logN improvement as ICs are combined. In order to achieve the result a low noise crystal oscillator reference source was needed. The motivation to the model in the next section is to derive a method to calculate how this measurement would scale in a large array with many distributed transceivers and more generally to any architecture with distributed phase-locked loops.
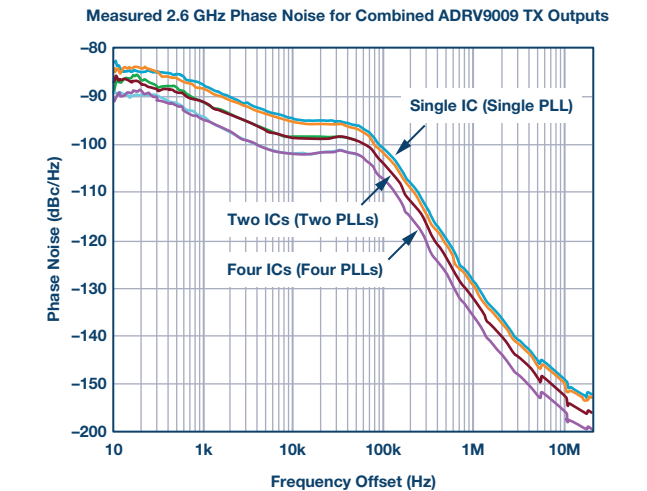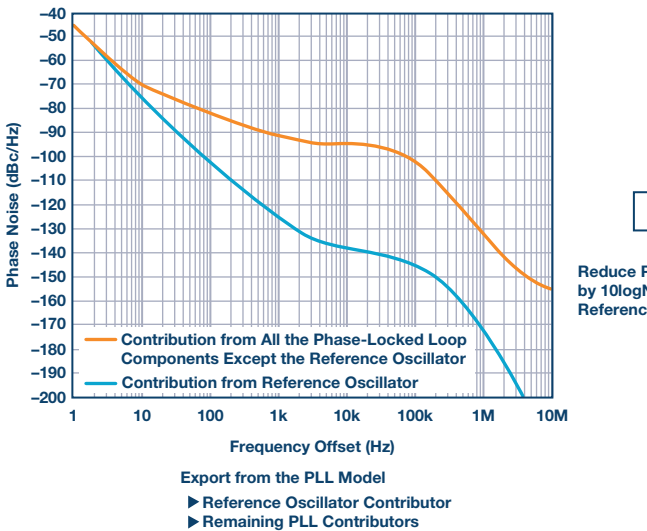
Measured 2.6 GHz Phase Noise for Combined ADRV9009 TX Outputs

Figure 2. Phase noise measurement of combined two phase-locked loops.

Phase-Locked Loop Model

Noise modeling in phase-locked loops is well documented.[1–5] An output phase noise plot is shown in Figure 3. In this type of plot, noise contributions for every component in the loop can be quickly assessed by the

designer, and the accumulation of these contributors leads to the overall noise performance. The model parameters were set to be representative of the data shown in Figure 2, and the source oscillator used to create a phase noise estimate if a large quantity of ICs were to be combined.

To examine the effect with a distributed phase-locked loop, first the reference contribution and the contribution from the remaining PLL components are exported from the PLL model.
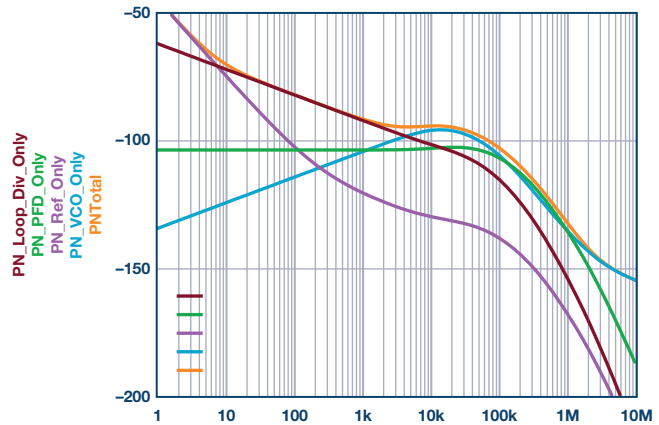
Figure 3. A typical phase-locked loop phase noise analysis showing the noise contributions of all the components. The total noise is the combination of all the contributors.

Extending Known PLL Models to Distributed PLL Models

Next, a process to calculate a combined phase noise for a system with many distributed phase-locked loops is described. This approach is based on being able to separate the noise contribution of the reference oscillator from the noise contributions of the VCO and loop components. Figure 4 illustrates a hypothetical distributed example of a single reference oscillator to many PLLs. This calculation assumes a noiseless distribution, which is not practical, but can be used to illustrate the principles. The noise contribution from the distributed PLL is assumed to be uncorrelated and reduced 10logN where N is the number of distributed PLLs. As channels are added, the noise is improved at larger offset frequencies and for large distribution systems the noise becomes almost completely dominated by the reference oscillator.
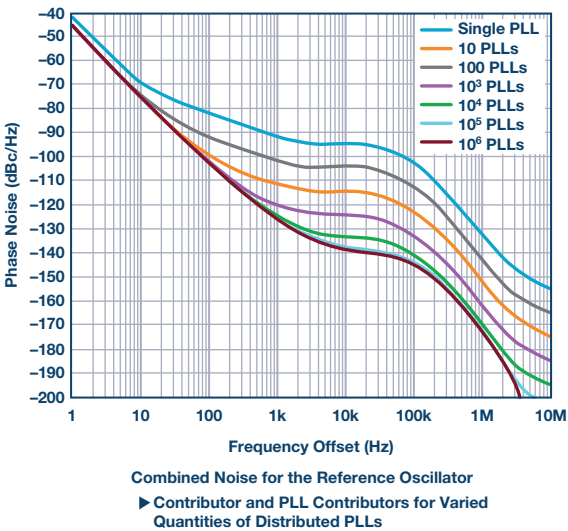

Figure 4. Beginning the distributed phase-locked loop phase noise modeling approach: the phase noise contributions of the reference oscillator and all the other components in the phase-locked loop except the reference oscillator are extracted from the PLL model. The combined phase noise as a function of the number of distributed phase-locked loops assumes that the reference noise is correlated and that the noise contributors distributed among many PLLs are uncorrelated.

The example illustrated in Figure 4 simplified assumptions on the reference oscillator distribution. In a true system analysis, it is expected that the system designer will also account for noise contributions in the reference oscillator distribution, which will degrade the overall results. However, a simplified analysis like this one is quite useful for gaining intuition on how architecture trade-offs may impact the overall system phase noise performance. Next we look at the impact of phase noise in the distribution system.

Accounting for Phase Noise in the Reference Distribution

Two examples of distribution options are evaluated next. The first case considered is shown in Figure 5. In this example, a wideband PLL is chosen that is common for the fast tuning of the VCO frequency. The distribution of the reference signal is implemented with clock PLL ICs that are also common to simplify timing constraints for digital data links such as JESD interfaces. Individual contributors are shown in the lower left. These contributors are at the frequencies of the device and are not scaled to the output frequency. The lower right phase noise plot shows the system-level phase noise for varying quantities of distributed PLLs.

A few features about the model are worth noting. A single high performance crystal oscillator is assumed, nominally at 100 MHz, and the central oscillator individual contributor is reflected on what is available in reasonably high end crystal oscillators, although not necessarily the best and most expensive choice available. While the central oscillator output would be practical to fan out to a limited number of distribution PLLs, these would fan out again to some practical limit and repeat to serve the complete distribution in the system. For the distribution contribution in this example, 16 distribution components are assumed, then these are assumed to fan out again. The individual contribution of the distribution circuitry shown in the lower left is the noise of the PLL components without the reference oscillator contribution. The distribution in this example is assumed to be at the same frequency as source oscillator and noise contributors were chosen based on typical ICs available for this function.

The wideband PLL is assumed nominally at S-band frequencies, set to a 1 MHz loop bandwidth for fast tuning, which is about as wide a loop as is practical.

It is worth noting that these models were chosen to be typical of what might be practical and illustrate the cumulative effect in an array. Any detailed design may be able to improve a particular PLL noise curve, which is anticipated, and this analysis method is intended to aid the engineering decision of where to allocate design resources for the best overall result and is not intended to make an exact claim relative to available components.

The lower right plot in Figure 5 calculates the total combined phased noise for the LO distribution. PLL noise transfer functions of each individual contributor are applied, which both scales to the output frequency and includes the effect of the PLL loop bandwidth. The system quantities are also included and assumed to be uncorrelated and, thus, that contribution is reduced by 10logN. For the distribution quantity, 16 is assumed, as previously described, and the distribution contribution is reduced by 10log16. In practice this would degrade further as the distribution is repeated. However, the additional noise contribution is less significant. For a fanout distribution in a large array, the noise will be dominated by the first set of active devices. In the case of a fanout by groups of 16, such that each active device is the input to 16 more active devices, the additional distribution layer of 16 degrades only by ~0.25 dB if all are uncorrelated to each other. Continuing the distribution will have even less overall contribution. Therefore, to simplify the analysis, this effect is not included and the noise contribution of the distribution is calculated from the first 16 parallel distribution components.

The resulting curve illustrates several effects. Similar to a single PLL model, the close in noise is dominated by the reference frequency, the far out noise is dominated by the VCOs, and the far out noise improves as uncorrelated VCOs are added together. This is fairly intuitive. What is not intuitive, and the value of the model, is a large section of offset frequencies dominated by the choice made in the distribution. This result leads to considering a second example with a lower noise distribution and a narrower PLL loop bandwidth.
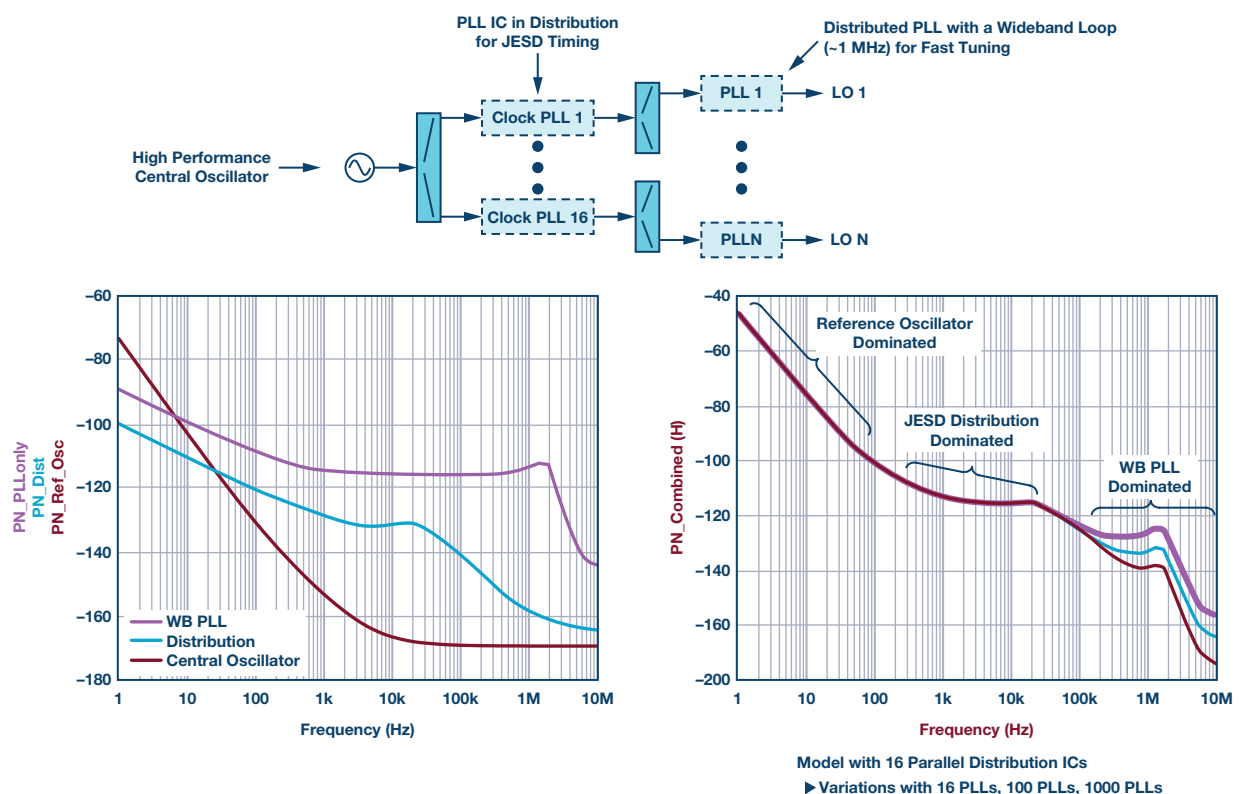

Figure 5. Distributed wideband PLL with a PLL IC in the distribution.
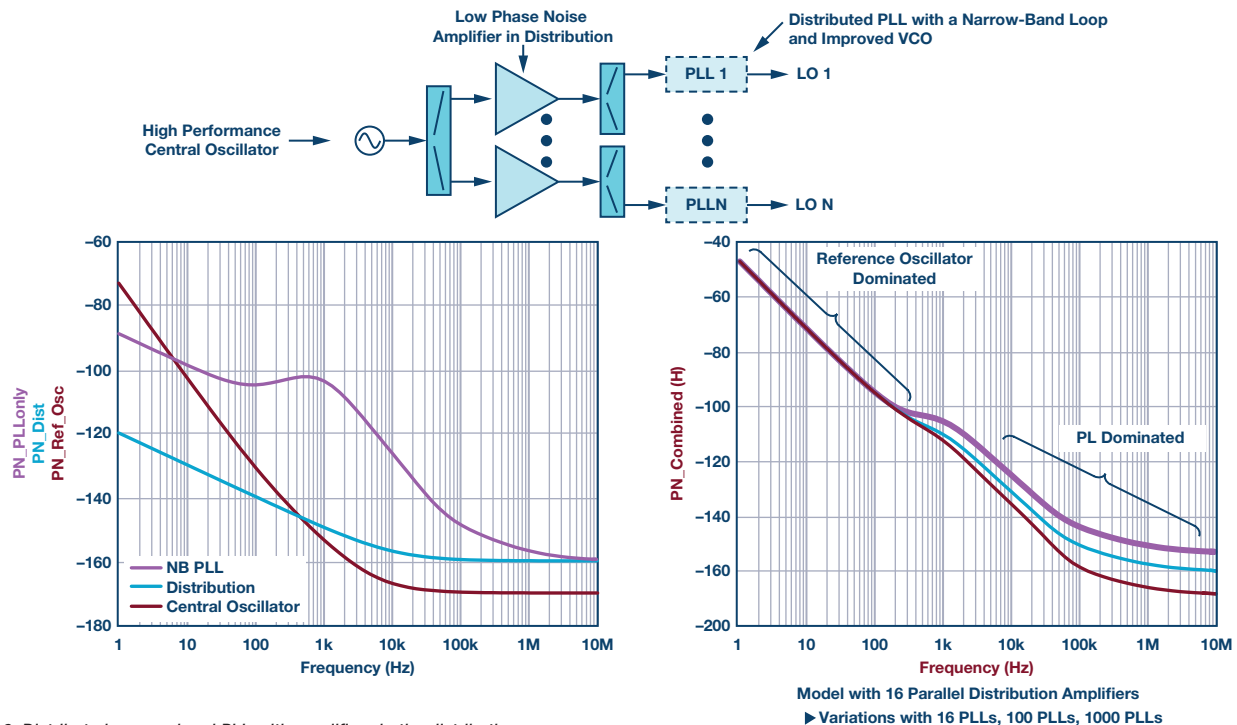
Figure 6. Distributed narrow-band PLL with amplifiers in the distribution.

Figure 6 illustrates a different approach. The same low noise crystal oscillator is used as a reference. This is distributed through RF amplifiers rather than retiming and resynchronizing through a PLL. The distributed PLL is chosen at a fixed frequency. This has two effects: at a single frequency with a narrow tuning range, the VCO can be intrinsically better, and the loop bandwidth can be made much narrower. The lower left plot shows the individual contributors. The central oscillator is the same as the previous example. Note the distribution amplifiers: they are not particularly high performance when considering low phase noise amplifiers, yet considerably better than using a PLL ICs such as the previous example. The distributed PLLs are improved at higher offset frequencies by both a better VCO and narrower loop bandwidth, but the mid frequencies of ~1 kHz are actually worse than the wideband PLL example. The lower right shows the combined result: the reference oscillator dominates the low frequencies, and above the loop bandwidth, the distributed PLL dominates performance and is improved with increasing the array size and quantities of distributed PLLs.

Figure 7 shows a comparison of the two examples. Note the wide range of differences in offset frequencies from ~2 kHz to 5 kHz.
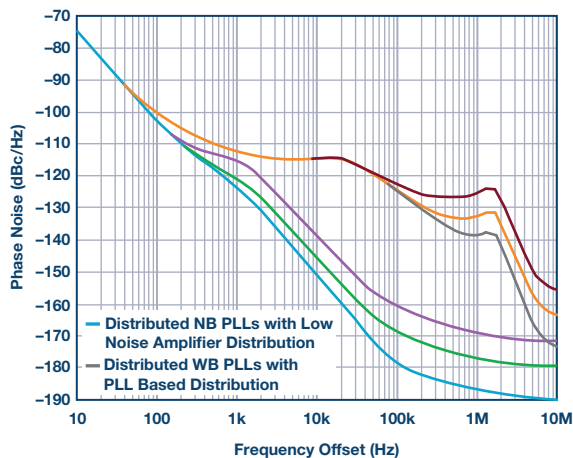

Figure 7. A comparison of Figure 5 and Figure 6 that illustrates the wide range of system-level performance dependent on the distribution and architecture chosen.

Distributed PLL Array-Level Considerations

Based on an understanding of weighted contributions to an overall system phase noise performance, several conclusions can be drawn relative to a phased array or multichannel RF system architecture.

PLL Bandwidth

Traditional phase-locked loop design optimized for phase noise sets the loop bandwidth at an offset frequency to minimize the overall phase noise profile. This typically is at a frequency where the reference oscillator phase noise normalized to the output frequency crosses the VCO phase noise. For a distributed system with many phase-locked loops this may not be the optimum loop bandwidth. The quantity of distributed components also needs consideration.

For optimum LO noise in systems implemented with distributed phase-locked loops, a narrow loop bandwidth is desired to minimize the correlated noise contributions of the reference.

For systems desiring fast tuning of PLLs, the loop bandwidth is typically widened to optimize speed. Unfortunately this by itself is the wrong direction for optimizing distributed phase noise contributions. One option to overcome this would be distributed narrow-band clean up loops prior to the wideband loop to reduce the offset frequency where reference and distribution noise is correlated.

Large Arrays

For systems employing thousands of channels, there is significant improvement to be gained from the distributed components if their contributions can remain uncorrelated. The primary concern may evolve around the selection of the reference oscillator and maintaining a low noise distribution system to the distributed receivers and exciters.

Direct Sampling Systems

With the proliferation of GSPS converters continually increasing in speed and RF input bandwidth, direct sampling systems are becoming realizable into the microwave frequencies. This leads to an interesting trade-off. The data converters need only a single clock frequency and the RF tuning is done completely in the digital domain. VCOs can be made with improved phase noise performance by limiting the tuning range. This also leads to a lower loop bandwidth for the PLLs creating the data converter clocks. The lower loop bandwidth will alter the noise transfer function of the reference oscillator to a lower offset frequency thus reducing its overall contribution to the system. This, combined with improved VCOs, may in some cases have benefits in a distributed system even if a single-channel comparison would appear to favor an alternate architecture:

Component Options

A large selection of component options available to the designer depending on the choices desired in the system architecture. An updated RF, microwave, and millimeter wave product selection guide for 2018 is available.

Recent integrated VCO/PLL options include the ADF4371/ADF4372. These provide an output frequency up to 32 GHz and 16 GHz, respectively, with a state-of-the art PLL phase noise FOM of −234 dBc/Hz. The ADF5610 provides an output up to 15 GHz. The ADF5355/ADF5356 output can operate up to 13.6 GHz, and the ADF4356 goes up to 6.8 GHz.

For separate PLL and VCO implementations, the ADF41513 PLL operates up to 26 GHz and includes a state-of-the art PLL phase noise FOM of −234 dBc/Hz. Sometimes, one consideration in selecting a PLL IC is to operate the phase detector at as high a frequency as possible to minimize noise in the loop from multiplying 20logN to the output. The HMC440, HMC4069, HMC698, and HMC699 operate with a PFD to 1.3 GHz. For VCOs, the 2018 selection guide lists dozens of VCO options ranging from 2 GHz to 26 GHz.

For direct sampling options, both ADCs and DACs have been released. The products enable direct sampling at L-band and S-band. The ADCs have a higher input frequency bandwidth that enables direct sampling into C-Band. The AD9208 is a dual 3 GSPS ADC with an input frequency to 9 GHz that enables sampling in the upper Nyquist zones. The AD9213 is a single 10 GSPS ADC that enables receivers with a large instantaneous bandwidths. For DACs, the AD917x series features dual 12 GSPS DACs, and the AD916x series features single 12 GSPS DACs that are optimized for lower residual phase noise and improved SFDR. Both families support L-band and S-band waveform generation.

This section merely offers guidance toward a starting point. New parts are rapidly emerging at higher frequencies and improved performance. Consult our website, *analog.com*, or your local sales support for the latest IC information.

Summary

A method for evaluating phase noise in a system with distributed phase-locked loops has been presented. The basis of the method is that every component can be tracked by its individual noise, the noise transfer function between the component and the system output, the quantity used, and any correlation between the devices. The examples shown are not intended to make a claim on available components or architecture capability. They are intended to illustrate an approach to aid designers in an educated assessment of array-level phase noise contributors in the LO and clock distribution networks servicing the distributed waveform generators and receivers in a digital beamforming phased array.

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