A Review of Wideband RF Receiver Architecture Options

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Introduction

The heterodyne receiver has been the standard receiver option of choice for decades. In recent years, the rapid advance of analog-to-digital converter (ADC) sampling rates, the inclusion of embedded digital processing, and the integration of matched channels now offers options for the receiver architect that were not practical only a few years ago.

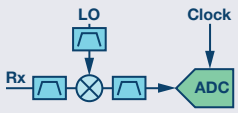
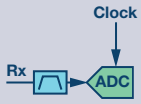
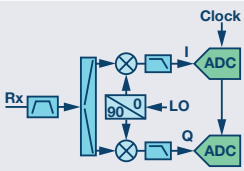
This article compares the benefits and challenges of three common receiver architectures: a heterodyne receiver, a direct sampling receiver, and a direct-conversion receiver. Additional consideration on spurious system noise and dynamic range is also discussed. The intention is not to promote one option over others—but rather describe the pros and cons of the options, and encourage the designer to select, through engineering discipline, the architecture most appropriate for the application.

Architecture Comparison

Table 1 compares the heterodyne, direct sampling, and direct-conversion architectures. The basic topology is shown along with some of the benefits and challenges of each architecture.

The heterodyne approach is well proven and provides exceptional performance. The implementation is to mix to an intermediate frequency (IF). The IF is chosen at a high enough frequency to allow practical filters in the operating band to provide good image rejection and LO isolation. It is also common to add an additional mixing stage to lower the frequency where very high dynamic range ADCs are available. Additionally, the receiver gain is distributed at different frequencies, which minimizes the risk of oscillation in high gain receivers. Through proper frequency planning, the heterodyne receiver can be made with very good spurious energy and noise performance. Unfortunately, this architecture is the most complicated. It typically requires the most power and the largest physical footprint relative to the available bandwidth. In addition, frequency planning can be quite challenging at large fractional bandwidths. These challenges are significant with the modern quest toward low size, weight, and power (SWaP), combined with the desire for wide bandwidth, and lead to designers considering other architecture options when possible.

Table 1. Receiver Architecture Comparison

Type	Configuration	Benefits	Challenges
Heterodyne		▸ Proven trusted ▸ High performance ▸ Optimum spurious noise ▸ High dynamic range ▸ EMI immunity	▸ SWaP ▸ Many filters
Direct Sampling		▸ No mixing ▸ Practical at L-, S-band	▸ ADC input bandwidth ▸ Gain not distributed across frequency
Direct-Conversion		▸ Maximum ADC bandwidth ▸ Simplest wideband option	▸ Image rejection • I/Q balance ▸ In-band IF harmonics ▸ LO radiation ▸ EMI immunity (IP2) ▸ DC and 1/f noise

The direct sampling approach has long been sought after. The obstacles have been operating the converters at speeds commensurate with direct RF sampling and achieving large input bandwidth. In this architecture, all the receiver gain is at the operating band frequency, so careful layout is required if large receiver gain is desired. Today converters are available for direct sampling in higher Nyquist bands at both L- and S-band. Advances are continuing and C-band sampling will soon be practical, with X-band sampling to follow.

Direct-conversion architectures provide the most efficient use of the data converter bandwidth. The data converters operate in the first Nyquist, where performance is optimum and low-pass filtering is easier. The two data converters work together sampling I/Q signals, thus increasing the user bandwidth without the challenges of interleaving. The dominant challenge that has plagued direct-conversion architecture for years has been to maintain I/Q balance for acceptable levels of image rejection, LO leakage, and dc offsets. In recent years, the advanced integration of the entire direct-conversion signal chain, combined with digital calibrations, has overcome these challenges and the direct-conversion architecture is well positioned to be a very practical approach in many systems.

Frequency Plan Perspective

Figure 1 illustrates block diagrams and frequency plan examples of the three architectures. Figure 1a is an example of a heterodyne receiver with a high-side LO mixing the operating band to the 2nd Nyquist zone of the ADC. The signal is further aliased to the 1st Nyquist zone for processing. Figure 1b shows a direct sampling receiver example. The operating band is sampled in the 3rd Nyquist zone and aliases to the 1st Nyquist, then an NCO is placed in the center of the band, digitally downconverting to baseband, followed by filtering and decimation, reducing the data rate commensurate with the channel bandwidth. Figure 1c is a direct-conversion architecture example. By mating the dual ADC with a quadrature demodulator, Channel 1 samples the I (in phase) signal and Channel 2 samples the Q (quadrature) signal.

Many modern ADCs support all three architectures. For example, the AD9680 is a dual, 1.25 GSPS ADC with programmable digital downconversion. A dual ADC of this type supports 2-channel heterodyne and direct sampling architectures, or the converters can work as a pair in a direct-conversion architecture.

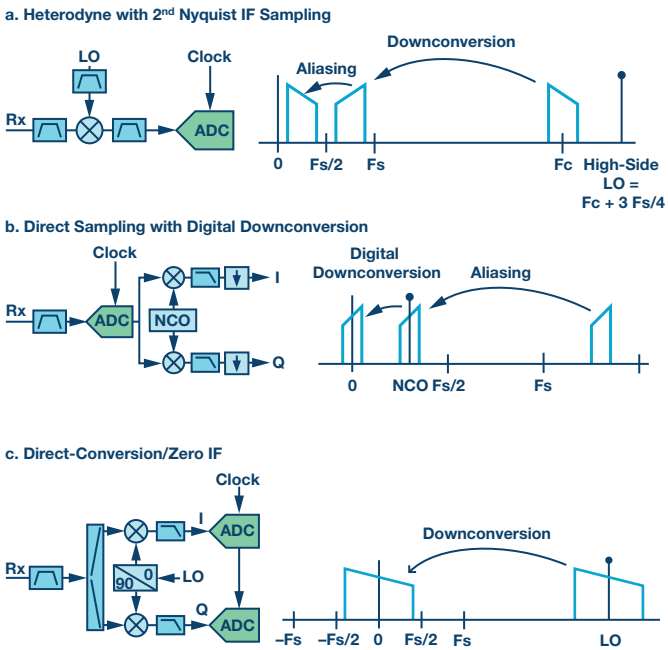


Figure 1. Frequency plan examples.

The image rejection challenges of the direct-conversion architecture can be quite difficult to overcome in a discrete implementation. With further integration combined with digitally assisted processing, the I/Q channels can be well matched, leading to much improved image rejection. The receiver section of the recently released AD9371 is a direct-conversion receiver and shown in Figure 2—note the similarity to Figure 1c.

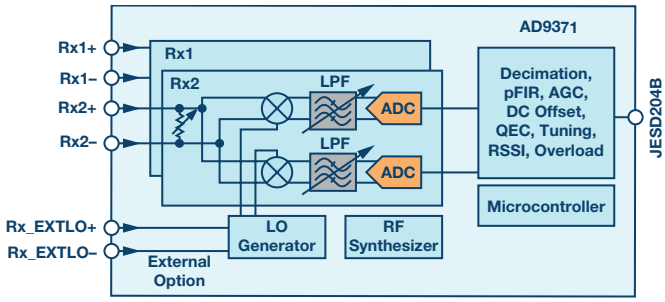


Figure 2. Receiver section of the AD9371: A monolithic direct-conversion receiver.

Spurious Noise

Any design with frequency translation requires much effort to minimize unwanted frequencies folding in-band. This is the art of frequency planning and involves a balance of available components and practical filter design. Some of the spur folding concerns are briefly discussed and the designer is referred to the references for further explanation.

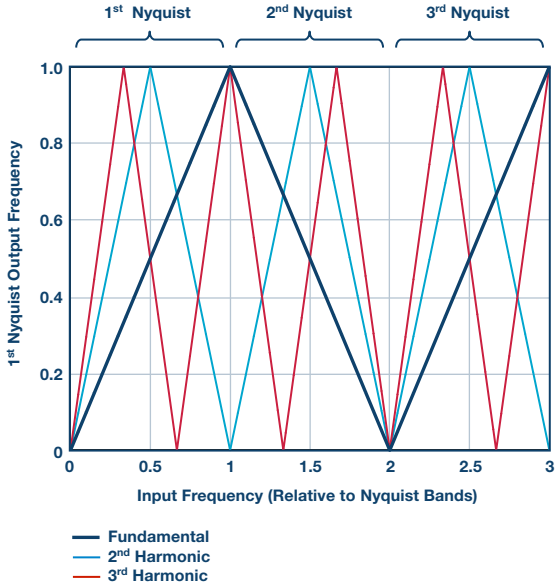


Figure 3. ADC frequency folding.

Figure 3 shows the folding of the ADC input frequency and the first two harmonics as a function of input frequency relative to the Nyquist band frequencies. For channel bandwidths much less than the Nyquist bandwidth, a goal for the receiver designer is to select operating points that place the folded harmonics out of the channel bandwidth.

The receiver downconversion mixer has additional complications. Any mixer creates harmonics inside the device. These harmonics all mix together and create additional frequencies. This effect is illustrated in Figure 4.

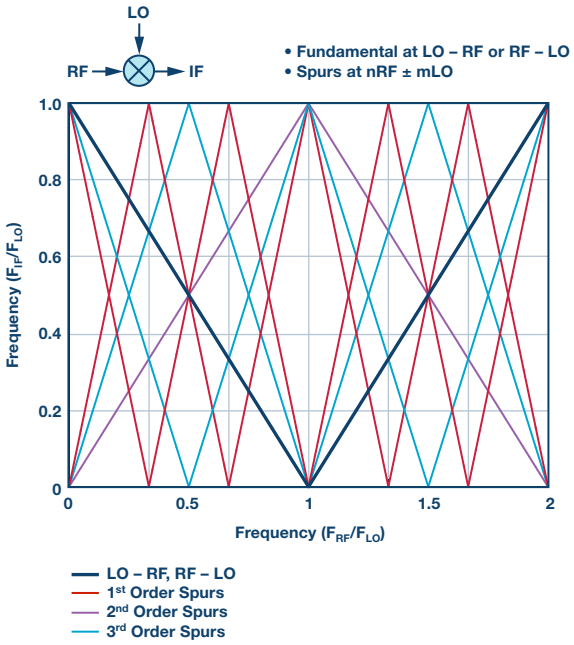


Figure 4. Downconversion mixer spurious.

Figure 3 and Figure 4 only plot spurs up to the third order. In practice, these are spurs of additional higher order, which quickly creates a spurious-free, dynamic range issue for the designer. For narrow fractional bandwidths, meticulous frequency planning can overcome the mixer spurious problems. As bandwidths increase, the mixer spurious problem becomes a dominant obstacle. As ADC sampling frequencies increase, it is sometimes more practical for a direct sampling architecture to have lower spurious performance.

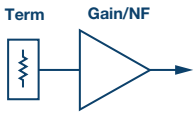
Receiver Noise

Much receiver design effort is placed on minimizing noise figure (NF). Noise figure is a measure of the degradation in signal to noise ratio.

$$F = \frac{(S/N)_{In}}{(S/N)_{Out}}, \text{ standardized at 290 K } (T_O) \tag{1}$$

$$NF = 10\log F$$

The impact of a component or subsystem noise figure is that the output noise power is increased above the level of thermal noise and gain by the noise figure.



(2)

$$Noise\ Power\ Out = -174\ dBm/Hz + Gain(dB) + NF(dB)$$

Cascaded noise figure is calculated as

$$F_{Total} = F_1 + \frac{F_2 - 1}{Gain_1} + \frac{F_3 - 1}{Gain_1 \times Gain_2} + \ldots + \frac{F_N - 1}{Gain_1 \times Gain_2 \times \ldots \times Gain_{N-1}} \tag{3}$$

The selection of receiver gain prior to the ADC and determining the required ADC SNR is a balance of the overall receiver noise figure and instantaneous dynamic range. Figure 5 provides a representation of the parameters to be considered. For illustrative purposes, the receiver noise is shown to be shaped by the antialiasing filter prior to the ADC. The ADC noise is shown as flat white noise and the signal of interest is shown as a continuous wave (CW) tone at –1 dBFS.

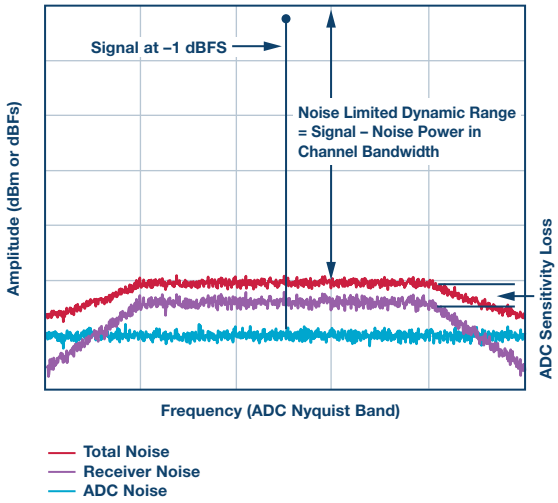


Figure 5. Receiver + ADC noise.

First, common units of either dBm or dBFS are needed. Converting the ADC noise from dBFS to dBm is known from the converter full-scale level and the converter noise density. In addition, noise power is proportional to bandwidth, so a common bandwidth unit is needed. Some designers will use the channel bandwidth, here we normalize to a 1 Hz bandwidth and noise powers are /Hz.

$$ADC\ noise(dBm/Hz) = ADC\ full\ scale(dBm) + ADC\ noise\ density(dBFS/Hz) \tag{4}$$

The total noise is calculated as

$$Total\ Noise\ (dBm/Hz) = 10\log_{10}\left(10^{\frac{\text{Receiver Noise } (dBm/Hz)}{10}} + 10^{\frac{\text{ADC Noise } (dBm/Hz)}{10}}\right) \tag{5}$$

This leads to the concept of ADC sensitivity loss. ADC sensitivity loss is a measure of the receiver noise degradation due to the ADC. To minimize this degradation, the receiver noise is desired to be well above the ADC noise. The limitation comes in the form of dynamic range and larger receiver gain limits the maximum signal received without ADC saturation.

$$ADC\ Sensitivity\ Loss\ (dB) = Total\ Noise\ (dBm/Hz) - Receiver\ Noise\ (dBm/Hz) \tag{6}$$

Thus, the receiver designer faces a constant challenge of balancing dynamic range vs. noise figure.

Conclusion

The heterodyne, direct sampling, and direct-conversion receiver architectures have been reviewed with emphasis on benefits and challenges of each architecture. Recent trends and considerations in receiver design have also been presented. With the worldwide desire for more bandwidth, combined with the advancement of GSPS data converters, it is anticipated that many varied receiver designs will proliferate well into the future.

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Peter Delos is a technical lead at Analog Devices, Inc., in the Aerospace and Defense Group. He received his B.S.E.E. from Virginia Tech in 1990 and M.S.E.E. from NJIT in 2004. He has over 25 years of industry experience.

Most of his career has been spent designing advanced RF/analog systems at the architecture level, PWB level, and IC level. His career includes various positions in the Naval nuclear power submarine program and at Lockheed Martin, Moorestown, NJ, in multiple radar and EW programs. In 2016, he accepted his current position with Analog Devices in Greensboro, NC.

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