

Replacing YIG-Tuned Oscillators with Silicon by Using an Ultrawideband PLL/VCO with Precise Phase Control

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RF and microwave instruments, such as signal and network analyzers, require wideband, swept frequency signals to make many of their basic measurements. Yet, perversely, wideband voltage controlled oscillators (VCOs) typically have the worst phase noise due to the low Q and high K_{VCO} (a VCO's tuning sensitivity in MHz/V) required to maximize their tuning ranges. Yttrium iron garnet (YIG) tuned oscillators (YTOs) neatly solve this problem with good, wideband phase noise performance and an octave of frequency tuning range but can be large, expensive, and can consume hundreds of mA current due to their tuning currents. And of course they still require an external phase-locked loop (PLL) to close the loop and a voltage controlled current source to provide their tuning current.

A YIG crystal sphere looks like a high Q LC circuit whose resonant frequency is linearly proportional to an externally applied magnetic field. The oscillator is tuned by a current through a single turn loop through an octave or more in the GHz range. YIG tuned oscillators exhibit a low level of phase jitter, and their broadband characteristics from approximately 2 GHz to 18 GHz (with a very linear tuning curve) make them a popular choice for many measurement applications.

However, the performance gap between YIG-tuned oscillators and integrated PLL/VCO ICs is closing. For example, recent advances in integrated PLL/VCO ICs, such as the Analog Devices [ADF4355](#), have much improved phase noise over their predecessors. They have also solved the wide tuning range issue by design techniques such as dividing the output frequency range into multiple, adjacent subbands, where each subband can have a dedicated band switched VCO to increase tuning range while making the band switched VCOs look like a single VCO with a moderate K_{VCO} (shown in Figure 1) to the user. Next, auxiliary frequency dividers and doublers extend the frequency coverage of the VCO's tuning range both above by multiplication and below by division. For example, the ADF4355's fundamental tuning range of 3.4 GHz to 7.2 GHz is extended down to 54 MHz by division. Each time the frequency is halved the phase noise improves by 3 dB (shown in Figure 2).

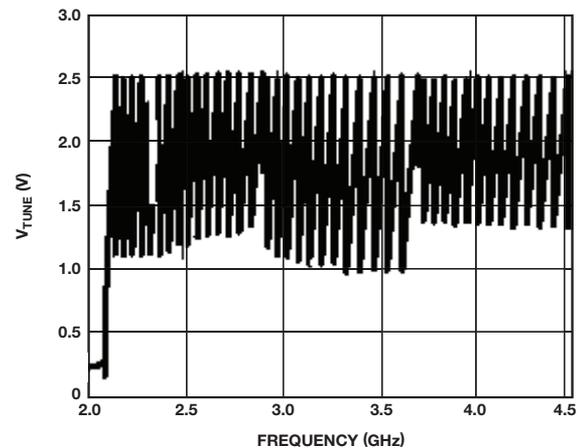


Figure 1. The multiband VCO in the ADF4355 PLL/VCO consists of an array of oscillators, each tuning a fraction of the entire band and maintaining a uniform K_{VCO} and thus V_{TUNE} across the entire range. The shape of the tuning voltage plot looks like a sawtooth because each oscillator has fixed capacitors that are switched in parallel with the voltage variable capacitance one at a time to maximize each VCO's overall tuning range.

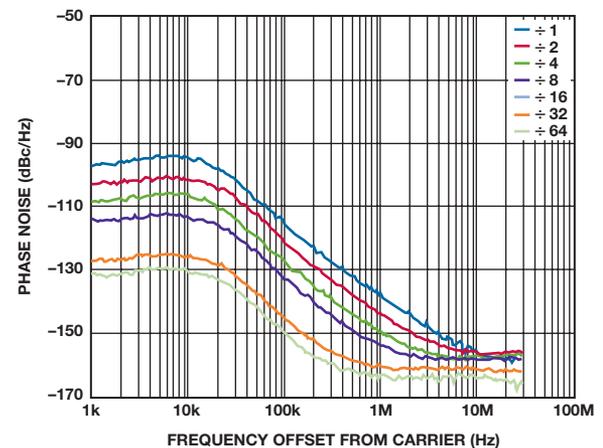


Figure 2. Each time the output frequency is halved, the overall phase noise improves by 3 dB. In this case, dividing the 3.4 GHz VCO by 64 GHz results in phase noise of better than -130 dBc/Hz at a 10 kHz offset at 53.125 MHz.

Yet, even if an integrated PLL/VCO IC has a more comparable tuning range than a YIG-tuned oscillator, one problem still remains: YIG-tuned oscillators still provide 12 dB better phase noise performance than the best integrated VCOs. Even this gap can be reduced if not yet closed, by combining the outputs of multiple PLL/VCOs in parallel (as shown in Figure 3). The outputs can be summed and the phase noise improved by 3 dB for each doubling (3 dB) of the number of PLL/VCOs in parallel. For example, two ADF4355 PLL/VCOs provide a 3 dB improvement, four ADF4355 PLL/VCOs provide a 6 dB improvement, and eight ADF4355 PLL/VCOs provide a 9 dB improvement (as shown in Figure 4).

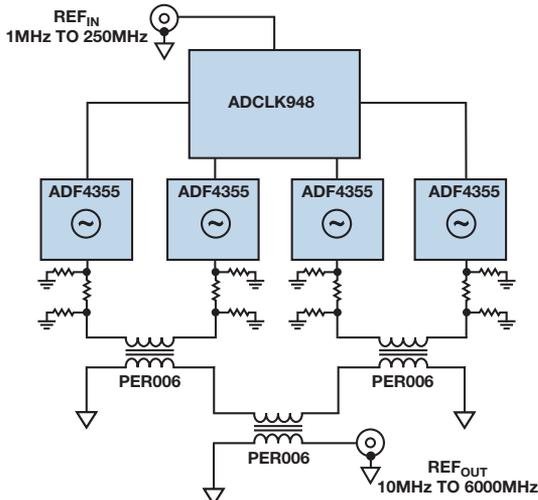


Figure 3. By synchronizing multiple PLL/VCOs and combining their outputs you can improve the phase noise by 3 dB for each doubling of the number of VCOs. Four ADF4355s are shown in parallel here and provide a 6 dB improvement in overall phase noise.

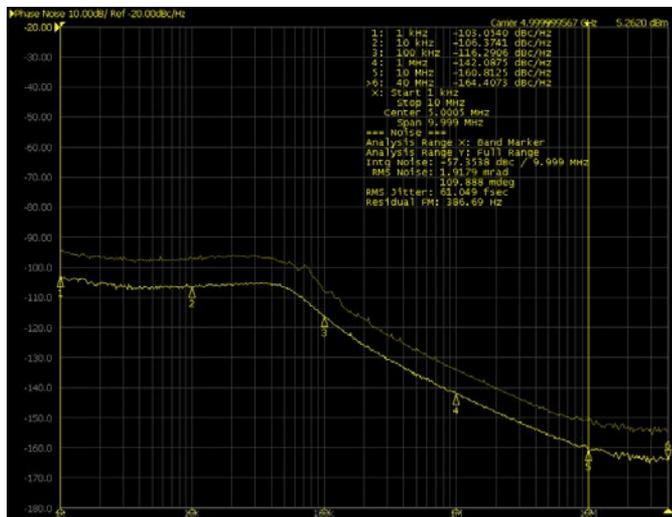


Figure 4. By phase locking and combining the outputs of eight ADF4355 PLL/VCOs you can improve the overall phase noise by nearly 9 dB over that of a single PLL/VCO. The spectrum here shows both the output phase noise of a single ADF4355 and the phase noise of the summed outputs of eight synchronized ADF4355s operating in parallel.

The key to summing the outputs of the PLL/VCOs is operating the outputs of all the oscillators in phase. The example we'll discuss here uses four PLL/VCOs in parallel. As one might guess, placing four phase-locked loops and voltage controlled oscillators at the same frequency, on the same printed circuit board, carries with it a number of challenges. Chief among these challenges is isolation. Poor isolation between PLLs can result in a phenomenon known as injection locking (as seen in Figure 5), in which an oscillator locks to a strong signal or harmonic thereof, in preference to the frequency selected by the tuning voltage supplied from the phase-locked

loop itself. Injection locking is observable by seeing an initially subtle degradation in noise and spurious, as the two locking mechanisms generate intermodulation distortion. In more severe cases the signal will look more like a modulated carrier than a continuous sine wave tone.

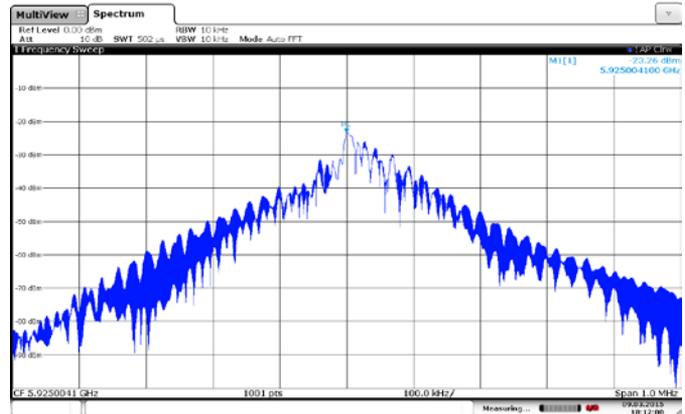


Figure 5. Injection locking occurs when the frequency of a VCO locks to an external oscillation rather than its control voltage. The result is increased intermodulation and phase noise.

Isolation requires a variety of techniques and circuitry. For example, buffer the reference signal to each PLL (pins REF_{INA} and REF_{INB}) by using a buffer, in this case the ADI ADCLK948 LVPECL 8:1 clock buffer. Additionally, minimizing crosstalk requires correct terminations of the source, and load pins as close to the source and load as possible. Extra shunt capacitance to ground (18 pF) was also included to attenuate any leakage from the VCO's output while passing the desired reference frequency.

Other paths requiring isolation are the power supply lines. To provide the required isolation, each PLL has its own high performance regulator (the ADI ADM7150), one for the +5 V lines, V_{VCO}, V_P, and V_{REGVCO}; the VCO supplies being the more critical here. The analog (AV_{DD}), digital (DV_{DD}), and output stage (V_{RF}) lines also require 3.3 V, and separate regulators for each line are also used. It is acceptable to tie the 3.3 V lines on each PLL together provided that good decoupling has been used.

On the RF output stage, the auxiliary output (pins RF_{OUTB+} and RF_{OUTB-}) is disabled and terminated to ensure no unwanted tones are generated. Output RF_{OUTA-} is terminated in a 50 Ω load, and its complementary output, RF_{OUTA+} is fed to a high isolation power combiner (Marki Microwave, PBR0006SMG). This combiner was chosen to ensure that coupling between the output stages is kept to a minimum while providing a combined signal at the common output. To improve isolation, a pair of these combines the outputs of two PLLs, and a third combiner sums the output of the first two.

Finally, an off the shelf shield from Laird provides additional isolation to minimize any stray radiation that might couple the VCOs electromagnetically. Taken together, all of these steps ensure the best possible isolation.

The ADF4355 contains a high resolution 24-bit modulator, which in addition to allowing the generation of fractional-N divide values, also contains circuitry, which permits small adjustments of the phase of the RF signal. To be useful, the phase values need to be repeatable. This requires the use of the function phase resync.

Phase resync is best described as a function that puts the fractional divider (a Σ-Δ modulator with noise shaping) into a known state after a frequency update. Because phase is a relative measurement, the resync function is defined as functional when changing from a frequency F1 with phase P1 to frequency F2, and when changing back to frequency F1, the phase should again be P1 as in the first measurement. This function combined with resync allows us to adjust the phase to minimize the phase difference between each of the four PLLs to get the maximum power sum of the power from the four PLLs and thus, the biggest improvement in phase noise. In addition to these

steps, it is also important to reset the counters of each PLL simultaneously, and this is easily achieved by a hardware power-down and power-up using the chip enable (CE) pin.

Process and part to part variation means that we cannot assume that the phase difference between each PLL, when following reset and resync procedures, will be close enough to zero to maximize signal-to-noise; thus an external calibration circuit is required.

The calibration procedure is simple: turn on a single PLL/VCO and define its phase as phase zero. Turn on each additional PLL/VCO in turn, change its output phase until the combined output power of the on PLL/VCOs is at a maximum, then turn on the next VCO and again tune its phase until the combined output power of the PLL/VCOs is again at a maximum. Note, that the largest change in power occurs when the second PLL/VCO is turned on as the combined power is doubled; the difference decreases for each subsequent PLL/VCO. In practice this means the signal-to-noise increases each time the number of PLL/VCOs in parallel doubles. That is, two in parallel provide a 3 dB improvement, four provide a 6 dB improvement, and eight provide a 9 dB improvement. Of course the complexity of the power combiner doubles as well, so four PLL/VCOs is a practical upper limit with diminishing returns for eight and 16 PLL/VCOs in parallel.

Note, that best phase performance and maximum output power are coincidental, so a power measurement is sufficient to ensure best phase noise performance. The calibrator in our case is an ADI ADL6010 power detector to measure the output amplitude of the combined signals. In this manner the phase of each PLL (at each frequency) can be adjusted, and the phase adjustment constant when the combined power has reached a maximum (as shown in Figure 6). This process is repeated for each additional PLL until all four PLLs have been powered up and adjusted, such that the signal at the output of the combiners is at a maximum.

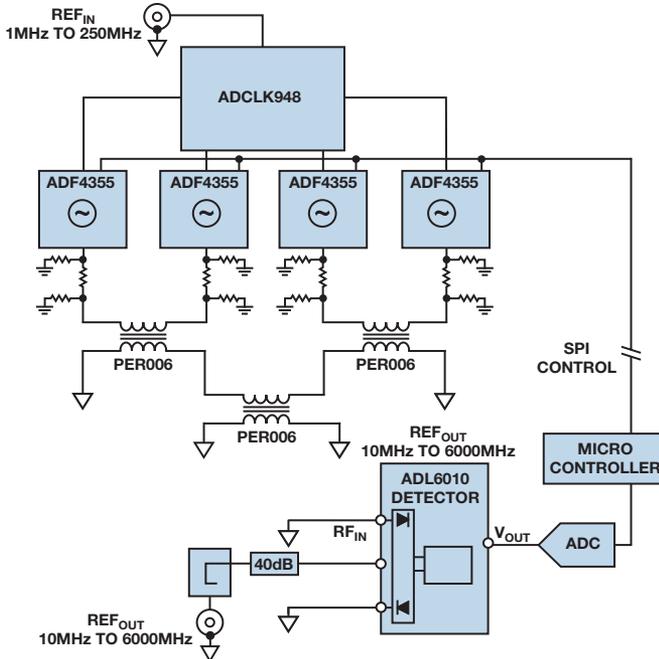


Figure 6. Four phase aligned ADF4355 integrated PLL/VCOs shown with an ADCLK948 clock buffer, combiners (PBR-0006SMG), and calibration circuitry.

Figure 7 shows that practical results follow theory, that for each doubling of PLL/VCOs and with the correct phase word written, the combined phase noise of the four PLL/VCOs improves by 6 dB over that of a single PLL/VCO. Thus, the performance of one ADF4355 PLL (-134 dBc/Hz at a 1 MHz offset) can be improved by 6 dB to about -140 dBc/Hz when four PLL/VCOs are combined in phase.

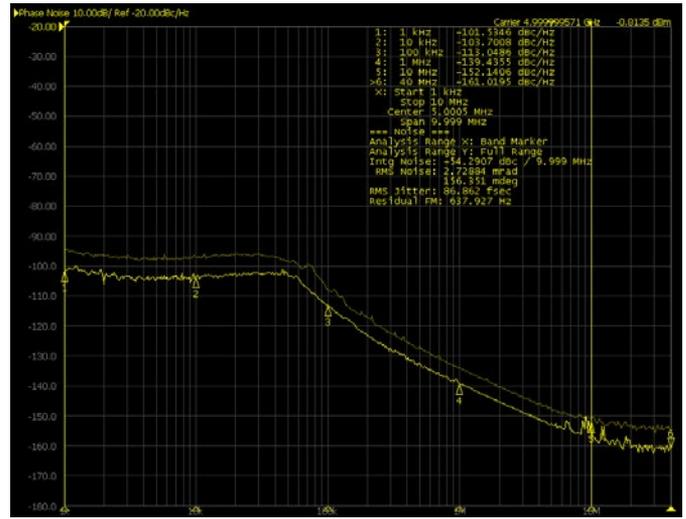


Figure 7. Output phase noise plot showing the phase noise of a single ADF4355 PLL/VCO oscillator and four ADF4355s combined in phase.

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