Receiver IC Blend Mixers, Synthesizers, and IF Amps

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Wireless base stations were once contained in large, climate controlled spaces—but now, they could be mounted anywhere. As wireless network service providers attempt to achieve coverage everywhere, the pressure is on base station component suppliers to provide more functionality in smaller packages.

A pair of integrated circuits (ICs) from Analog Devices provides a solution by redefining the meaning of mixer in receiver front ends. Essentially, the ICs incorporate many of the components once added to a mixer in a receiver—such as local oscillators (LOs) and intermediate frequency (IF) amplifiers—within the mixer IC itself. They make it possible to dramatically shrink a cellular base station, while also providing software-defined radio (SDR) flexibility to handle a number of different wireless standards.

The ICs in question are the models ADRF6612 and ADRF6614, both designed for RF ranges of 700 MHz to 3000 MHz, LO ranges of 200 MHz to 2700 MHz, and IF spans of 40 MHz to 500 MHz. They work with low- or high-side LO injection and include an on-board, phase-locked loop (PLL) and multiple low noise voltage controlled oscillators (VCOs), all packed within a 7 mm × 7 mm, 48-lead LFCSP housing. This level of integration and component density is enhanced by the diversity and programmability to support a number of different wireless standards in the small volumes required by modern microcells.

To appreciate the savings in space offered by these highly integrated mixer ICs, it may help to remember the front end of a cellular base station receiver from around 2010, as seen in Figure 1. The dual-mixer architecture covered a bandwidth of approximately 1 GHz, requiring multiple components to handle the then cellular frequency range of 800 MHz to 1900 MHz. Frequency synthesis was provided by a separate PLL and narrow-band VCO module that required a unique PLL loop filter for optimum performance. Dedicated VCO modules were used for each band of interest, adding to the required circuit board area within the base station.

In addition, these discrete components were interconnected by low impedance transmission lines that contributed some signal loss. As a result, generous current was needed to drive the VCO output to a sufficient level for the mixer to generate low phase noise and noise figure under signal blocking conditions.

Receiver ICs with integrated VCOs are not new. But achieving the wide bandwidths and low phase noise levels required by multiple carrier, global system for mobile communications (MC-GSM) wireless networks has been a challenge. The channel reuse scheme of GSM requires that receive LOs have extremely low phase noise, particularly at an alternate channel offset frequency of 800 kHz, shown in Figure 2. If excessive phase noise at these alternate channels mixes with unwanted signals at the same 800 kHz offset, it can result in phase noise translated to the IF output degrading system sensitivity.

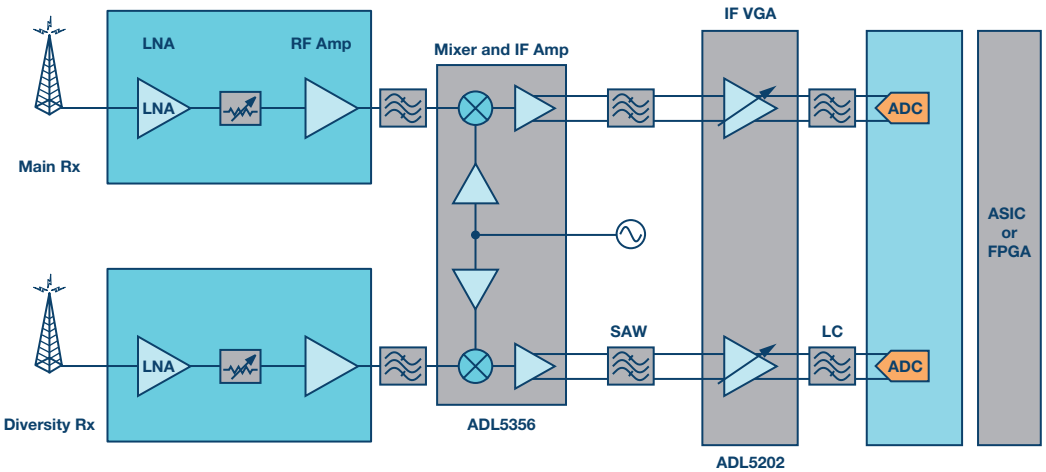


Figure 1. The block diagram represents a typical cellular wireless base station from about 2010.

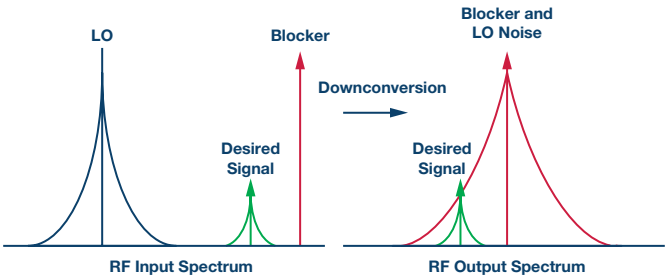
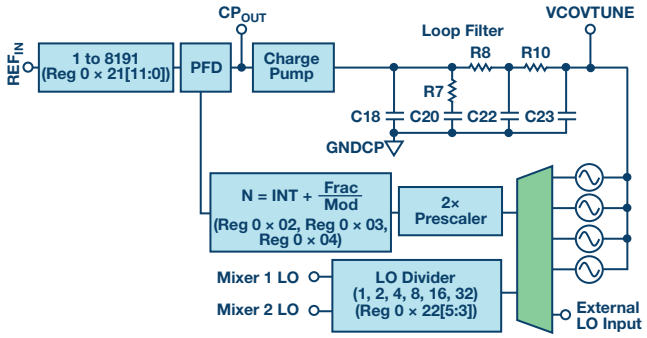


Figure 2. The channel reuse scheme requires the use of wide bandwidth VCOs with low phase noise in GSM wireless systems to avoid performance degradation due to blocking.

Low VCO phase noise is typically achieved with a high quality factor (high-Q) tank and narrow-band design. Frequency division can also reduce noise. By operating a VCO at an integer multiple of a receiver's LO frequency, a 6 dB/octave reduction in phase noise is achieved by the subsequent division, which is displayed in Figure 3. The phase noise requirements for GSM in the 1800 MHz to 1900 MHz band are extremely difficult—roughly twice as severe as those in the 800 MHz to 900 MHz band.



ADRF6614 GSMVCO1 Phase Noise—Locked
f_{REF} =153.6 MHz, f_{PFD} = 1.6 MHz, Bleed = 32 (0 µA), CSCALE = 8 mA

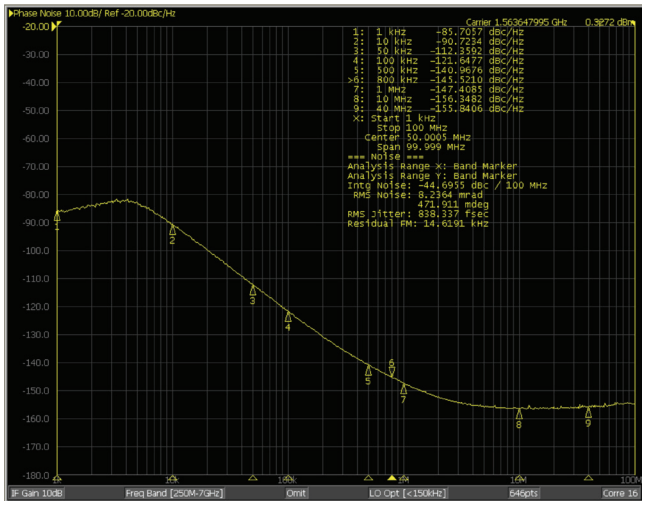


Figure 3. Octave bandwidths are possible with this VCO circuit configuration.

In addition to low phase noise, modern base station receiver designs must support the many modulation schemes currently used in wireless communications networks. In addition to GSM, other modulation schemes include wideband code division multiple access (WCDMA) and long-term evolution (LTE) systems. Receiver designs often consist of a number of different VCOs with moderate phase noise performance levels configured so that they are combined to cover an octave bandwidth within the base station.

Once a number of VCOs have been configured to generate an octave bandwidth for the highest frequencies of operation, lower LO frequencies can be achieved by binary division. This approach was used in the ADRF6612 receiver mixer, where VCO fundamental frequencies span 2.7 GHz to 5.6 GHz and two stages of frequency division realize LO frequencies from 200 GHz to 2700 MHz, by dividing from 1 to 32. For applications that also include MC-GSM, the ADRF6614 receiver mixer includes two additional high performance VCO cores to provide the LO frequencies needed for the 1800 MHz to 1900 MHz GSM bands.

Since modern wireless microcells may not have the benefits of climate controlled environments, components such as these receiver ICs must provide consistent, reliable performance over wide temperature extremes. To achieve specified performance over a wide operating temperature range, the PLLs and VCOs in the ADRF6612 and ADRF6614 ICs employ a number of calibration techniques.

For wide bandwidths with low noise, each VCO core employs an 8-bit capacitive digital-to-analog converter (CDAC) that automatically selects the correct band (1 of 128) for a given LO frequency. Any variations in VCO tank amplitude are carefully monitored by the system and the amplitude is adjusted using an automatic level control (ALC) system for optimum output amplitude. Each IC performs a calibration sequence any time the operating frequency is reprogrammed. This ensures that the selected band centers the tuning voltage for a VCO's tuning varactor diode in the optimum range to maintain the synthesizer in lock over the required operating temperature range.

The four VCO cores in each ADRF6612 and ADRF6614 IC are positioned to ensure that their operating ranges provide suitable overlap for changing environmental conditions and device fabrication tolerances. The cores will generally move frequency in the same direction for environmental and process variations, so there is enough overlap built in for the frequency synthesizer to always achieve locked conditions.

Once the calibration solution is determined, frequency should be maintained indefinitely and the tuning voltage range supports the required hold-in range. In time division duplex (TDD) systems where the base station may change frequencies on a time slot-to-time slot basis, this operating time may be measured in microseconds. In frequency division duplex (FDD) systems, it might be necessary to maintain lock on a single frequency for years.

There is no allowable downtime at any point during the system operation of the ADRF6612 and ADRF6614 ICs. Thus, changes in temperature and component aging effects are covered by the varactor tuning voltage range and frequency tuning sensitivity (kV) of the VCO for potentially a 145°C temperature range. Each IC constantly monitors device temperature and adjusts the VCO bias as required.

The ADRF6612 and ADRF6614 ICs use a unique approach to minimize degradation of receiver sensitivity from spurious signal products. Using the synthesizer's integer mode with a tight loop filter results in low reference spurious products of less than −100 dBc. Minimal spurious signals are critical for modulation schemes, such as MC-GSM. For LTE and other modulation schemes, or where fine frequency steps are required, the synthesizer can be operated in fractional-N division mode. The reference path incorporates a 13-bit divider, and the integer and fractional paths each incorporate 16-bit dividers for flexibility.

For applications where colocated, phase tracked receive channels are required, such as in multiple input, multiple output (MIMO) systems,

multiple ADRF6612 and ADRF6614 ICs can be cascaded in a daisy-chain manner to permit one unit acting as a master synthesizer to supply additional slave receivers through their external LO output and input ports, respectively. In this way, additional LO distribution amplifiers and their associated increases in phase noise can be minimized.

To support both high- and low-side LO injection, each IC's LO chain provides flexible signal processing, as shown in Figure 4. Using integer division ratios of 1 to 32, low-side injection is possible even for the 700 MHz band with a high IF. The LO stages also provide a square-wave drive to the passive mixer cores over the full LO range from 200 MHz to 2700 MHz.[1]

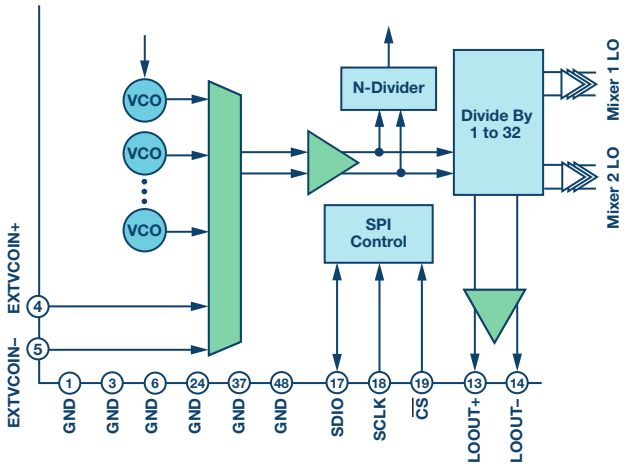


Figure 4. This LO signal chain is used in support of a wireless base station receiver.

Modern wireless base station in-band signals close in frequency to low level input signals so the cellular receiver can act as blocking signals. In such a case, phase noise from the LO amplifier in the vicinity of the blocking signal is mixed into the IF output band directly on top of the desired signal. This increases the noise floor and reduces the signal-to-noise ratio (SNR) of the receiver—sometimes dramatically.

Since the blocking signal may be large (high power), it is important that both the VCO phase noise be extremely low and the LO chain does not degrade the noise floor at the blocker offset. At these very high blocking levels, the receiver noise figure will eventually become dominated by the blocking signal and degrade according to the power level of the blocker.

In discrete implementations of the receive chain, it would be possible to introduce some filtering into the LO path to minimize the phase noise at the blocker offset coming from the VCO and LO distribution amplifiers. However, in an integrated front end, care must be taken to avoid additive phase noise in the LO chain.

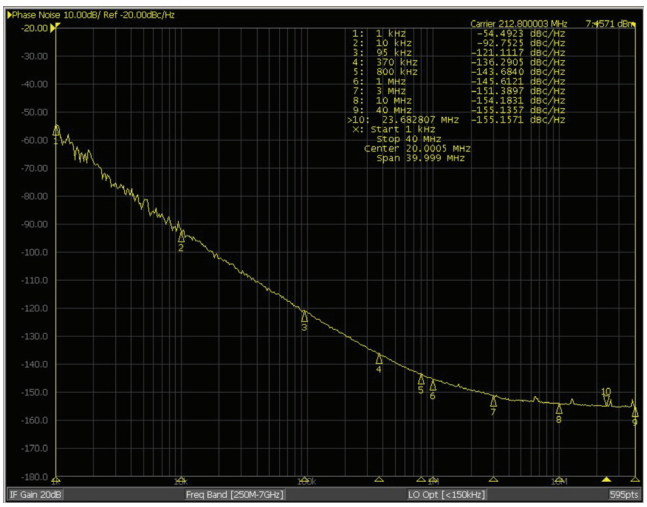
The ADRF6612 and ADRF6614 ICs employ a high gain LO chain and hard limiting amplifiers to drive the LO chain into limiting. As each stage enters hard limiting, the small signal gain of the LO chain that would otherwise increase phase noise is substantially reduced, minimizing noise figure degradation under blocking conditions.

The noise fold over from the blocking signal degrades the output noise spectrum of the receiver, and hence the receiver noise figure, by raising the output noise floor. The ADRF6612 and ADRF6614 receiver ICs are designed to withstand significant blocking signals with minimal degradation of receiver noise figure, displayed in Figure 5. Even with a 10 dBm input blocking level, the receiver's noise figure is only degraded by 3.2 dB at 10 MHz offset from the carrier, even though the conversion gain is compressed by 1 dB at that extreme blocking level.

The high level of integration in these receiver ICs has enabled significant performance improvements and savings in dc power for modern wireless base station designers, as seen in Figure 6. The ICs feature a technique that simultaneously optimizes the RF and IF stages surrounding the on-chip mixer.[2]

This technique, first implemented in the ADRF6612, provides a minimum IIP3 of over 25 dBm over temperature and the full frequency range with low power dissipation, and 29 dBm up to 2 GHz over temperature. The technique also provides optimum receive path noise figure performance with high conversion gain, shown in Figure 7.[3,4]

ADRF6614 Output Noise, Low Level Blocker



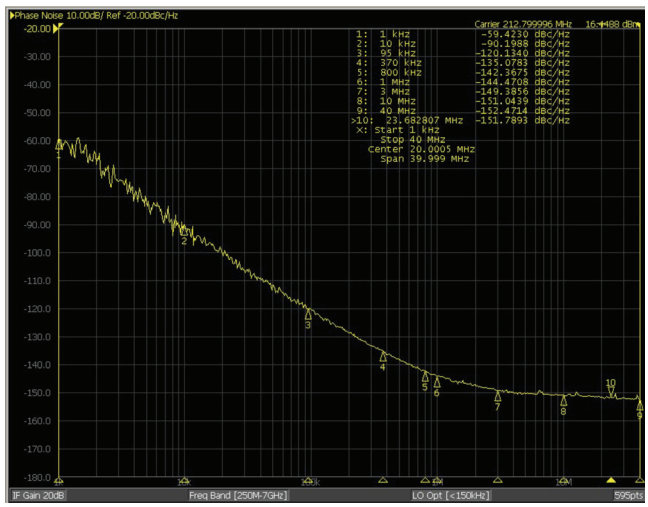
p_{RF} = 0 dBm (Unblocked Case) f_{RF} = 1960 MHz

PN10M = –154.2 dBc/Hz
Output Level = 8.4 dBm (7.4 dB + xfmr Loss, Uncompressed)

Locked Using Internal Synthesis
f_{VCO} = 3494 MHz
f_{LO} = 1747 MHz

f_{RF} = 1960 MHz (Frf Cavity Filtered)

ADRF6614 Output Noise, High Level Blocker



p_{RF} = 10 dBm (Blocker Case)

PN10M = –151.0 dBc/Hz
Output Level = 17.4 dBm (16.4 dBm + xfmr Loss, ~1 dB Compressed)

Locked Using Internal Synthesis
f_{VCO} = 3494 MHz
f_{LO} = 1747 MHz
f_{RF} = 1960 MHz (Frf Cavity Filtered)

Figure 5. The plot compares the output noise spectrum of the ADRF6614 receiver IC with low and high level blocking signals (left and right, respectively).

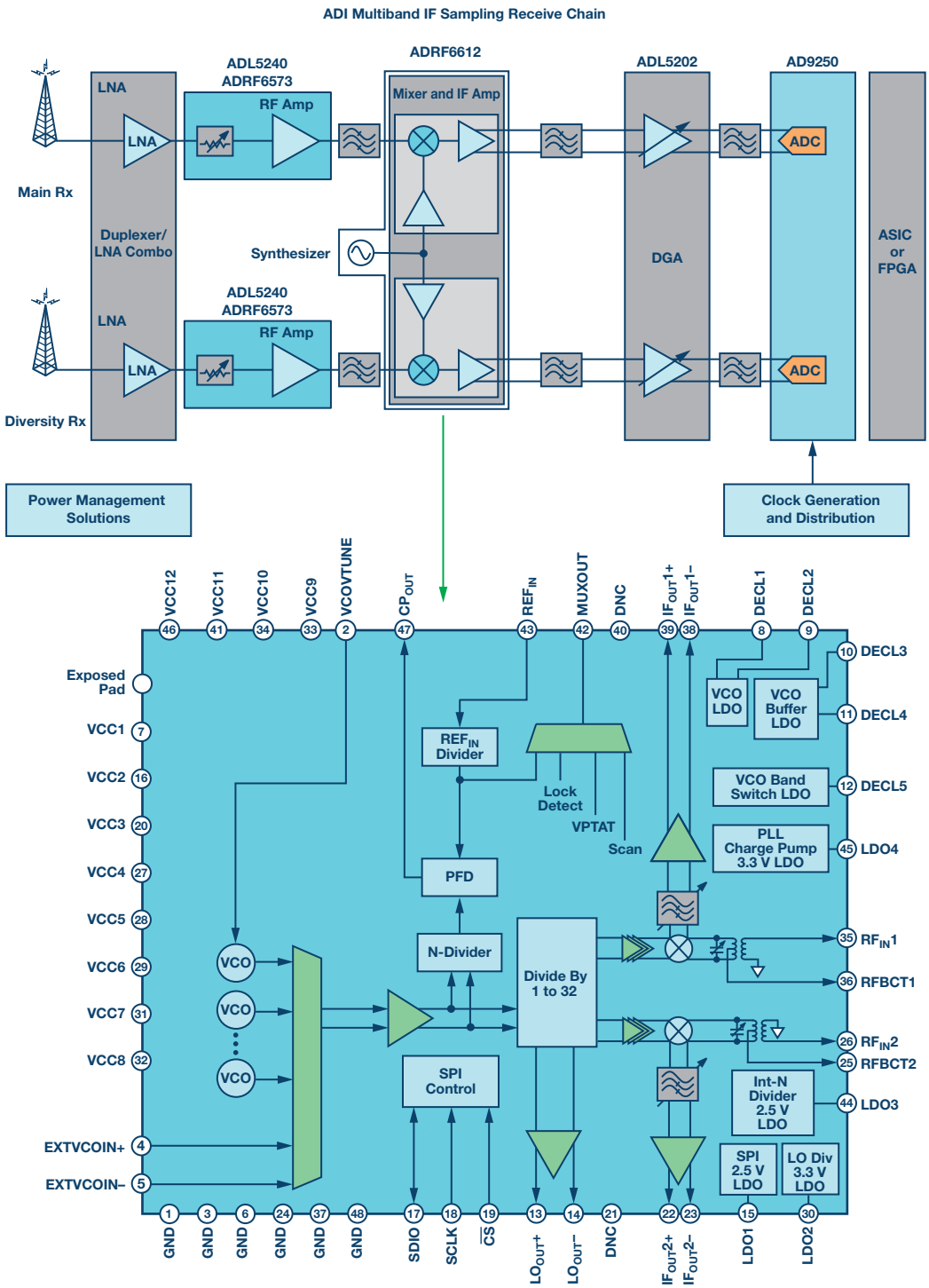


Figure 6. The signal chain shows the components employed in a typical wireless base station receiver.

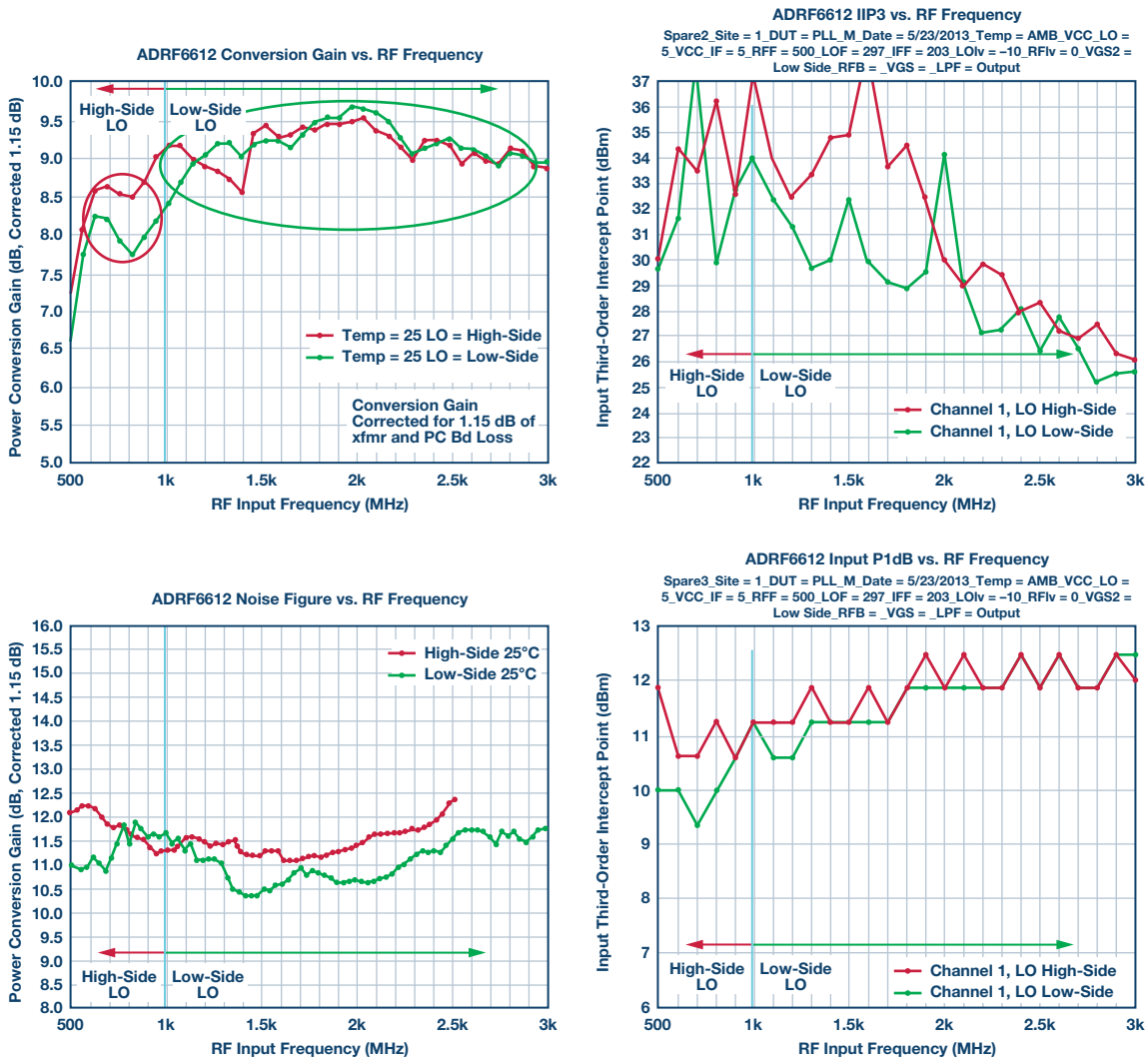


Figure 7. The plots show measured gain, noise figure, and input third-order intercept point (IIP3) for the ADRF6612 receiver IC.

Acknowledgments

With the increased level of integration inherent in complete receiver chains comes a much larger development team. While it isn't possible to list all of the people that contributed to this work, the authors take great pleasure in acknowledging the efforts of the following industry experts: Kurt Fletcher and Dominic Mai spent many hours implementing an excellent layout while maintaining symmetry and avoiding unwanted couplings. Vincent Bu worked to develop the necessary packaging with our vendors. Susan Stevens maintained the excellent working relationship with our external foundry partner. Craig Levy and Rachana Kaza developed the production test capability for these parts. Wendy Dutile, Ed Gorzynski, and Chris Norcross all participated in the extensive prototyping of the test circuitry. Mark Hyslip coordinated the business aspects of successfully bringing this project together. The authors would like to dedicate this work in the memory of our colleague, Edward J. Gorzynski.

References

[1] Marc Goldfarb, Russel Martin, and Ed Balboni. "Novel Topology Supports Wideband Passive Mixers." *Microwaves & RF*, pp. 90, October 2011.

[2] Marc Goldfarb. "Apparatus and Method for a Wideband RF Mixer." Analog Devices, 2012.

[3] ADRF6612 Data Sheet. Analog Devices, Inc., 2016.

[4] ADRF6614 Data Sheet. Analog Devices, Inc., 2016.

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Tom Bosia [*thomas.bosia@analog.com*] joined ADI in 2013 as an RF product engineer. Prior to Analog Devices, he was an RF test engineer at Raytheon, Cree, and Auriga Microwave, accruing over 25 years of experience in microwave semiconductors. He received a B.S.E.E. from UMass Lowell in 2001.

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Marc Goldfarb [*marc.goldfarb@analog.com*] has over 35 years of design experience in analog, RF, and microwave integrated circuits in military, industrial, and consumer applications. He has worked in SiGe/silicon, GaAs, and microwave hybrid integrated circuit technologies, among others. Prior to joining Analog Devices, Marc held engineering roles at Pacific Communications Sciences, Inc. (PCSI), Raytheon, and M/A-COM Microwave Associates. He holds a Master of Engineering degree from Rensselaer Polytechnic Institute in Troy, NY, has 13 patents, and has authored numerous publications for reference and trade journals.

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Ed Balboni [*ed.balboni@analog.com*] has 30 years' experience designing high performance, highly integrated, radio transceiver circuits. His expertise is in microwave, RF, mixed-signal, and analog circuits in SiGe BiCMOS, bipolar, and CMOS technologies for communication products. Ed joined Analog Devices in 2000 and works in the RF IC Design Group as an IC designer and design manager. At ADI he develops high performance RF IC components supporting wireless infrastructure including cellular base stations and point-to-point microwave.

Prior to joining ADI, Ed worked at Draper Laboratory in Cambridge, MA on MEMS inertial sensors and low power communication electronics. Ed graduated from University of Massachusetts Lowell with a B.S.E.E. degree in 1985 and received a M.S.E.E. degree in 1990 from Northeastern University.

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