# New Digital Demodulator and JESD204B Ultrasound Analog Front End Reduces Data Rates and Interface Routing Up to 80%

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## Abstract

A design based on digital demodulator and JESD204B interface for multiple channel ultrasound receive systems is introduced. The design reduces the data rates and simplifies board routing between the analog front end (AFE) and digital processing circuits up to 80%. In addition, the ultrasound system can achieve more targets, such as utilization of cheaper and less computationally efficient field programmable gate arrays (FPGA), a software-based beamformer, and higher order multiline processing for real-time 4D and advanced imaging modes.

## Introduction

As medical ultrasounds are widely used in the medical diagnostics field, doctors have ever increasing demands for higher image quality of the ultrasound image systems, and one of the key techniques for image quality improvement is to enhance the signal-to-noise ratio of the receiving channel. As the number of receiving channels in a system doubles, the signal-to-noise ratio should improve by 3 dB in theory. Therefore, increasing the number of system channels has become the easiest and most effective method to strengthen the signal-to-noise ratio. At present, 128-channel has successfully become the mainstream configuration for middle to high level medical ultrasound equipment, and 192 or more channels will become the next trend for premium systems. With the increase in the number of channels, the data rates between the analog front-end and back-end digital processing as well as the physical connections sharply increases. They also cause the number of digital circuit device interfaces, the processing power, the costs, the design complexity of the entire receiver circuit, and the corresponding power consumption to increase as well. At present, the ultrasound system uses the radio frequency (RF) beamforming. The output data rate is entirely determined based on the resolution, sampling rate, and channel numbers of the analog-to-digital converter (ADC). Meanwhile, the analog front end (AFE) usually uses low voltage differential signaling (LVDS) output interfaces. An octal AFE requires eight pairs of LVDS data wires plus a pair of data clock and frame clock each. For a system with over 128 channels, there are significant amounts of data and physical connections.

In this article, an ultrasound receiving channel design solution based on an octal AFE with digital demodulator and JESD204B interface is introduced, which effectively resolves the design difficulties caused by the large data rates and complex physical connections of the system as mentioned above.

## System Architecture

An ultrasound system is composed of a probe (transducer), transmitting circuit, receiving circuit, back-end digital processing circuit, control circuit, display module, etc. Figure 1 is the block diagram of a 128-channel ultrasound system transmit/receive path with JESD204B interface. The digital processing module usually comprises a field programmable gate array (FPGA), which generates the corresponding waveforms according to the current configuration and control parameters of the system. The transmit circuit's driver and the high voltage circuit then generate a high voltage to excite the ultrasound transducers. The ultrasound transducer is usually made of piezoelectric ceramic transducer (PZT). It converts voltage signal into ultrasound waves that enters into the human body while receiving the echoes produced by the tissues. Then the echoes are converted into a voltage signal and transmitted to a transmitting/receiving (T/R) switching circuit. The primary objective of the T/R switch circuit is to prevent the high voltage transmit signal from damaging the low voltage receive analog front end. The analog voltage signal after signal conditioning, gaining, and filtering is passed to the integrated ADC of the AFE and then converted into digital data, which is then transmitted through a JESD204B interface to the back-end digital parts for the corresponding processing to eventually create the ultrasound image. The receiving channel is composed of a 128-channel T/R switching circuit, 16-octal-channel ultrasound AFE devices with digital demodulator and JESD204B interface, and an FPGA with JESD204B interface.

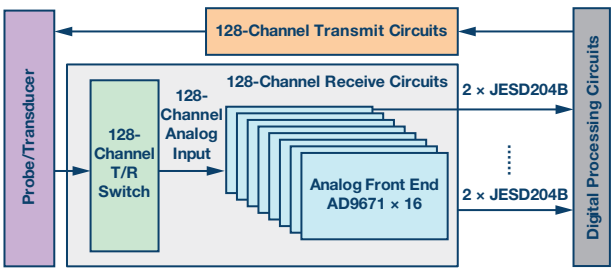


*Figure 1. 128-channel ultrasound system block diagram.*

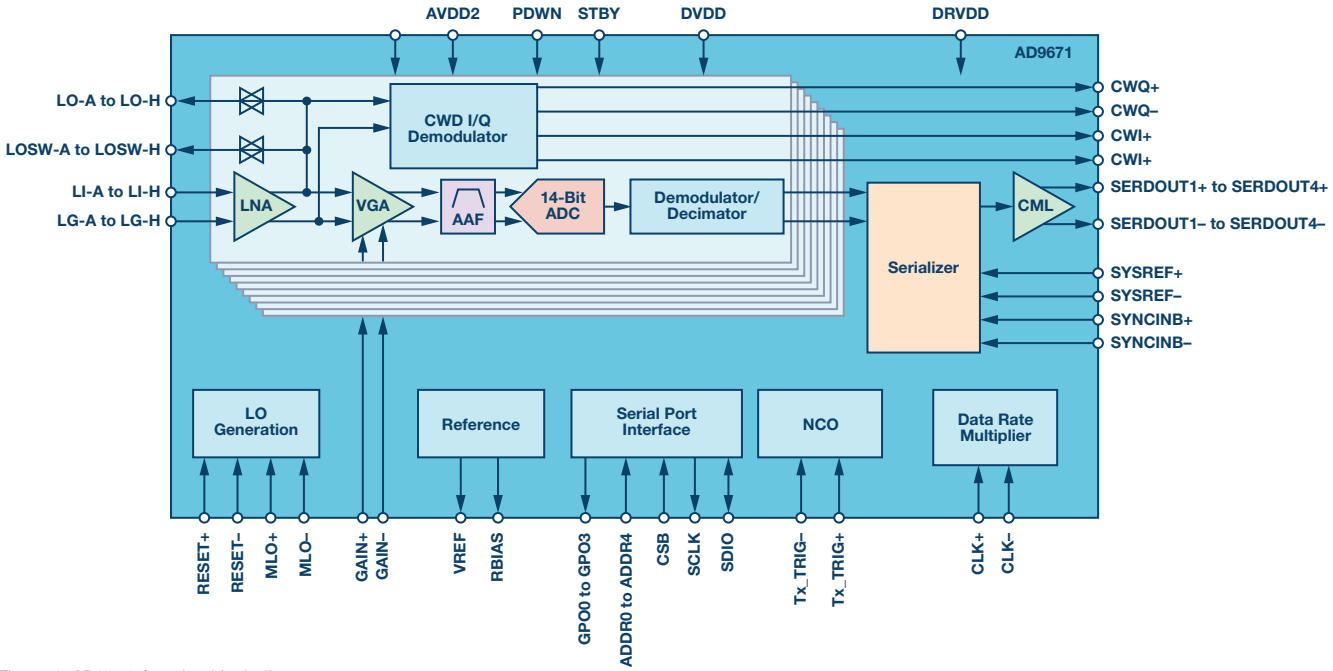


*Figure 2. AD9671 function block diagram.*

## AD9671: Octal Ultrasound AFE with Digital Demodulator and JESD204B Interface

AD9671, the octal ultrasound AFE with digital demodulator and JESD204B interface from Analog Devices (ADI), is selected to be used in this ultrasound system receiving circuit. It contains eight channels of a variable gain amplifier (VGA) with a low noise amplifier (LNA), a continuous wave (CW) harmonic rejection I/Q demodulator with programmable phase rotation, an antialiasing filter (AAF), a 14-bit ADC, a digital demodulator and decimator for data processing and bandwidth reduction, and JESD204B interfaces. Figure 2 is a functional block diagram of AD9671.

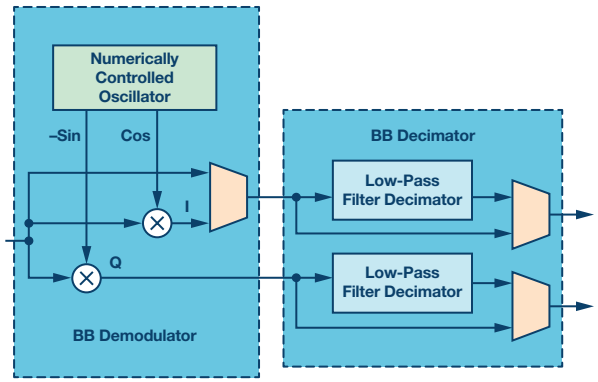


*Figure 3. Digital demodulator block diagram.*

## Digital Demodulator

The digital demodulator is composed of a baseband demodulator and baseband decimator. The demodulator downconverts the RF signal to a baseband quadrature signal. The excess oversampling is reduced by the decimator. Figure 3 is a block diagram of a digital demodulator.

## JESD204B Interface

The AD9671 digital output complies with the JEDEC standard JESD204B, serial interface for data converters. The AD9671 supports single, dual, or quad lane interfaces. It can connect to an FPGA with a maximum data output rate of 5.0 Gbps.

## System Design and Application

The receiving circuit design of the AD9671 multichannel ultrasound system is introduced in this section and the benefits of using digital demodulators and the JESD204B interfaces for the system are analyzed further.

## Receive Circuit Design

A 32-channel receive circuit module schematic top diagram is shown in Figure 4, which can be designed to verify the feasibility of the system based on the AD9671. With four such modules, a 128-channel receive circuit of an ultrasound system can be configured. This module can be used to perform data capture and processing as well as achieve ultrasonic signal processing and image generation by connecting to an FPGA through a dedicated FMC connector.

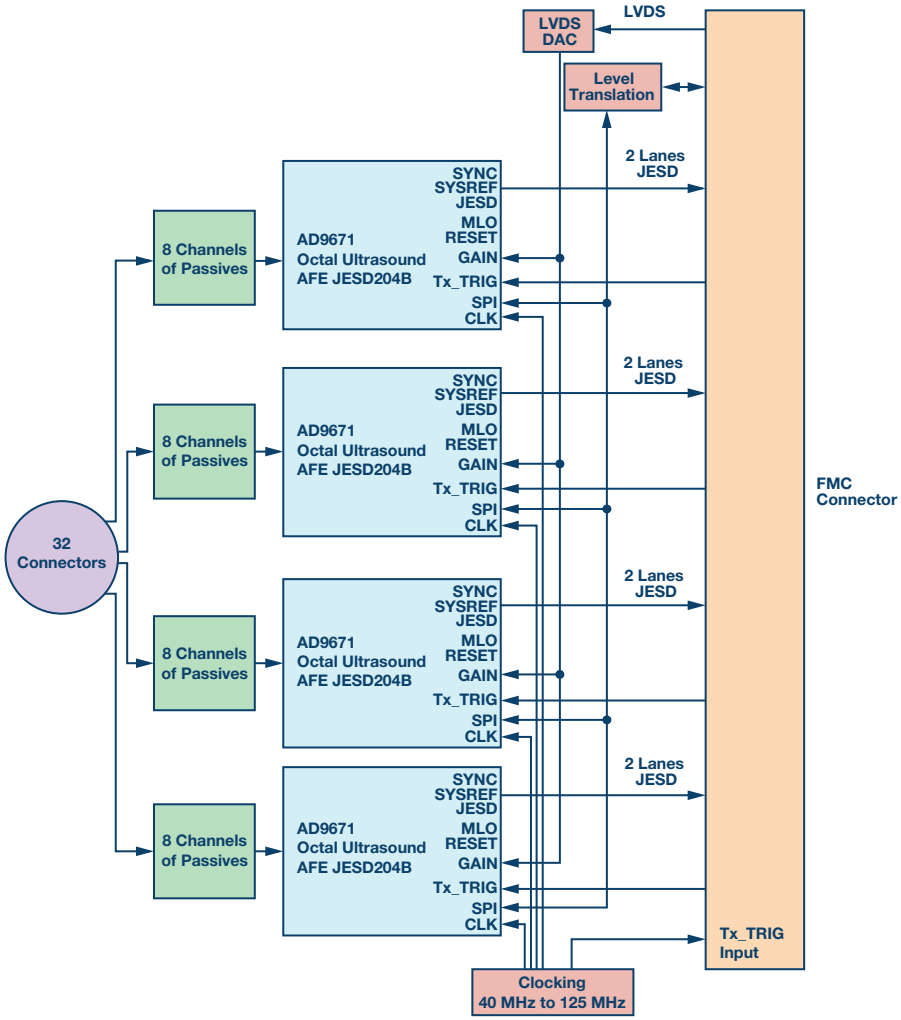


*Figure 4. Top level schematic diagram of the receiving circuit.*

## Digital Demodulator Application Analysis

For a 128-channel ultrasound system, if a 14-bit ADC is utilized with a sampling rate of 40 MSPS, and an RF beamforming algorithm is used, then the data rates between the ADC output and the beamforming FPGA is 14 × 40 × 128 = 71.68 Gbps.

The benefits of using a digital demodulator are analyzed below.

The baseband demodulator of the RF signal performs quadrature demodulation. It can be achieved by multiplying the digitized RF signal outputted by the ADC with a complex sinusoidal signal ($e^{-j2\pi f_d t}$), where $f_d$ is the demodulation frequency that can be close to the center frequency of the ultrasound transducer to downconvert the center frequency to around 0 Hz. The output signal is a complex signal that is represented by its I (in phase) and Q (quadrature phase). The center frequency of the probe and all of the interested frequency band signals are downshifted to approximately 0 Hz, the unwanted frequency components are filtered out with the filters and decimator to retain the band information that is useful to generate the ultrasound images.

For a probe transducer with a center frequency of 3.5 MHz, after baseband demodulation and decimation, with 16-bit format I and Q data output, the data rate is now 2 (I&Q) × 16 bits × 3.5 MHz × 128 channels = 14.336 Gbps. Compared to the original 71.68 Gbps, the data rate is decreased by 80%, even with the I and the Q channels outputting simultaneously.

## JESD204B Interface Application Analysis

In terms of current AFE and ADC in multichannel ultrasound system applications, LVDS has replaced the parallel output interface. However, for the 128-channel or higher ultrasound system, the large amount of LVDS wire connections for the ADC output is still a headache for the design engineers. With LVDS, there are 10 pairs of wires for one octal AFE in a current ultrasound system. For a 128-channel ultrasound system, 128/8 × 10 = 160 pairs of LVDS data, and clock wires are required to be connected to the FPGA.

The benefits of using the JESD204B interface are analyzed below.

As the JESD204B uses a 16-bit digital output format and uses 8B/10B encoding, the output data rate for an octal AFE with 14-bit resolution, 40 MSPS ADC the sampling rate is 20 × 40 × 8 = 6.4 Gbps. The maximum data rate of each lane of the AD9671 JESD204B interface is 5.0 Gbps, so only two pairs of data lanes are needed to implement an 8-channel AFE data output. So for a 128-channel ultrasound system, only 128/8 × 2 = 32 pairs of output data lanes are required as compared to 160 pairs of the LVDS wires; 80% of the physical interface routing is eliminated.

## Conclusion

A multichannel ultrasound system design based on AD9671, an octal AFE with digital demodulator and JESD204B interface, is introduced in this article. The application advantages and benefits of using such an AFE with digital demodulator and JESD204B interface in an ultrasound system are effectively analyzed respectively. Comparing with most of current RF beamforming and LVDS interface-based designs, both the data rate and interface routing between the analog front end and digital processing parts are reduced 80%. If the two methods are combined together in an analysis, the physical connections would be reduced even further. Therefore, the system design presented in this article can effectively simplify the circuit design and software processing complexity by reducing the required board area for data interface routing, the computational complexity requirement, as well as the system design costs.

## References


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Hugh Yu earned his master's of electronic and information engineering in 2001 from the Nanjing University of Posts and Telecommunications, China. He worked as an ultrasound hardware engineer at GE Medical System, China, between 2002 and 2005, and worked as a research scientist at Siemens Corporate Technology China between 2005 and 2010. He is currently a healthcare systems application engineer at Analog Devices, Shanghai, China.

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