Designing Power Supplies for High Speed ADC

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IDEA IN BRIEF

Designing clean power supplies for high speed ADCs can be challenging with so many power options that are available to the designer today. This is especially important when utilizing efficient switching power supplies rather than traditional LDOs. In addition, most ADCs do not adequately specify high frequency power supply rejection, a key factor when selecting the proper supply.

This technical article describes techniques to measure a converter's AC power supply rejection, thereby establishing a baseline for the converter's power supply noise sensitivity. A simple noise analysis of an actual power supply is given to show the user how to apply these numbers in a design to verify the power supply is adequate for the converter(s) chosen. In summary, some simple guidelines are described in order to give the user some guidance in designing power supplies for high speed converters.

Many of today's applications require high speed sampling analog-to-digital converters (ADC) with resolutions of 12 bits or more, as the higher resolution allows users to develop more accurate system measurements. Unfortunately, higher resolution also implies that the system will be more sensitive to noise. Every time the system resolution increases by one bit, for example, 12 bits to 13 bits, the system sensitivity goes up by a factor of two. Thus, when designing with ADCs, it is crucial that designers consider the noise contributions from an often forgotten source—the system power supply. ADC are sensitive devices and each input, that is, analog, clock, and power should be treated equally to achieve the best performance as specified in the data sheet. Noise sources are abundant and can come in many forms and be emitted or radiated affecting the performance.

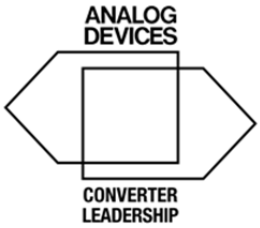

Figure 1.

All the buzz and hype in today's electronic world is that new cost-down designs are "going green". Keeping power low requires less thermal management, keeping power efficiency maximized and batteries happy when it comes to portable applications. However, most ADC data sheets suggest that linear power supplies be used because their noise is lower than that of switching type supplies and in some cases that may be entirely true. However, new advances in technology have proven that switching power supplies could possibly be used in communications and medical applications (see the "How to Test Power Supply Rejection Ratio (PSRR) in an ADC" article in the References section).

This article describes different test measurement methods that are critical to understanding power supply design for a high speed ADC. Commonly called power supply rejection ratio (PSRR) and power supply modulation ratio (PSMR), both of these tests are useful in determining just how sensitive the converter is too noisy effects on the power supply rails as well as to determine just how quiet the power supply rail must be in order to achieve the expected performance of the ADC itself.

LOOKING CLOSER AT ANALOG POWER PINS

Typically, a power pin is not thought of as an input. But it is. It can be just as sensitive to noise and distortion as clock and analog input pins are known. Even though the signal that comes onto the power pin is dc in nature and typically doesn't fluctuate in a repetitive manor it still has some finite amount of noise and distortion riding on the dc bias. This noise can be generated intrinsically or extrinsically which will affect the converter's performance.

Think of the classic example when there is a noise or jitter present on the converter's sampling clock signal. Jitter on the sample clock can present itself as both close-in noise and/or it can be in the form of broadband noise as well. Both will depend on the oscillator and system clock circuitry used. Even with an ideal analog input signal presented to an ideal ADC the clock impurities will be resolved on the output spectrum as shown in Figure 2.

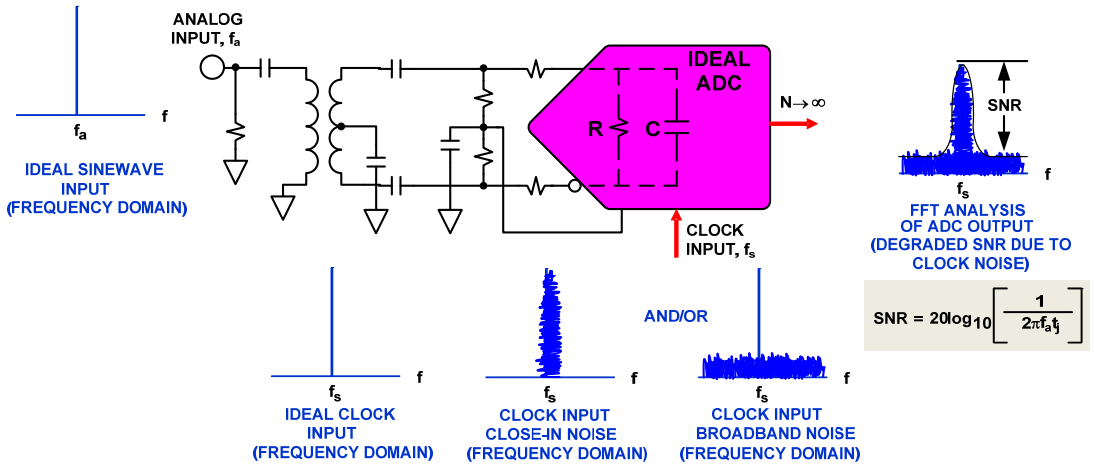

Figure 2. Effect of Sampling Clock Noise on Ideal Digitized Sine Wave

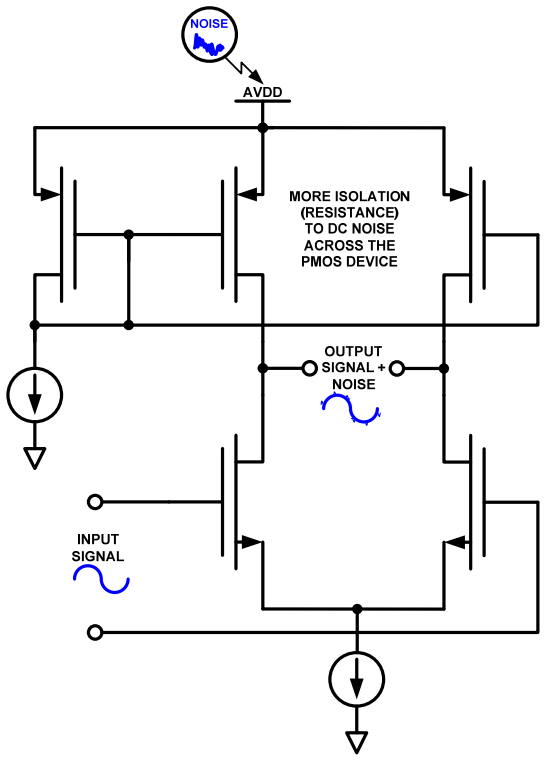

Figure 3. Different Circuit Topologies—Implementation A

The corollary to this figure is the power pin. Substitute the sampling clock input pin in Figure 2 with an analog power pin (AVDD). The same mechanism applies here too, that any noise, either close-in or broadband, will show itself on the output spectrum in this convolved manor. However, there is a difference; a power pin can be thought of as a broadband input pin with a 40 dB to 60 dB attenuator (depending on the process and circuit topology). In general MOS circuit construction, any source or drain pin is isolated (resistive) in nature from the signal path, thus providing a significant amount of attenuation vs. the gate pin, or signal path. There is some assumption that the design employs the right type of circuit construction to maximize isolation. Some types, such as common-source, may not be well suited when supply noise is evident because the supply is biased through a resistive element, which then connects to the output stage, see Figure 3 and Figure 4. Any modulation, noise, etc on the AVDD pin could show through more easily and affect the local and/or adjacent circuitry. This is why there is always grounds for understanding and seeking PSRR data on converters.

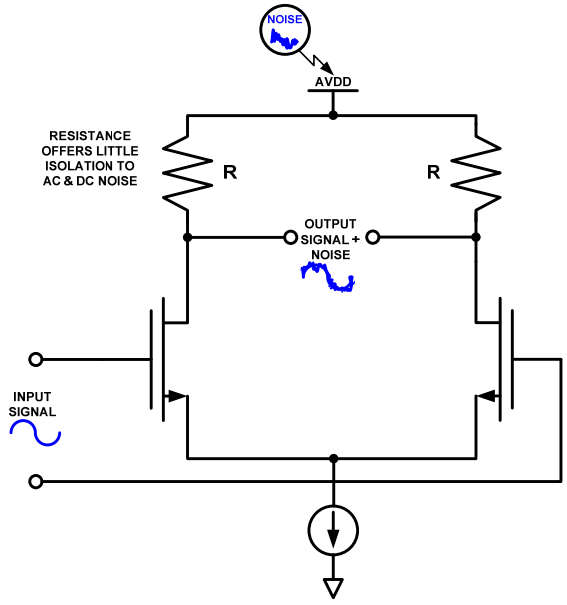

Figure 4. Different Circuit Topologies—Implementation B

As the different implementations suggest there are different frequency characteristics due to parasitic R, C, and mismatch. Remember processes are getting smaller too, with smaller process geometries the more bandwidth and speed available. Taking this into account, this means lower supplies and smaller thresholds. So why not treat a power supply node as a high bandwidth input, similar to a sampling clock or analog input pin.

POWER SUPPLY REJECTION DEFINED

There are some terms that govern how well a ADC performs when there is noise on the power supply rail. They are PSRR-dc, PSRR-ac, and PSMR. PSRR-dc is the ratio of the change in power supply voltage to the resulting change in the ADC's gain or offset error. This can be expressed in fractions of a least significant bit (LSB), a percentage, or logarithmically, in dB (PSR = 20 × log10 (PSRR)), and is usually specified at dc.

However, this method only reveals how one specified parameter of the ADC may change with a change in power-supply voltage, and therefore cannot prove the robustness of the converter. A better method is to test supply rejection by riding an ac signal on top of the dc power supply, PSRR-ac, thus actively coupling the signal (noise source) through the converter's circuitry. This method essentially exercises the attenuation of the converter, reviling itself as a spur (noise) that rises above the noise floor of the converter at some given amplitude. This presents itself as where the converter breaks given a certain amount of injected noise and amplitude. This also gives the designer insight as to how much power supply noise will affect the signal or add to it. PSMR, affects the converter in a different way, it tells the designer just how sensitive the converter is to power noise effects as it modulates with analog input signal applied. The effect is shown as modulation around the IF frequency applied to the converter and can wreak havoc in or around the carrier sidebands if the supply is not carefully designed.

In summary, power supply noise should be tested and treated just like any other input to the converter. It is imperative that the user understands the system supply's noise. If not, power supply noise will increase the converter noise floor and limit the dynamic range of the entire system.

POWER SUPPLY TESTS

Figure 6 shows a PSRR measurement of an ADC on a system board. Each supply is measured individually to better gain perspective on the ADC's dynamic behavior when an ac signal rides on the power supply under test. Start with a high capacitor value such as a 100 µF nonpolarized electrolytic. For the inductor, use a 1 mH to act as the ac blocker to the dc power supply. This is commonly called a bias-T and can be purchased in a packaged-connectorized housing.

Using the oscilloscope measure the amplitude of the ac signal with a scope probe applied to the point at which the power enters the ADC's supply pin under measurement. To make things simple define the amount of ac signal riding on the supply as a value related to the converter's input full-scale. For example, if the ADC's full-scale is 2 V p-p, then use 200 mV p-p or −20 dB. Next, with the input of the converter grounded (no analog signal applied), look for an error spur at the test frequency coming out of the noise floor/FFT spectrum, as shown in Figure 5. To calculate PSRR, simply subtract −20 dB from the error spur value seen on the FFT spectrum. For example, if the error spur shows up at −80 dB from the noise floor, then the PSRR is −80 dB − −20 dB or −60 dB, (PSRR = error spur (dB) − oscilloscope measurement (dB)). The value of −60 dB may not seem like much, but let's look at that in terms of a voltage, it equates to 1 mV/V (or $10^{-60/20}$), which is not uncommon for a PSRR specification in any converter data sheet.

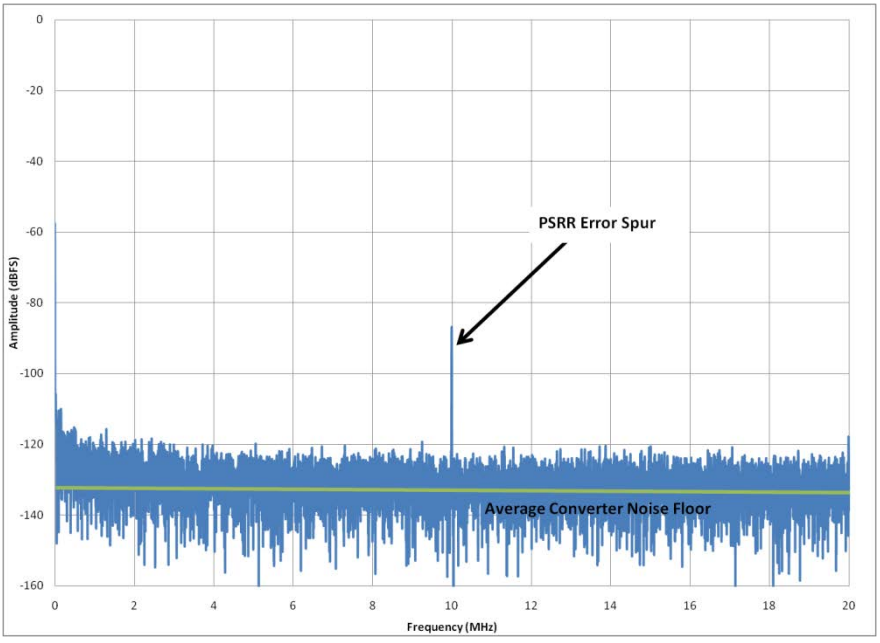

Figure 5. Example of PSRR—FFT Spectrum

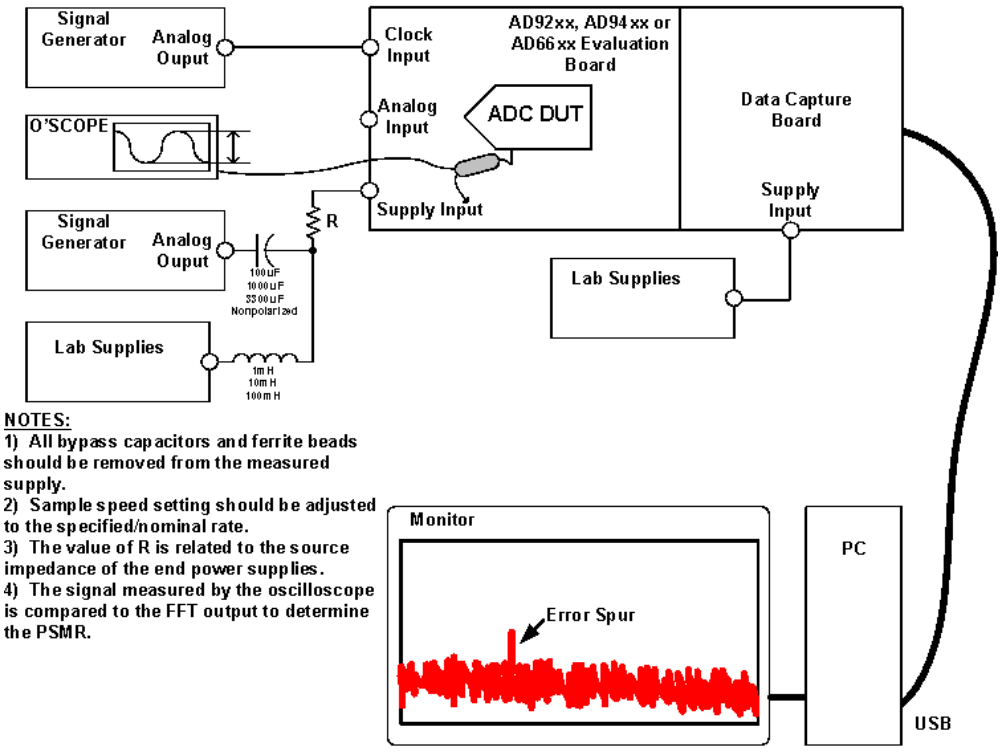

Figure 6. Typical PSRR Testing Setup

The next step is to vary the frequency and amplitude of the ac signal in order to characterize the ADC's PSRR in your system board. Most data sheet numbers are typical, and might only specify worst-case operating conditions or worst performing supply. For example, the 5 V analog power supply might be the worst relative to the other supplies. Make sure all the supplies are specified or ask the factory for this data if not specified completely. This will allow the designer to place the proper design constraints to each supply.

Keep in mind there is a disadvantage of testing PSRR/PSMR when using an LC arrangement. When sweeping the frequency band of interest, the signal level required at the output of the waveform generator to achieve the desired input level at the ADC supply pin may need to be very high. This is because the LC arrangement will form a notch filter at some frequency depending on the values chosen. This greatly increases ground currents at the notch, which can get into the analog inputs. To get around this, simply swap in new LC values when testing at the frequencies that are causing measurement difficulty. It should also be noted here that losses across the LC network are caused at dc as well. Remember to measure the dc supply at the supply pin of the ADC to compensate for that loss. For example, the 5 V supply may only read 4.8 V on your system board after the LC network. Simply move the power supply voltage up to compensate for the loss.

PSMR is measured essentially the same way as PSRR. However, when measuring PSMR an analog input frequency is applied to the test setup, this is shown in Figure 7.

The other difference is the modulation or error signal applied only at low frequency in order to see the mixing effects of this signal with the analog input frequency applied to the converter. It is typical to use 1 kHz to 100 kHz frequencies for this test. The amplitude of this error signal can be relatively constant as long as the error signal, and the mixing products, can be seen around the fundamental. However, it may be worthwhile to change the amplitude of the modulated error signal applied in order to check to make sure this value is constant. To acquire the final result, the difference between the amplitude of the highest (worst) modulation spur relative to the fundamental will determine the PSMR specification. An example of a measured PSMR FFT spectrum is shown in Figure 8.

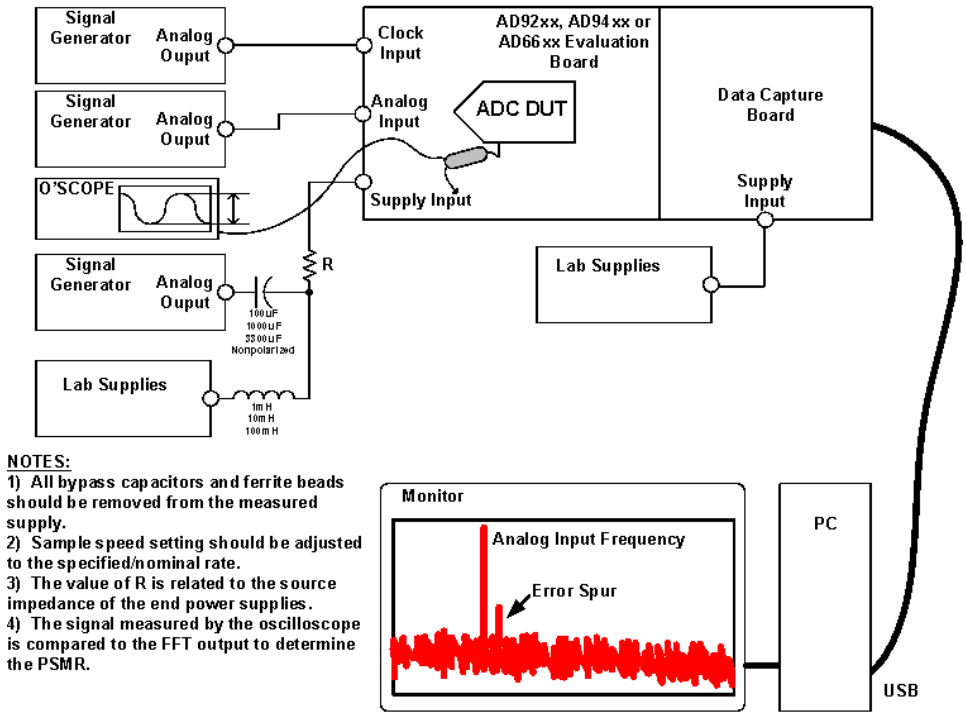

Figure 7. Typical PSMR Testing Setup

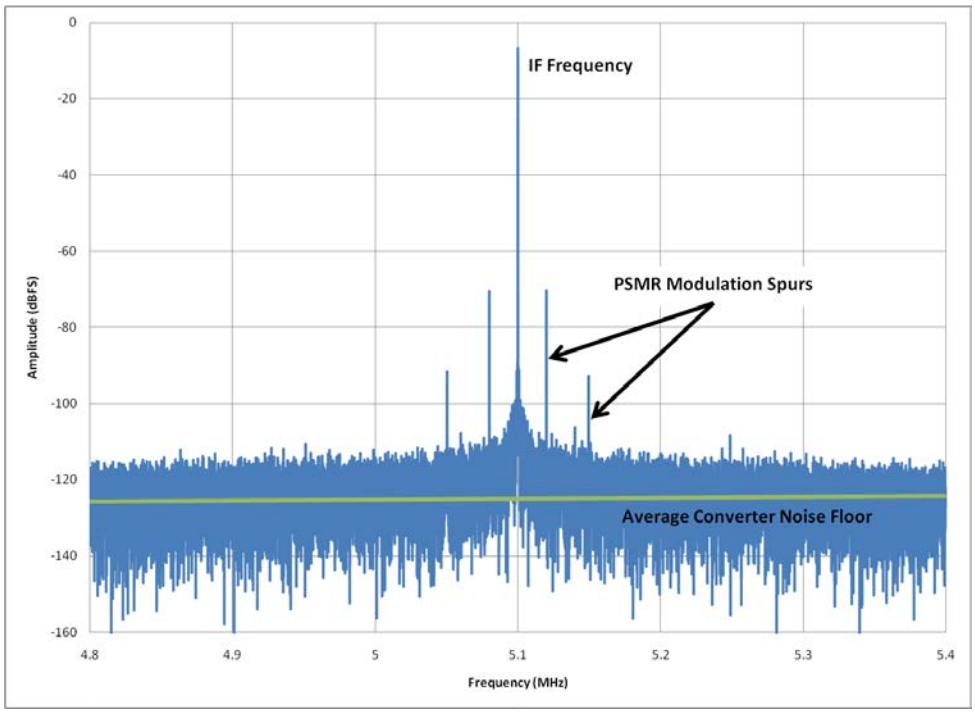

Figure 8. Example of PSMR—Partial FFT Spectrum

POWER SUPPLY NOISE ANALYSIS

What is important to the converter, and ultimately the system, is that noise on any given input does not affect the performance. Now that PSRR and PSMR have been defined and the significances understood, an example will be described in order to understand how to apply the measured numbers.

The following example shows what to look for and how to design the proper way when it comes to understanding the power supply's noise meeting the system design needs.

Begin by choosing a converter and then choose a regulator, LDO, switcher, etc. Not just any regulator will do. From the data sheet, check the regulator's noise and ripple specifica-

tions, as well as its switching frequency, if using a switcher. A typical regulator might have 10 µV rms noise over a 100 kHz bandwidth. Assuming the noise is white, this is equivalent to a noise density of 31.6 nV rms/√Hz over the band of interest.

Next, check the converter's power supply rejection specification to get an understanding of where the converter's performance will degrade due to noise on the supply. 60 dB (1 mV/V) is typical for most high speed converters over the first Nyquist zone, $f_S/2$. If it is not given, either measure it as described previously or ask the factory contact.

Using a 16-bit ADC with 2 V p-p full-scale input range, 78 dB SNR, and 125 MSPS sampling rate, the noise floor is 11.26 nV rms. The noise from any source must be kept below this to prevent it from being seen by the converter. In the first Nyquist zone, the converter noise will be 89.02 µV rms (11.26 nV rms/√Hz) × √(125 MHz/2). Although the regulator's noise (31.6 nV/√Hz) is more than twice that of the converter, remember to account for the converter's 60 dB PSRR, which will suppress the switcher's noise to 31.6 pV/√Hz (31.6 nV/√Hz × 1 mV/V). This noise is much smaller than the converter's noise floor, so the regulator's noise will not degrade the converter's performance.

Supply filtering, grounding, and layout are important too. Adding 0.1 µF capacitors to the ADC power supply pins will reduce the noise even lower than that calculated previously. Keep in mind that some supply pins draw more current or are more sensitive than others. So use decoupling sparingly but be mindful that an extra decoupling capacitor may be needed on some supply pins. Adding a simple LC filter on the power supply output may also help the reduction of noise as well. However, when using a switcher, a cascaded filter will suppress the noise even more. Remember that a approximately 20 dB/decade is gained for each additional stage.

One final point that should be made about the analysis is that this is for a single converter only. If there are multiple converters or channels involved in a system, things change. For instance, ultrasound employs many ADC channels that are summing digitally to increased dynamic range. What this essentially does is push the noise floor of the converter/system down by 3 dB each time the channel count is doubled. For instance, using the previous example, the noise floor of the converter will be half (−3 dB) if two converters are used and −6 dB if four converters are used. This is true because each converter can be treated as an uncorrelated noise source. Uncorrelated noise sources can be RSS'ed or root sum squared because these noise sources are independent and have no relationship between each other instantaneously. In the end, this quickly puts a heavier design constraint on the power supply as the number of channels is increased and the noise floor of the system is reduced and becomes more sensitive.

CONCLUSION

There is no possible way to ensure that all supply noise is eliminated in your application. No system will be totally immune to unwanted power supply interaction. Therefore, as a user of ADCs, the designer must be proactive during the power supply design and layout stage. Here are some useful tips in maximizing PC board noise immunity to supply changes:

- Decouple all power supply rails and bus voltages that come onto the system board.
- Remember that approximately 20 dB/decade is gained for each additional filtering stage.
- Decouple again if supply leads are long and are feeding a particular IC, part, and/or area.
- Decouple for both high and low frequencies.
- Series ferrite beads are commonly used at the power entry point just before the decoupling capacitor to ground. This should be done for each individual supply voltage coming in on the system board whether it be from an LDO or switcher regulator.
- For added capacitance, use tightly stacked power and ground planes (≤4 mil spacing) this adds inherent high-frequency decoupling to the PCB design.
- Like any good board layout, keep supplies away from sensitive analog circuitry such as the front-end stage of the ADC and clocking circuits.
- Good circuit partitioning is key and some components maybe located on the opposite side of the PCB for added isolation.
- Pay attention to ground return paths, particularly on the digital side, so that digital transients don't find their way back to the analog section of the board. Split ground planes may also be useful in some cases.
- Keep analog and digital referenced components over their respective plane. This common practice ensures added isolation to noise and coupling interactions.
- Follow the IC manufacture recommendations; if they are not directly stated in the application note or data sheet, then study the evaluation board. These are great vehicles to start from.

This technical article is intended to give a clear view of power supply sensitivities as they relate to high speed converters and why it is so important to the user's system dynamics. One should appreciate the layout techniques and hardware required to achieve data sheet specifications of an ADC on the system board.

ABOUT THE AUTHOR

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