# I<sup>2</sup>C-Cabling

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An inter-integrated circuit (I<sup>2</sup>C) bus uses two lines, serial data (SDA) and serial clock (SCL), to transfer information between devices connected to the bus. I<sup>2</sup>C devices have open-drain outputs. When an I<sup>2</sup>C device drives a low, the output of the devices pulls the bus to ground. When an I<sup>2</sup>C device switches high, the output of the device goes into a high-Z state where the bus is pulled up to V<sub>DD</sub> by a pull-up resistor connected between the bus and V<sub>DD</sub>. The pull-up resistors along with the capacitance of the cabling or bus creates a charging RC time constant. If using off board cabling or very long buses, the total bus capacitance increases, which increases the rise time of the signal and reduces maximum operating frequency. The total bus capacitance also increases with the number of devices connected to the bus. Figure 1 illustrates the connections of two basic I<sup>2</sup>C devices to an I<sup>2</sup>C bus.



Figure 1. Two basic I<sup>2</sup>C devices connected to an I<sup>2</sup>C bus.

The I<sup>2</sup>C bus specifications restrict the rise time of a signal for different operating frequencies. The fast-mode plus (1 MHz maximum operating frequency) specification declares a maximum rise time for a data or clock signal to be 120 ns. If 1 MHz operating frequency is not necessary, fast mode (400 kHz maximum operating frequency) can be used, which permits a

rise time up to 300 ns. With a fixed value of the pull-up resistor ( $R_p$ ), a linear relationship between rise time ( $t_R$ ) and total bus capacitance ( $C_B$ ) is described by Equation 1. In this case, rise time ( $t_R$ ) is the time it takes a signal to rise from  $0.3 \times V_{DD}$  to  $0.7 \times V_{DD}$ . This equation is derived by solving the voltage of a charging capacitor for  $V_c = 0.3 \times V_{DD}$  and  $V_c = 0.7 \times V_{DD}$ .

$$C_{B(MAX)} = rac{t_R}{R_P imes 0.8473}$$

Equation 1.

Using the data sheet recommended pull-up resistor values for 5 V operating conditions for side one and side two of an I<sup>2</sup>C compliant hot swappable digital isolator (ADUM1250), we can calculate that the maximum cable capacitance for side one is 88 pF and for side two is 780 pF. These are theoretical maximum capacitance values; the suggested load capacitance values in the ADUM1250 data sheet are 40 pF for side one and 400 pF for side two. The data sheet values account for design margin, ESD protection, and 400 pF is a standard for an I<sup>2</sup>C bus. The primary reason for the different load capacitance values of each side of the ADUM1250 is due to their drive strengths. The higher drive strength of side two (30 mA) allows for a lower pull-up resistor value than side one's 3 mA drive strength permits.

Four-way ribbon cable can be used to extend an I<sup>2</sup>C bus. Normally, this type of ribbon cable is approximately 50 pF per meter. For a cabling application, an ADUM1250 could connect one section of the I<sup>2</sup>C bus with 40 pF of total bus capacitance to side one. Side two could connect a four way ribbon cable (up to 8 meters in length) that transfers isolated data to additional I<sup>2</sup>C devices connected to the bus. If a distance larger than 8 meters is necessary, or if there is more than 40 pF of total capacitance connected to side one, the maximum operating frequency can be reduced to allow a longer rise time and a larger bus capacitance.

## References

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The I<sup>2</sup>C-Bus and How to Use It. Phillips Semiconductor, 1995. http://www.PC-bus.org/fileadmin/ftp/I<sup>2</sup>C bus specification 1995.pdf

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UM10204. I<sup>2</sup>C-bus specification and user manual. NXP Semiconductors, 2012. http://www.nxp.com/documents/other/UM10204\_v5.pdf

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