

Michael Clifford Applications Engineer, Analog Devices, Inc.

# FUNDAMENTAL PRINCIPLES **BEHIND THE SIGMA-DELTA ADC TOPOLOGY: PART 1**



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Figure 1. Pillar concepts of the  $\Sigma$ - $\Delta$  ADC.

Oversampling

As the  $\Sigma$ - $\Delta$  modulator is an oversampled architecture, let's start with the sampling theory and the scenario of Nyquist and oversampled ADC operation.

Noise Shaping

**Digital Filtering** 

Decimation

Figure 2 illustrates the comparison between the Nyquist operation of an ADC with the oversampled case and finally with the  $\Sigma$ - $\Delta$  modulated (also oversampled) case.

Figure 2a represents the quantization noise of an ADC when running in a straight Nyquist operation. In this case, the quantization noise is determined by the LSB size of the ADC. Fs is the sampling rate of the ADC and  $F_s/2$  is the Nyquist frequency. Figure 2b shows the same converter, except now it is used in an oversampled context so a faster sampling rate is employed. The sampling rate is increased by a factor of K with the quantization noise now spread over a wider bandwidth up to  $K \times F_s/2$ . The low-pass digital filter (typically with decimation) removes quantization noise outside of the blue region.



Figure 2a. Nyquist scenario. Sampling at F<sub>s</sub>, Nyquist bandwidth is F<sub>s</sub>/2.







Figure 2c.  $\Sigma$ - $\Delta$  ADC scenario. Oversampled and noise shaped, sampling occurring at  $F_{MOD} = K \times F_{ODR}$ .

My/nalog 🕞 🎦 💼 😭 Visit analog.com The  $\Sigma$ - $\Delta$  modulator has the added feature of noise shaping, as shown in Figure 2c. The quantization noise of the analog-to-digital conversion is shaped by the modulation scheme, shifting it (typically) from a low bandwidth up to a higher frequency, allowing a low-pass digital filter to eliminate it from the conversion result. The  $\Sigma$ - $\Delta$  ADC can be designed with the noise floor determined by thermal noise and not limited by quantization noise.

#### Sample, Modulate, Filter

The  $\Sigma$ - $\Delta$  ADC is clocked using either an internal or external sampling clock. Often the ADC's master clock (MCLK) is divided down prior to use by the modulator; be mindful of this when reading the ADC data sheet and understand the modulator frequency. The sampling frequency passed to the modulator sets the sampling frequency  $F_{MOD}$ . The modulator outputs data to the digital filter at this rate, in turn the digital filter (typically low-pass, with some decimation) provides data at the output data rate (ODR). Figure 3 illustrates this flow.

## In-Depth View of a First Order $\Sigma$ - $\Delta$ Modulator

The  $\Sigma$ - $\Delta$  modulator is a negative feedback system, analogous to a closedloop amplifier. The loop contains a low resolution ADC and DAC, as well as a loop filter. The output and feedback are coarsely quantized often only a single bit output as a high or low. The basic structure is implemented as an analog system for ADCs, where the quantizer is the block in which the sampling is accomplished. Provided conditions exist for stability of the loop, the output is a coarse representation of the input. The digital filter takes the coarse output and reconstructs an accurate digital version of the analog input.

A ones density output in response to a sine wave input is illustrated in Figure 4. The rate of change of the modulator output from a low level to high level depends on the rate of change of the input. At full-scale input of the sine wave, the modulator output switching rate reduces and the output +1 state dominates. Similarly when the sine wave is at its negative full scale, the transitions between +1 and -1 are reduced and the -1 output dominates. At the maximum rate of change of the sine wave input, the highest density of switching between +1 and -1 in the modulator output occurs. The rate of change of the output is following that of the input. It is the rate of transition of the  $\Sigma$ - $\Delta$  modulator output that describes the analog input.

Using a linear model to describe this single bit modulator (Mod 1) the system is shown as a control system with negative feedback. The quantization noise is the difference between the input and the output of the quantizer. A low-pass filter follows the input delta node. In Figure 5b, the quantization noise is described by the term N.

H(f) is the function of the loop filter and it defines both the noise and signal transfer functions. H(f) is a low-pass filter function with very high gain at low frequencies (within the bandwidth of interest) and attenuation of higher frequency signals. The loop filter can be implemented as a simple integrator or a cascade of integrators. In practice a DAC is placed in the feedback path to take the digital output signal and feed it back to the analog input delta node.



Figure 3.  $\Sigma$ - $\Delta$  ADC flow: sampling from modulator output to digitally filtered output.



Figure 4.  $\Sigma$ - $\Delta$  ones density in response to sine wave input. Linear model (a) of the Mod 1  $\Sigma$ - $\Delta$  loop.



Figure 5. Linear model (b) of the Mod 1  $\Sigma$ - $\Delta$  loop including equations, filter, signal, and noise transfer function plots.

Solving the equations shown in Figure 5 gives the signal and noise transfer functions. The signal transfer function operates as a low-pass filter, with a gain of 1 in the bandwidth of interest. The noise transfer function is a high-pass filter function, providing the noise shaping. There is strong suppression of the quantization noise at low frequencies around dc. The quantization noise signal seen at high frequencies outside the bandwidth of interest is increased. For the single-order modulator (Mod 1), the noise increases at a rate of approximately 20 dB/decade.

A common method to increase the resolution of the system is to increase the loop filter order by cascading two loop filters. The H(f) of the overall loop filter now has a greater roll off, and the noise transfer function has a transition of 40 dB/decade for a Mod 2 style. The quantization noise is shaped more aggressively, with much lower frequency noise. Figure 6 compares Mod 1 and Mod 2  $\Sigma$ - $\Delta$  ADCs. The variations and styles of  $\Sigma$ - $\Delta$  modulators are wide ranging. Architectures that circumvent stability concerns of higher order, single bit loops are called multistage noise shaping modulators (MASH) architectures. The multistage (MASH style) architectures enable design of stable, high order  $\Sigma$ - $\Delta$  modulators through a combination of inherently stable lower order loops.





Figure 6. Mod 1 and Mod 2 block diagram configurations with comparative plots of the filter and noise transfer functions.

# About the Author

Michael Clifford is an applications engineer within the Linear and Precision Technology team at Analog Devices, Ireland.

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Analog Devices, Inc. Worldwide Headquarters

Analog Devices, Inc. One Technology Way P.O. Box 9106 Norwood, MA 02062-9106 U.S.A. Tei: 781.329.4700 (800.262.5643, U.S.A. only) Fax: 781.461.3113

#### Analog Devices, Inc. Europe Headquarters

Analog Devices, Inc. Wilhelm-Wagenfeld-Str. 6 80807 Munich Germany Tel: 49.89.76903.0 Fax: 49.89.76903.157 Analog Devices, Inc. Japan Headquarters

Analog Devices, KK New Pier Takeshiba South Tower Building 1-16-1 Kaigan, Minato-ku, Tokyo, 105-6891 Japan Tel: 813.5402.8200

Fax: 813.5402.1064

Analog Devices, Inc. Asia Pacific Headquarters

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