Functional SPI Isolation

Assuming a constant ground voltage helps us analyze circuits, but it is not necessarily accurate![1] A combination of parasitic inductance and large high frequency currents creates voltage noise on circuit grounds. For example, large high frequency currents flowing through a ground reference can result from thousands of transistors in digital circuitry switching simultaneously. This is bad news for sensitive analog components, such as a analog-to-digital converters (ADC) that use the digital components' ground.

It is important to provide a clean ground reference for analog components. Implementing a multipoint grounding system and filtering the analog circuits' supply connections are useful techniques. Digital isolation allows components to have different ground references and still maintain a communication link. For the purposes of isolating ground noise from sensitive components where safety isolation is not required, a high isolation rating is unnecessary. Digital isolators with 1 kV rms withstand voltages, such as the ADuM744x family, are more than sufficient for ground noise isolation applications.

Figure 1 shows an ADuM7441 isolating an SPI bus between a microcontroller and an ADC, allowing them to operate with separate ground references. Table 1 lists the maximum SPI clock frequencies that are possible with the ADuM7441A and ADuM7441C using 5 V and 3.3 V supplies given their maximum propagation delays.[2] Refer to Reference 2 for information on clocking isolated SPI buses.

An alternative implementation of an isolated SPI bus is shown in Figure 2. In this case, the data from the ADC (DOUT) is clocked into a separate register by a delayed version of SCLK; this implementation also allows for three more slave devices. The SPI bus can be clocked at rates up to 12.5 MHz with the ADuM744x family in this configuration. The ADuM7442 in Figure 2 isolates SCLK, DIN, and DOUT; the ADuM7440 isolates four CS_x signals. The three other channels in the ADuM7440 can be used to isolate CS_x signals for three more slave devices. Alternatively, the ADuM140x family can be used in this configuration with clock rates of up to 45 MHz. The delayed clock implementation allows the SPI bus to be clocked at a digital isolator's maximum data rate.
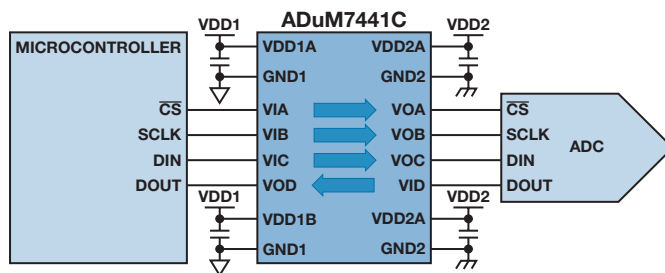

Figure 1.

Table 1.

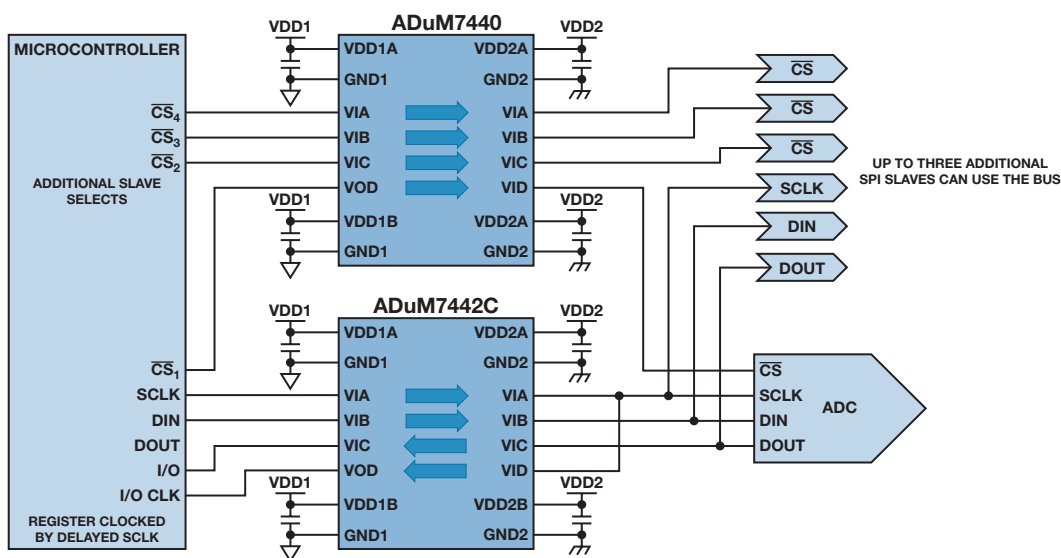| Model	Supply Configuration (V)	Maximum Propagation Delay (ns)	Maximum SCLK Frequency (MHz)
ADuM7441A	3.3	85	2.9
	5.0	75	3.3
ADuM7441C	3.3	66	3.7
	5.0	50	5.0

Figure 2.

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References

[1] Ott, H.W. *Noise Reduction Techniques in Electronic Systems*. New York, NY: John Wiley & Sons, 1988. pp. 73–115.

[2] Cantrell, M. "Clocking Options for SPI."
http://www.analog.com/static/imported-files/newsletters/digital_isolation/iCoupler_0308.html

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