

in LinkedIn 🖂 Email

An Interview with Analog Devices Discussing RF Electronics for Phased Array Applications

Peter Delos

Design Section Leader, Analog Devices, Inc.

Introduction

We are witnessing an historic moment for radio frequency (RF) electronics in phased array applications. Rapid advancements in the wireless industry have proliferated the integration and miniaturization of RF electronics. Many applications now reap the benefits of these achievements. The integration of large sections of the signal chain into complete integrated circuits (ICs) has enabled phased array antennas in particular. New systems are proliferating with analog beamforming or digital beamforming implementations fueled by recent IC releases into the broad markets.

At Analog Devices we routinely receive inquiries and interview requests from customers and publishers. The complete portfolio offering an antennato-bits solution ranging from RF to high speed converters, transceivers, PLLs, and power, along with advanced integration, has created a system architecture expertise. There is much curiosity about our developments covering the entire RF signal chain that will enable the phased arrays of the future.

This article summarizes some of the routine inquiries that are scattered in various forms on the internet into a more comprehensive discussion. We start with a brief history of phased array evolution, discuss architecture trends and challenges, offer insight into our view of recent developments, and offer links to articles and webcasts that provide more detail on various topics.

Let's Start with the Evolution of Phased Arrays. How Did We Get Here?

Much of the early phased array work was developed for radar applications, so considering the evolution of radar antenna implementations provides good insight as to how the modern digital beamforming antennas were conceived. Out of necessity, significant radar development was accelerated during and after World War II. Following World War II, the majority of mathematics used today for waveform and radar processing was worked out at various government laboratories and organizations. An important radar processing technique is pulse compression. Pulse compression is enabled by waveform choices such as linear frequency modulations (LFMs) and phase codes where the pulse at the output of the matched filter is much shorter than the transmitted pulse. The amount of pulse compression is directly related to signal bandwidth. This was all documented and understood by the 1960s. Some say radar was born with pulse compression. With the mathematics understood, extended implementation developments continued, and ultimately lead to the modern phased array.

F Facebook

The first implementations had rotating antenna dishes with high power RF being generated in tube amplifiers. Rotating dishes were then replaced with the first phased array antennas, which were used for very high performance radars. The tube high power amplifiers (HPAs) remained and the transmit signal flow was: tube HPAs \rightarrow waveguide distribution \rightarrow phase shifters \rightarrow radiating elements. The beamforming was an all analog system. On receive, several beam patterns could be made, but the process was complex and expensive, so it was typically limited to a few beams. Antenna systems for monopulse radars could be implemented this way. The first step toward solid-state phased arrays was the introduction of transmit/ receive (T/R) modules distributed at every element, with first implementations still using analog beamforming with similar backend processing. The T/R module consists of a solid-state HPA for transmit, a low noise amplifier (LNA) for receive, and either a circulator or switch to control the direction of RF energy (transmit or receive) from the antenna.

The current transition in progress is the migration toward digital beamforming phased arrays. Hybrid architectures consisting of analog beamformed subarrays, then receivers and ADCs behind every subarray, allow digital beamforming to form many beams within the subarray pattern. Everyelement digital phased arrays include receivers and waveform generators behind every element. The every-element digital beamformed phased array is the enabler for truly software-defined antenna patterns. Many beams can be formed simultaneously in many diverse directions, and the antenna patterns can be adaptively controlled, including nulls. Due to the systemlevel programmability, every-element digital phased arrays have become the goal for many antenna architects.

My/nalog 🖸 🎦 in 🚹 Visit analog.com

Can You Further Explain the Difference Between Analog and Digital Beamforming?

This is may be best understood with an illustration such as Figure 2. In analog beamforming, there is a phase shifter and gain control in the RF domain behind every element, typically after a T/R module. The beam direction is formed by controlling the RF phase of each element prior to combining. An amplitude taper can be applied to help antenna sidelobe levels. In digital beamforming, a similar process is done except it is all digital. There are complete receivers with ADCs for every element, the beamforming is done in the digital domain, phase shifts are applied digitally on each channel, and a weighted sum forms the antenna pattern. Because the beam is formed digitally, many antenna beam patterns can be created simultaneously on the same ADC data. This is accomplished by duplicating the digital beamforming time delay and summing structures. It is a form of parallel processing that creates multiple beams that are independently programmable from the same ADC data stream. In theory, this could be extended to a very large number of beams. In practice, the realizable limit is typically set by the digital processing capability. To bound the processing with practical data rates, some systems define a beam bandwidth product. This definition allows a trade-off between the number of beams and the bandwidth per beam while maintaining a constraint on the data rates required for the system.

One benefit of analog beamforming is the simplicity of the implementation. There are few data converters, and thus a very manageable digital development effort. The challenge is that the analog beamforming structure has to be repeated for every antenna beam. There are also single points of failure after the beamforming. However, for low cost, low beam count systems, analog beamforming is a good choice and will be a primary candidate in cost-constrained antenna systems.

The benefits of digital beamforming are in the flexibility for multiple programmable antenna beams simultaneously in many directions. Unfortunately, the challenges are significant, including the large volume of digital data, the synchronization, and physical size constraints for the electronics needed behind every radiating element. In spite of the challenges, it can still be a cost-effective architecture when many simultaneous beams are needed from a single antenna.

A compromise is to use a mix of both analog and digital beamforming. In this case, elements are formed into subarrays in the analog domain, then beams can be formed digitally within the subarray pattern. This can be considered a hybrid architecture and is also quite popular when digital beamforming is desired, but full digital beamforming is not practical due to any of the varied challenges or system cost constraints.



Figure 1. The evolution of phased array. There have been continual technological advancements from the beginning of radars implemented with rotating dishes to the most recent every-element digital phased arrays.



Figure 2. Analog vs. digital beamforming.

Can You Describe Some of Your Work in RF Front Ends?

First, let's define the RF front end. This typically consists of the T/R module along with any analog beamforming. We are developing products in all of these areas. HPAs and LNAs are regularly released to support market demands. There are also low loss, high power switches that enable rapid front-end switching between transmit and receive. These can be integrated into T/R modules as a full solution when appropriate for customer applications.

The industry is doing a lot of work to improve GaN technology for HPAs and LNAs. There are several well-publicized primary motivators such as the capability for higher power density and higher breakdown voltages. There are also additional motivators for phased array applications. With higher operating voltages, there is less current in the power distribution leading to overall system efficiency benefits. The higher breakdown voltages bring a higher survive power for LNAs and, in some cases, can eliminate the need for front-end limiters that can lead to an overall lower receiver noise figure even if the GaN LNA noise figure is slightly above a GaAs LNA.

For analog beamformers, we have recently released the ADAR1000. This is an X- and Ku-band, 4:1 analog beamformer. In addition to all the required analog beamforming functions, a unique feature for HPA/LNA pulsing through the gate control has been included. Rapid turn on/off has been demonstrated through control of the gate rather than the drain. This approach eliminates the need to switch high current through the drain. We have released application notes on possible circuit techniques for gate switching and the capability in the ADAR1000 to aid in simplification of the control circuitry around the T/R modules.

For the Receivers and Waveform Generators, What Are Some of the Architectures Being Implemented Today?

The receiver and waveform generator architectures can roughly be categorized in three variations: heterodyne, direct conversion, and direct sampling. There are pros and cons of each architecture choice depending on the application. We view all of them as having a place depending on the objective and create ICs supporting all of the architectures depending on how people use the parts. Figure 3 illustrates the different architectures. Although only the receiver is shown, the topologies also apply to the waveform generator signal chains.

The superheterodyne approach, which has been around for 100 years now, is well-proven, and can provide exceptional performance with proper frequency planning. Unfortunately, it is also the most complicated. It typically requires the most power, the largest physical footprint relative to the available bandwidth, and frequency planning that can be quite challenging at large fractional bandwidths. It is also the least programmable, unless added hardware is included to switch between a variety of filter and LO paths. One of the newer trends is that modern high speed converters and transceivers offer the ability to sample at higher IF frequencies. Use of these latest releases can simplify frequency plans, eliminate mixing stages, and reduce companion agile LO complexity.

The direct sampling approach has long been sought after, but has faced the obstacles of operating the converters at speeds commensurate with direct RF sampling and achieving large input bandwidth. Today, high speed converters are available for direct sampling through S-band and higher, and several are listed in the references. Sampling at GSPS rates with analog input bandwidths above 6 GHz is new with the latest high speed converters. Direct sampling of higher frequencies will continue to be a trend to watch in emerging data converters. As next-generation FinFET CMOS nodes continue to increase the transistor operating speeds and reduce parasitic capacitance, new families of data converters will become possible, with potential to have a significant impact on future RF system design.

Direct conversion architectures provide the most efficient use of the data converter bandwidth. The data converters operate in the first Nyquist where performance is optimum and low-pass filtering is easier. The two data converters work together sampling I/Q signals, thus increasing the user bandwidth without the challenges of interleaving. The dominant challenge that has plagued the direct conversion architecture for years has been to maintain I/Q balance for acceptable levels of image rejection, LO leakage, and dc offsets. In recent years, the advanced integration of the entire direct conversion signal chain, combined with digital calibrations, has overcome these challenges. Our transceiver product line is based on direct conversion architectures. Where the performance is a fit, these will be the most highly integrated, economical solutions available.

| Туре | Configuration | Benefits | Challenges |
|-------------------|---------------|--|--|
| Heterodyne | | Proven/trusted High performance Optimum spurious High dynamic range EMI immunity | SWaPMany filters |
| Direct Conversion | | Maximum ADC BW Simplest WB option | Image rejection I/Q balance In-band IF harmonics L0 radiation EMI immunity (IP2) DC and 1/f noise |
| Direct Sampling | | No mixing Now practical at L-/S-band | ADC input BW Gain not distrubuted across frequency |

Table 1. Receiver Architecture Options



Figure 3. Half wavelength element spacing vs. frequency.

Are There Any Other Benefits to Distributing the Waveform Generators and Receivers in a Digital Beamforming Array?

One of the system engineering objectives with distributed RF electronics is to achieve a dynamic range improvement as channels combine. When combining two RF signals, if the RF signals are matched in amplitude and phase, and if noise in each of the channels is uncorrelated, there will be a 10logN combining gain producing a dynamic range improvement. If the noise in the channels is correlated, there is no improvement when they are combined. Therefore, one of the system engineering efforts is to track noise contributors that are correlated vs. uncorrelated. Correlated noise can come from anything shared across channels, including clocks, LOs, power, etc.

For large arrays there is significant value to this improvement. For example, 100 channels can offer a 20 dB dynamic range improvement if the noise components are all uncorrelated. We have developed our own multichannel RF testbeds to ensure these parameters are understood both for our customers use of our components and for our own internal design efforts.

Can You Elaborate on the Physical Size Challenges Designers Encounter in Digital Beamforming Phased Arrays?

A fundamental physical challenge is the element spacing as a function of wavelength, which reduces as the operating frequency increases. Many systems set the element spacing at half the wavelength or less to avoid grating lobes in the antenna pattern. At L- and S-band, it is practical to fit the electronics in an every-element spacing, utilizing the latest transceivers or direct sampling converters. As frequency increases to X-band (10 GHz), it is challenging, but possible, with advanced integration. At Ka-band, it is quite challenging. As frequency increases, hybrid architectures can become more practical and a 4:1 beamformer, such as the ADAR1000, can reduce the receiver/exciter count by 4 and allow additional space to be allocated for the RF electronics.



To address this challenge, we are continuing to integrate full sections of the signal chains. Multichannel integrated transceivers and converters form the foundation for RF sampling in a reduced physical footprint. In addition, integrated RF design in monolithic RFICs, SiPs (system in packages), and integrated T/R modules are all continually advancing. The combination of the multichannel high speed converters or transceivers with the RF advancements enables the integration needed for modern phased array implementations.

Additional Links/References

Phased array design covers many aspects of engineering from radio frequency design, power distribution, high speed digital design, advanced packaging, and digital signal processing. The breadth of the Analog Devices portfolio covers all of these areas. The comprehensive range of offerings in a single company is quite unique to the RF/microwave industry and an enabler for system integrators developing phased array antenna systems. Here we have introduced the trends and some of the considerations. Much more technical information is online at *analog.com*, along with all of the product data sheets. A starting point is offered below for technical articles, webcasts, and recent ICs all applicable to phased array applications.

Masterson, Claire. "Massive MIMO and Beamforming: The Signal Processing Behind the 5G Buzzwords." *Analog Dialogue*, Vol. 51, June 2017.

Delos, Peter. "Advanced Technologies Pave the Way for New Phased Array Radar Architectures." Analog Devices, Inc., Nov. 2016.

Delos, Peter and Jarret Liner. "Unique Gate Drive Applications Enable Rapidly Switching On/Off for Your High Power Amplifier." *Analog Dialogue*, Issue 148, Dec. 2017.

Delos, Peter, Michael Jones, and Mark Robertson. "RF Transceivers Enable Forced Spurious Decorrelation in Digital Beamforming Phased Arrays." Analog Devices, Inc., Sept. 2018.

Delos, Peter. "System-Level LO Phase Noise Model for Phased Arrays with Distributed Phase-Locked Loops." Analog Device, Inc., Nov. 2018.

Half Wavelength Spacing (in mils)

Delos, Peter and Jarret Liner. "Improved DAC Phase Noise Measurements Enable Ultra-Low Phase Noise DDS Applications." *Analog Dialogue*, Vol. 51, Aug. 2017.

Delos, Peter. "A Review of Wideband RF Receiver Architecture Options." Analog Devices, Inc., Feb. 2017.

Brannon, Brad. "Some Recent Developments in the Art of Receiver Technology: A Selected History on Receiver Innovations over the Last 100 Years." *Analog Dialogue*, Vol. 52, Aug. 2018.

Benson, Keith. "Advances in Phased Array Analog Beamforming Solutions." Analog Devices, Inc. Webcast, Sept. 2017.

Delos, Peter. "Digital Beamforming Techniques for Phased Arrays." Analog Devices, Inc. Webcast, Jan. 2017.

Jones, Michael. "Enabling Next-Generation EW and Phased-Array Systems." Analog Devices, Inc. Webcast, 2018.

Henderson, Greg. "RF/Microwave Product Selector Guide." Analog Devices, Inc. June 2018.

ADAR1000: Analog Beamformer. Analog Devices, Inc., 2019.

Phase Locked Loop (PLL) Synthesizers. Analog Devices, Inc., 2019.

AD9213. Analog Devices, Inc., 2019.

AD9208. Analog Devices, Inc., 2019.

AD9172. Analog Devices, Inc., 2019.

ADRV9009. Analog Devices, Inc., 2019.

About the Author

Peter Delos is a technical lead in the Aerospace and Defense Group at Analog Devices in Greensboro, North Carolina. He received his B.S.E.E. from Virginia Tech in 1990 and M.S.E.E. from NJIT in 2004. Peter has over 25 years of industry experience. Most of his career has been spent designing advanced RF/analog systems at the architecture level, PWB level, and IC level. He is currently focused on miniaturizing high performance receiver, waveform generator, and synthesizer designs for phased array applications. He can be reached at *peter.delos@analog.com*.

Online Support Community



Engage with the

Analog Devices technology experts in our online support community. Ask your tough design questions, browse FAQs, or join a conversation.

Visit ez.analog.com

Analog Devices, Inc. Worldwide Headquarters

Analog Devices, Inc. One Technology Way P.O. Box 9106 Norwood, MA 02062-9106 U.S.A. Tel: 781.329.4700 (800.262.5643, U.S.A. only) Fax: 781.461.3113

Analog Devices, Inc. Europe Headquarters

Analog Devices GmbH Otl-Aicher-Str. 60-64 80807 München Germany Tel: 49.89.76903.0 Fax: 49.89.76903.157

Analog Devices, Inc. Japan Headquarters

Analog Devices, KK New Pier Takeshiba South Tower Building 1-16-1 Kaigan, Minato-ku, Tokyo, 105-6891 Japan Tel: 813.5402.8200 Fax: 813.5402.1064

Analog Devices, Inc. Asia Pacific Headquarters

Analog Devices 5F, Sandhill Plaza 2290 Zuchongzhi Road Zhangjiang Hi-Tech Park Pudong New District Shanghai, China 201203 Tel: 86.21.2320.8000 Fax: 86.21.2320.8222 ©2019 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. Ahead of What's Possible is a trademark of Analog Devices. T21044-0-1/19

analog.com

