How to Achieve 7.5-Digit Accuracy in Instrumentation Applications: Part 2

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Abstract

This article explores the challenges involved with designing high accuracy equipment for instrumentation applications. It will introduce a high precision signal chain solution composed of a high linearity successive approximation register (SAR) analog-to-digital converter (ADC), a fully integrated ultralow drift precision reference, a quad-matched resistor network, and a zero-drift low noise amplifier. It will discuss the measurement results found in "How to Achieve 7.5 Digits Accuracy in Instrumentation Applications: Part 1".

Introduction

In various high precision industries, there is a common reliance on 7.5-digit or higher resolution digital multimeters (DMMs) employing multislope integrating ADCs constructed from discrete components. While these ADCs can provide reasonably accurate measurements, their design and troubleshooting processes tend to be more complex for most customers, who often opt for commercial ADC integrated circuits (ICs) to streamline their designs.

Over the past decade, 24-bit sigma-delta ADCs were widely implemented in 6.5-digit DMM design. However, higher performance ADCs became a limiting factor in achieving 7.5 digits of accuracy and linearity. Additionally, addressing the issue of reference voltage presents a challenge, particularly in the case of buried Zener voltage references, which require intricate external signal conditioning circuitry to attain ultralow temperature drift.

These scenarios hold true for various high precision applications, such as 3-phase standard meters, field meter calibrators, high accuracy data acquisition (DAQ) systems, laboratory weighing scales, seismic instrumentation, and source measure units (SMUs)/power measurement units (PMUs) in automated test equipment (ATE).

This article will introduce a high precision signal chain solution composed of a high linearity SAR ADC, a fully integrated ultralow drift precision reference, a quad matched resistor network, and a zero-drift low noise amplifier. Real measurement results for several key specifications will be provided, along with discussions of several typical applications for the reader's reference.

Solution and Evaluation System Introduction

The high accuracy solution consists of two boards: a 7.5 digits high accuracy signal chain board and a controller board

- Initially, the input signal passes through an EMI filter for differential mode and common-mode filtering. It then proceeds into the AFE signal conditioning circuit to convert the signal within the ADC input range. This circuit ensures extremely low drift over temperature, minimal noise interference, and accurate gain. For ensuring system accuracy and temperature drift characteristics, Analog Devices' oven-controlled precision voltage reference ADR1001 is used to provide a 5 V reference voltage for the ADC and a 2.5 V common-mode voltage for the AFE circuit.
- A crucial subsequent step is the entry of the conditioned signal into ADI's AD4630-24, renowned for its linearity and high resolution.
- The controller board gathers the data from the ADC and transfers it to the PC. ADI's EVAL-AD4630-24's ACE software is used to configure the AD4630 (sampling rate, ADC channel, and acquisition mode) and analyze the ADC data.

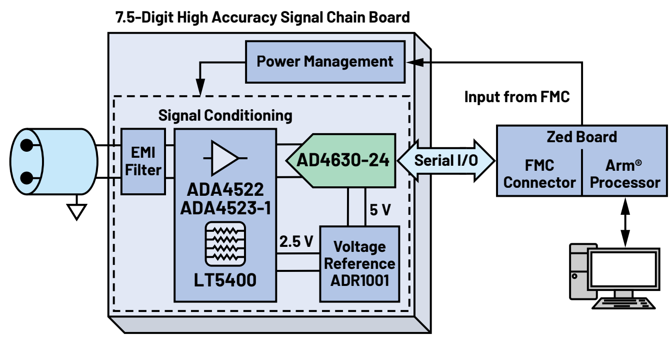

Figure 1. 7.5-digit high accuracy signal chain board.

Figure 2 is the evaluation system setup. The DC source generates the signal, which is fed into the signal chain board, and the Zedboard gathers the data and transfers it to the PC by the USB.

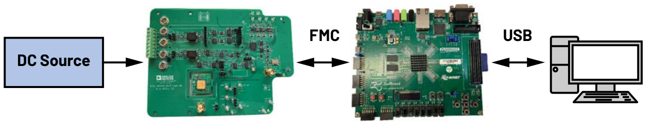

Figure 2. Evaluation system setup.

Figure 3 depicts the linearity curve of the DC source as measured by an 8.5-digit DMM. The DMM is set to a 500 PLC (power line cycle) reading rate. After addressing offset and gain errors, and conducting a 2 point calibration, the linearity error of the DC source in conjunction with the DMM falls within the range of ±0.1 ppm, indicating an excellent result. This level of performance from the DC source makes it well-suited for evaluating the capabilities of a 7.5-digit high accuracy signal chain.

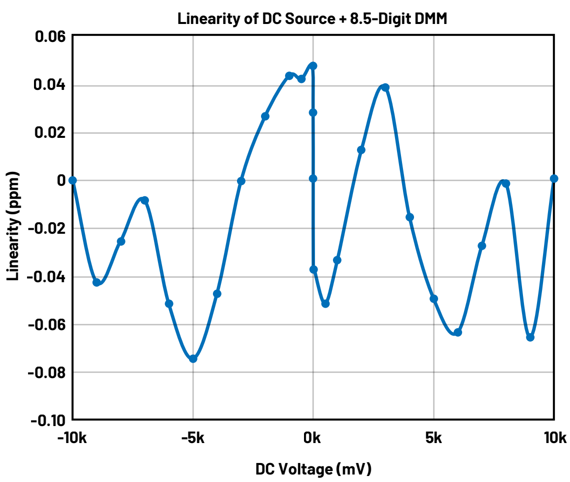

Figure 3. Linearity of DC source +8.5-digit DMM.

Test Result

In order to fully evaluate the performance of the signal chain board, the test was carried out in four steps: noise test, linearity test, temperature coefficient (TC) test, and a 24-hour accuracy test.

Noise Test

The initial step in evaluating the board's performance is assessing its noise characteristics, which lays the foundation for subsequent tests. In cases where the system's noise level is elevated, it can lead to slight variations in measurement data for linearity and accuracy, potentially resulting in reduced overall performance. A total of four boards are measured, two boards' AFE circuit incorporate ADI's ADA4522, while the other two boards employ the ADA4523-1. The specific experimental settings are as follows:

- The two input terminals of the board are shorted to ground.
- The ADC's sampling rate is set to 62.5 kHz or 1 MHz, and the average value register of the ADC is configured to 4096 or 65536. The output rate remains fixed at 15 Hz.
- Three samples are averaged to yield one data point (resulting in a 5 Hz, 10 PLC reading rate). A total of 50 data points are gathered to calculate the rms noise.

The ADR1001 serves as the reference for this experiment.

Table 1 shows the measured noise of the four boards.

- The ADA4523-1 board has a lower noise performance than the ADA4522 board. The noise of the ADA4523-1 board is about 500 nV rms with 62.5 kHz F_S, meaning 0.05 ppm noise (500 nV rms/10 V).
- With higher sampling rates (such as 1 MHz, which is about 16 times of 62.5 kHz), and while keeping the output rate constant at 15 Hz output rate, it is possible to reach noise levels that are up to four times lower. This aligns with the principles of the oversampling theory.

Table 1. Measured Noise Results at Different F_S

Board	Measured Total Noise (F_S = 62.5 kHz)	Measured Total Noise (F_S = 1 MHz)
Board 1 (ADA4522)	727.27 nV	242.42 nV
Board 2 (ADA4523-1)	530.73 nV	122.02 nV
Board 3 (ADA4522)	818.18 nV	318.18 nV
Board 4 (ADA4523-1)	439.39 nV	121.21 nV

Figure 4 shows the rms noise of Board 3 and Board 4 with an input at 10 PLC reading rate (F_S = 1 MHz).

- As the orange curve shows, the ADA4523-1 board has lower noise performance.
- In the cases of two boards, the overall rms noise increases in tandem with the input. This can be due to two key factors: (1) As the input (V_{IN}) increases, the ratio V_{IN}/V_{REF} increases, leading to a greater contribution of V_{REF} noise to the overall system noise, and (2) the input signal originates from a DC source, which is not ideal as the output rms noise of the DC source may increase with its output signal amplitude.
- The curves are not monotonous and both curves share similar characteristics. This behavior may be attributed to nonideal qualities in the DC source.

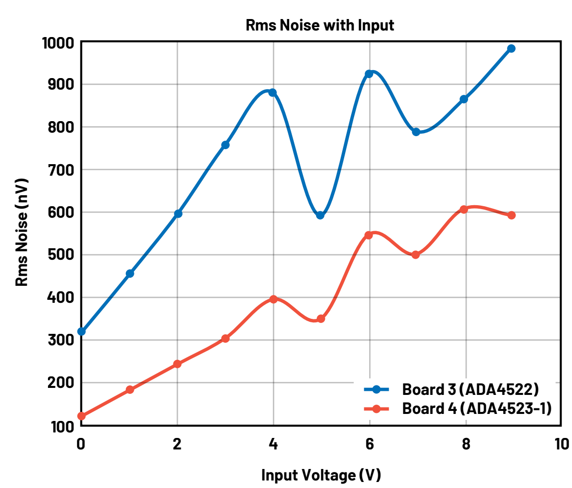

Figure 4. Rms noise with input at 10 PLC reading rate.

Linearity Test

Evaluation of the ADA4522/ADA4523-1 + AD4630-24 + ADR1001

In the linearity test, the ADC is set to a 62.5 kHz sampling rate, the average value register is set to 4096, the output data rate is at 15 Hz, 30 samples are collected, and the average value is read, which corresponds to 100 PLC reading rate.

The DC source generates a ±9 V signal as the input. The ±9 V input signal is chosen for comparing the performance between the ADR1001, the ADR1399, and the ADR4550 D grade. The result of Board 2 (ADA4523-1) is shown in Table 2.

Table 2. INL Test Results of Board 2 (ADA4523-1)

Input Voltage (mV)	ADC Reading	Input Voltage Reading After Calibration	Error (ppm)
9000	-483369652.3	-9000	0
8000	-429662903.8	-7999.999873	0.0141
7000	-375956223.4	-7000.001015	-0.1128
6000	-322249399.4	-5999.999482	0.0576
5000	-268542733	-5000.000884	-0.0982
4000	-214835963	-4000.000357	-0.0396
3000	-161129232.7	-3000.00057	-0.0633
2000	-107422478.8	-2000.000342	-0.0379
1000	-53715760.87	-1000.000785	-0.0872
0	-8977.033	0	0
0	-7377.033	0	0
-1000	53699320.73	999.9992934	-0.0785
-2000	107406047.8	1999.999132	-0.0964
-3000	161112827.2	2999.999945	-0.0061
-4000	214819567.7	4000.000034	0.0038
-5000	268526316.7	5000.000282	0.0313
-6000	322232987	5999.999065	-0.1039
-7000	375939825.3	7000.000974	0.1083
-8000	429646511.3	8000.000048	0.0053
-9000	483353244.4	9000	0

The first column is the input voltage, the second column is the ADC reading, the third column is the measured voltage obtained after 2 point calibrating of the ADC readings, and the fourth column is the full-scale INL (integral nonlinearity) error. Table 2 shows that the INL error of the whole system reaches 0.11 ppm.

The linearity of the four circuit boards is shown in Figure 5. As shown, the INL of the four circuit boards does not exceed 0.2 ppm, which matches the typical INL spec of the AD4630-24. A linearity of 0.2 ppm is significantly better than the 1.5 ppm linearity currently found in today's 7.5-digit DMMs.

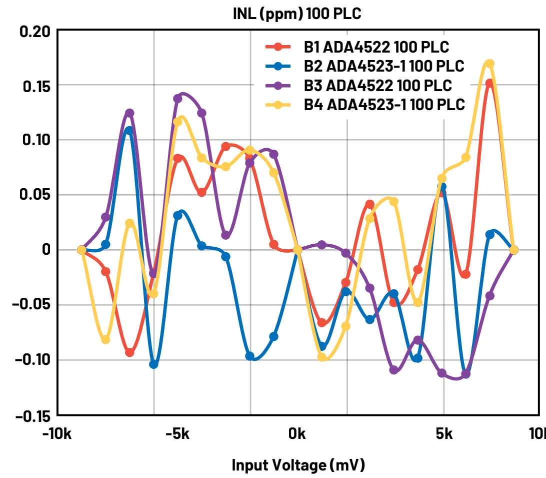

Figure 5. INL results with the ADR1001 (100 PLC).

When the ADC is set to a 62.5 kHz sampling rate, the average value register is set to 1024, the output data rate is 60 Hz, 12 samples are collected, and the average value is read, which corresponds to a 10 PLC reading rate. This setting is usually accompanied by higher noise, as shown in Figure 6, as the INL results degrade to ±0.32 ppm.

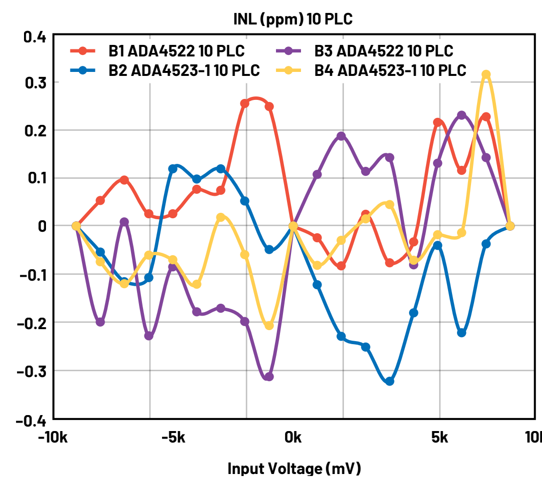

Figure 6. INL results with the ADR1001 (10 PLC).

ADA4522/ADA4523-1 + AD4630-24 + ADR1399

The ADR1399 has similar performance as ADI's LM399, which is widely used in high accuracy DMMs. To assess the ADR1399's performance as an ADC reference, the ADR1001 output is disconnected. Instead, the ADR1399 daughter board is linked to the signal chain board via an SMA connector. This setup supplies the voltage reference to the ADC and a bias voltage to the signal conditioning circuit. The ADR1399's typical output voltage is 7 V, the LT5400-1 is used to attenuate the ADR1399's output to get 4.67 V as ADC reference and 2.33 V as bias voltage. So, a ±9 V input voltage is used in the test.

Each signal chain board is equipped with a separate ADR1399 daughter board. Board 1 and Board 2's ADR1399 package is LCC, and Board 3 and Board 4's ADR1399 package is TO-46.

Figure 7 is the INL results of the ADR1399 with a 100 PLC, it is within ±0.3 ppm. Compared to the ADR1001's 0.2 ppm INL, the ADR1399's 0.3 ppm is a little bit worse, but still lower than that of a typical 7.5-digit DMM of 1.5 ppm INL. Also, the ADR1399 LCC package and TO-46 package haven't shown much difference in terms of INL measurement.

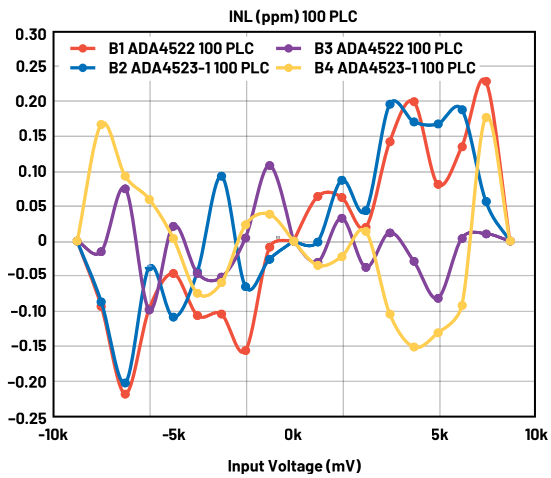

Figure 7. INL results with ADR1399 (100 PLC).

ADA4522/ADA4523-1 + AD4630-24 + ADR4550D

The ADR4550D daughter boards are connected to boards 3 and 4 to measure the linearity spec. Refer to Figure 8, which shows that the INL is within ±0.4 ppm.

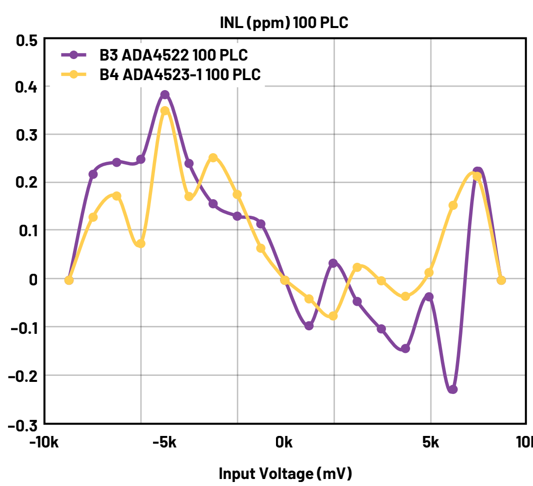

Figure 8. INL results with the ADR4550D (100 PLC).

Temperature Coefficient Test

The temperature coefficient of a typical 7.5-digit DMM is 5 ppm + 1 ppm, and it is 0.5 ppm + 0.01 ppm for an 8.5-digit DMM.

ADA4522/ADA4523-1 + AD4630-24 + ADR1001

The temperature coefficient of the system is measured by the 100 PLC reading rate. The test board is placed into the incubator, and the temperature is set to 40°C. After waiting for the thermostat to stabilize, input the signal to 0 V+, 5 V, 9 V, 0 V-, -5 V, and -9 V through the DC source and read the ADC reading from the ACE software. Then, set the temperature to 23°C and 0°C and repeat the above test. The temperature coefficients of gain error and offset error are calculated as shown in the formulas below. Note that the actual measured value is the ADC reading multiplied by 9.313 nV. Since there is 0.5 times gain between the value read by the ADC and the input voltage, the denominator is half of the input voltage.

$$\text{Gain Error} = \frac{\text{ADR reading error} \times 9.313\ nV}{\frac{\text{Input voltage}}{2}} / (T - T_0) \quad (1)$$

$$\text{Offset Error} = \frac{\text{ADR reading error} \times 9.313\ nV}{10\ V/2} / (T - T_0) \quad (2)$$

Table 3. Temperature Coefficient Results of Board 1

Input Voltage	ADC Reading at T = 40°	ADC Reading at T_0 = 0°	ADC Reading Error	ppm/°C	Error Type
0 V+	5655.7	5802.767	147.067	0.0068481749	Offset
5 V	-268593323.267	-268587481.167	5695.033	0.5303784233	Gain
9 V	-483472282.7	-483461764.133	10371.5	0.5366098861	Gain
0 V-	7360.167	7428.9	68.733	0.0032005521	Offset
-5 V	268606411.1	268600957.167	-5522.666	-0.5143258846	Gain
-9 V	483485748.533	483476016.2	-9801.066	-0.5070962648	Gain
Input Voltage	**ADC Reading at T = 23°**	**ADC Reading at T_0 = 0°**	**ADC Reading Error**	**ppm/°C**	**Error Type**
0 V+	5738.	5802.767	64.367	0.0052126076	Offset
5 V	-268590538.167	-268587481.167	2992.633	0.4847024544	Gain
9 V	-483467520.6	-483461764.133	5692.1	0.5121790077	Gain
0 V-	7348	7428.9	80.9	0.0065514930	Offset
-5V	268603652.3	268600957.167	-2776.033	-0.4496207883	Gain
-9 V	483480833.567	483476016.2	-4898.267	-0.4407493775	Gain

The temperature coefficient results of the boards with different references are shown in Figure 9, Figure 10, and Figure 11.

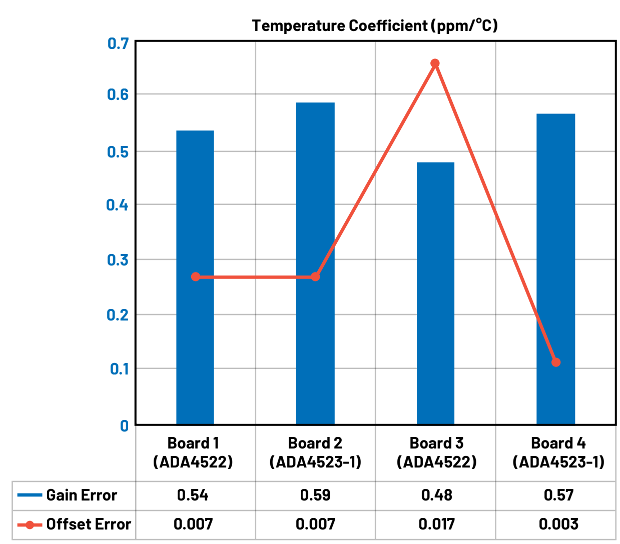

Figure 9. Temperature coefficient results with the ADR1001.

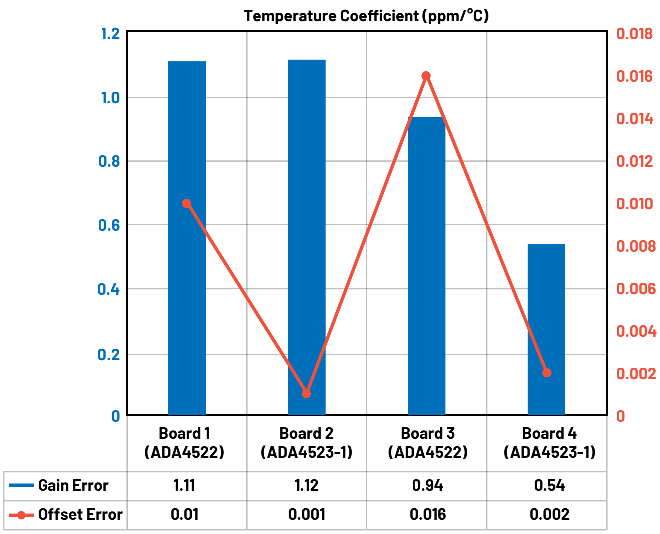

Figure 10. Temperature coefficient results with the ADR1399.

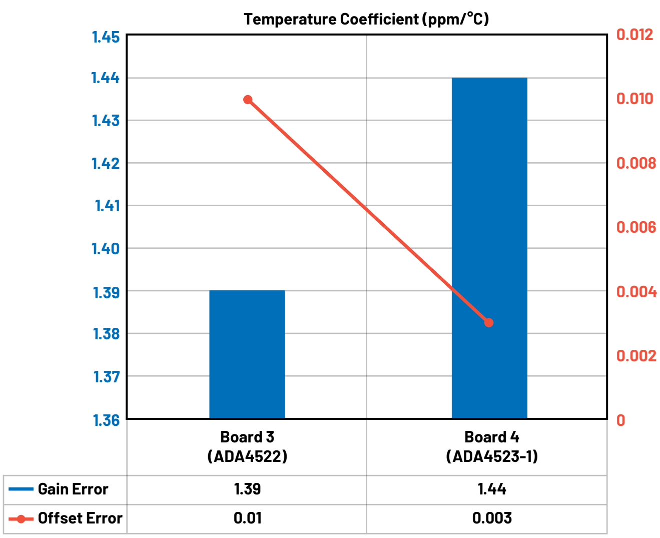

Figure 11. Temperature coefficient results with the ADR4550D.

Table 4 shows the comparison of temperature coefficient results between the ADR1001, the ADR1399, and the ADR4550D. According to the previous accuracy analysis and the experiment data:

- The LT5400 contributes to the offset error TC. It is important to highlight that there are not any notable distinctions observed among various references in this aspect.
- The LT5400 and references contribute to the gain error TC. The signal chain board with the ADR1001 has the highest TC performance. The ADR1399 and ADR4550D are slightly less efficient in terms of TC compared to the ADR1001.

Table 4. TC Comparison with Different References

	Board with ADR1001	Board with ADR1399	Board with ADR4550D	Typical 7.5-Digit DMM	Typical 8.5-Digit DMM
Offset Error/ Range Error (ppm/°C)	0.017	0.016	0.01	1	0.01
Gain Error/ Reading Error (ppm/°C)	0.59	1.12	1.44	5	0.5

24-Hour Accuracy Test

The 24-hour accuracy of a typical 7.5-digit DMM is 8 ppm + 2 ppm, and it is 0.5 ppm + 0.05 ppm for an 8.5-digit DMM.

ADA4522/ADA4523-1 + AD4630-24 + ADR1001

The 24-hour accuracy is measured by the 100 PLC reading rate. First, the test board is placed into the incubator and the temperature is set to 23°C. After waiting for the thermostat to stabilize, input the signal to 0 V+, 5 V, 9 V, 0 V−, −5 V, and −9 V through DC source and read the ADC data from the ACE software. After 24 hours, repeat this test. Calculating gain error and offset error for 24-hour accuracy is akin to determining temperature coefficient error, with the sole distinction being the absence of temperature variation.

The 24-hour accuracy results of the signal chain boards are shown in Figure 12, Figure 13, and Figure 14.

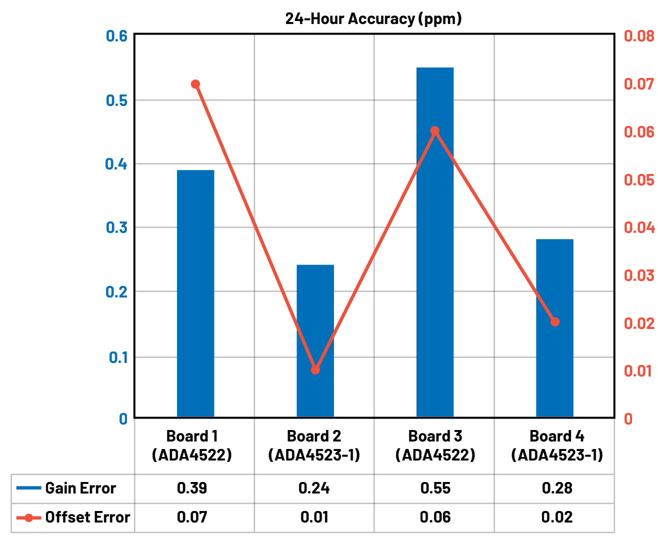

Figure 12. 24-hour accuracy results with the ADR1001.

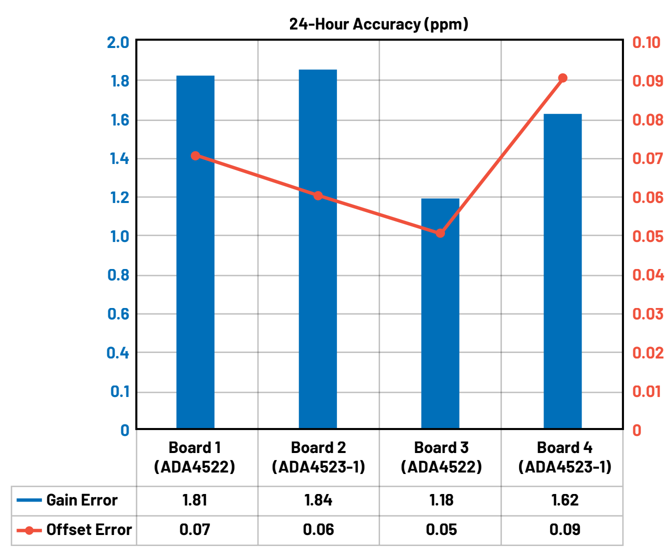

Figure 13. 24-hour accuracy results with the ADR1399.

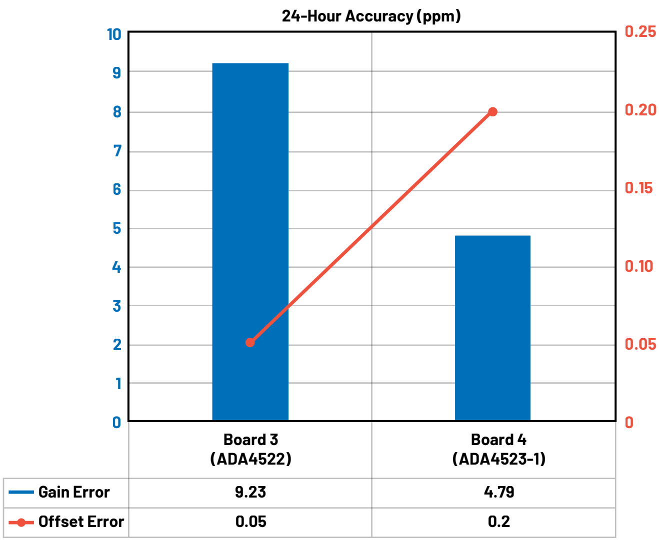

Figure 14. 24-hour accuracy results with the ADR4550D.

Table 5 shows the comparison of the 24-hour accuracy results between the ADR1001, the ADR1399, and the ADR4550D. Based on the previous accuracy analysis and the experiment data:

- The LT5400 contributes to the offset error, and there are not any noticeable differences between the different references.

The LT5400, references' LTD influence the gain error. Among the boards, the ADR1001 offers the best 24-hour accuracy performance, while the ADR1399 and the ADR4550D exhibit lower accuracy compared to the ADR1001.

Table 5. 24-Hour Accuracy Comparison with the Different References

	Board with ADR1001	Board with ADR1399	Board with ADR4550D	Typical 7.5-Digit DMM	Typical 8.5-Digit DMM
Offset Error/ Range Error (ppm)	0.07	0.09	0.2	2	0.05
Gain Error/ Reading Error (ppm)	0.55	1.84	9.23	8	0.5

Application Focus: DMM (Digital Multimeter)

Table 6 lists the specification comparison table of the signal chain board with typical high accuracy DMMs:

- The measured performance of the ADA4523-1 + AD4630 + ADR1001 or ADR1399 is better than 7.5-digit DMMs.
- The 24-hour accuracy, linearity, and TC of the ADA4523 + AD4630 + ADR1399 are slightly inferior to those of the ADR1001.
- The 1-year accuracy value is a theoretical estimation derived from prior calculations. LTD of references significantly influences the specifications. To mitigate the impact of LTD on 1-year accuracy, components or boards are baked before installation and shipment to customers. This process helps eliminate the substantial early life drift of the components.

The actual DMM equipment is more complex than the one discussed in this article. It includes additional circuits for input protection, voltage, current, and impedance measurements, introducing more uncertainties. The article focuses on a simpler signal chain setup, showcasing the performance of specific parts. Design engineers can use these results as a reference when creating highly accurate equipment.

Table 6. Specifications Comparison Between Typical DMMs and the Article Solution

	6.5-Digit DMM	7.5-Digit DMM1	7.5-Digit DMM2	8.5-Digit DMM	ADA4523-1 + AD4630 + ADR1001	ADA4523-1 + AD4630 + ADR1399
Digits	6.5	7.5	7.5	8.5	7.5	7.5
Input Range (V)	10	20	10	10	10	9
Resolution (ppm)	1	0.1	0.1	0.01	0.05	0.05
24-Hour Accuracy (ppm)	15 + 4	7 + 4	8 + 2	0.5 + 0.05	0.55 + 0.07	1.84+0.09
1-Year Accuracy (ppm)	35 + 5	24 + 4	16 + 2	8 + 0.05	13.4 + 1.5 (theory)	23.1 + 1.5 (theory)
Linearity (ppm)	3	3.5	1.5	0.1	0.2	0.3
Noise (ppm)	1	0.1	0.1	0.01	0.05	0.05
TC (ppm/°C)	5+1		5+1	0.5 + 0.01	0.59 + 0.017	1.12+0.016

Application Focus: Field Meter Calibrators

Field meters like pressure meters, temperature meters, and process meters need calibration. Calibrators integrate high accuracy DC signal measurement modules. The table below lists the typical specifications when the calibrator is used to measure ±10 V voltage, which is similar to the 7.5-digit DMM specifications in Table 6. The ADA4523-1 + AD4630 + ADR1001/ADR1399 + LT5400 can also be used in high accuracy calibrator for field meters.

Table 7. Typical Specifications of High Accuracy Field Meter Calibrators

Range	Reading	Resolution	24-Hour Accuracy (20 ± 1)°C	1-Year Accuracy (20 ± 1)°C	TC
±10 V	Slow	1 µV	2 ppm + 0.05 ppm	14 ppm + 0.08 ppm	1 ppm + 0.3 µV
	Mid	1 µV	2 ppm + 0.35 ppm	14 ppm + 0.38 ppm	
	High	10 µV	2.6 ppm + 1.05 ppm	14.6 ppm + 1.08 ppm	

Application Focus: 3-Phase Standard Meter

In testing single or 3-phase power and energy meters, a standard meter serves as the reference grade standard. It needs exceptionally high accuracy at the power frequency (50 Hz or 60 Hz) for accurate testing. Table 8 lists the typical specifications of 3-phase standard meters. For an ADA4523-1 + AD4630 + ADR1001 signal chain, 24-hour voltage accuracy and drift specification are similar with these standard meters.

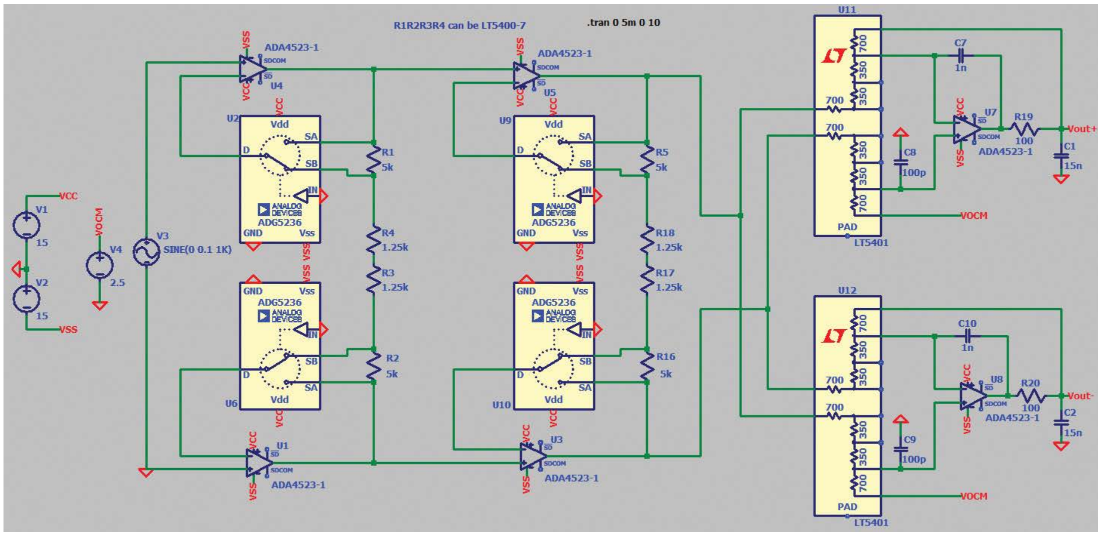

Figure 15. PGIA Circuit 1.

Table 8. Typical specifications of 3-Phase Standard Meter

	Standard Meter 1	Standard Meter 2	ADA4523-1 + AD4630 + ADR1001
Fundamental Frequency	15 Hz to ~70 Hz	40 Hz to ~1000 Hz	50 Hz
24-Hour Voltage Accuracy Drift LTD	40 ppm + 10 ppm 0.5 ppm/K <15 ppm/Year	12 ppm + 8 ppm 0.4 ppm/K 15 ppm/Year	14 ppm + 1 ppm 0.54 ppm/K 15 ppm/Year (theory)

Application Focus: High Accuracy Data Logger

The data logger can be used in a broad range of measurement and control functions. To achieve high accuracy measurements of voltage, thermocouples, and current with varying amplitudes and frequencies, 24-bit ADCs are commonly used.

Hardware designers developing these data acquisition signal chains typically require high input impedance to allow direct interface with a variety of sensors. In this case, a programmable gain is often needed to adapt the circuit to different input signal amplitudes—unipolar or bipolar and single-ended or differential with varying common-mode voltages. The majority of PGIAs (programmable gain instrumentation amplifiers) consist of a single-ended output that cannot directly drive a fully differential, high precision SAR architecture-based signal chain at full speed and may require at least one signal conditioning or driver stage.

Figure 15 shows the PGIA AFE Solution 1:

- The ADA4523-1 and the LT5400/LT5401 are selected due to their TC specifications.
- The ADG5234 is chosen for its low capacitance.
- The first stage Gain is 1 or 5, and the second stage Gain is also 1 or 5. By switching the ADG5234, the total gain can be 1, 5, or 25.
- The last stage consists of the ADA4523-1 and LT5401, which attenuate the signal within the ADC input range.
- When combined with the AD4630-24 and the ADR4550B, the signal chain can be used in high accuracy data logger applications.

Table 9 displays noise specifications for various input ranges and output data rate (ODR). The typical accuracy specifications is ±400 ppm + 2 μV within the operating temperature range of 0°C to 40°C. The combination of ADA4523-1, AD4630, and ADR4550B/LTC6655LN offers significantly lower noise levels, especially at ±5000 mV range and ±1000 mV range.

Table 9. Typical Noise Specifications at Different Input Range and ODR

ODR (Hz)	Range (mV)	Traditional Data Logger Rms Noise (μV)	PGIA Circuit 1 RTI Rms Noise (μV) (ADR4550B)	PGIA Circuit 1 RTI RMS Noise (μV) (LTC6655LNB)
15000	±5000 ±1000 ±200	11.8 2.6 1.0	3.3 1.08 0.93	3.0 1.08 0.93
50	±5000 ±1000 ±200	0.88 0.2 0.08	0.15 0.07 0.06	0.15 0.06 0.06
5	±5000 ±1000 ±200	0.28 0.07 0.03	0.08 0.03 0.02	0.08 0.03 0.02

Additionally, the INL and accuracy of the signal chain are excellent. Looking at Table 10, the accuracy achieved with ADA4523-1 + AD4630 + ADR4550B/LTC6655LN is ten times better than 400 ppm specification commonly found in traditional data loggers.

Table 10. INL and TC Accuracy at Different Gains

	INL at 0°C to ~40°C (ADR4550B)	INL at 0°C to ~40°C (LTC6655LNB)	TC Accuracy (ADR4550B)	TC Accuracy (LTC6655LNB)
Gain = 1	0.39 ppm	0.24 ppm	±(42 ppm + 2.9 ppm)	±(54 ppm + 6.1 ppm)
Gain = 5	0.16 ppm	0.12 ppm	±(45 ppm + 4.6 ppm)	±(54 ppm + 5.4 ppm)
Gain = 25	1.31 ppm	2.26 ppm	±(48 ppm + 14 ppm)	±(58 ppm + 14 ppm)

Another PGIA AFE solution is shown in Figure 16, which uses two stages to decrease the noise from the amplifier. This circuit provides various gain options by using different LT5400-X components. It allows users to configure different gains based on specific requirements.

- When mux's S1A is connected, Gain = 1
- When mux's S3A is connected, Gain = 5
- When mux's S2A is connected, Gain = 21

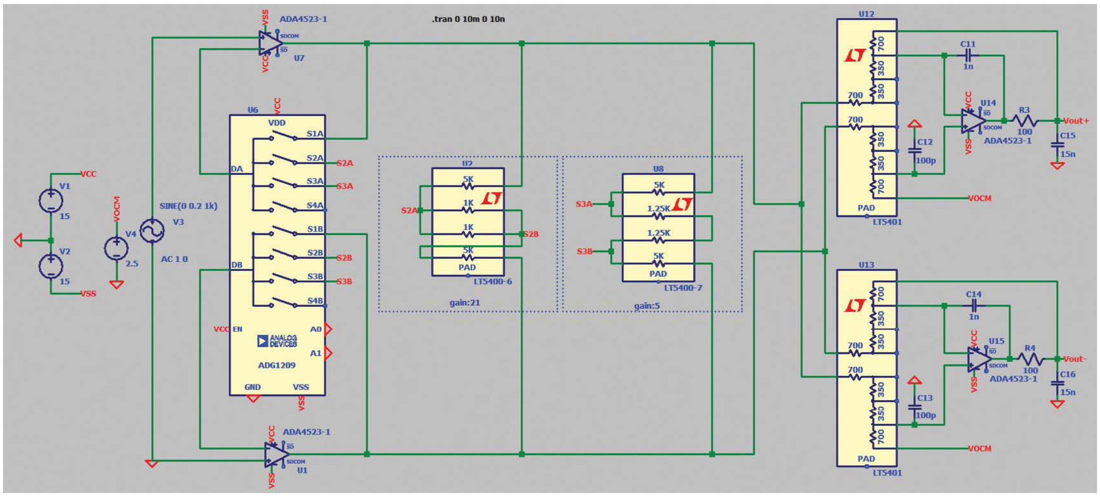

Figure 16. PGIA Circuit 2.

Table 11 compares the RTI rms noise of PGIA Circuit 1 and Circuit 2. Circuit 2 exhibits lower noise at high gain and high ODR. The linearity and TC test results are similar for both PGIA circuits.

Table 11. RTI Noise of Two PGIA Circuits

ODR (Hz)	Gain	PGIA Circuit 1 RTI Rms Noise (μV)	PGIA Circuit 2 RTI Rms Noise (μV)
19000	1 25 or 21	3.31 1.08	3.37 0.82
50	1 25 or 21	0.155 0.058	0.159 0.051
5	1 25 or 21	0.083 0.018	0.085 0.018

Conclusion

In precision instrumentation applications such as DMMs, sigma-delta ADCs are commonly used. However, achieving lower linearity and higher accuracy can be challenging due to limitations in INL specifications. Additionally, the complex external signal conditioning design of buried Zener voltage references poses a bottleneck for customers seeking to enhance the performance of their established products.

By utilizing components like the 0.1 ppm INL 2 MSPS SAR AD4630-24, the fully integrated ultralow drift ADR1001, the low noise zero drift ADA4523-1, and the 1 ppm/°C LT5400, the analog front-end signal chain can attain impressive specifications: 0.6 ppm 24-hour accuracy, 0.2 ppm linearity, 0.05 ppm noise, and 0.6 ppm/°C temperature coefficient. These real measurement results align closely with the theoretical analysis and calculations presented in Part 1 of the article series. This suggests that the signal chain is suitable for various high accuracy applications, including DMMs, field meter calibrators, 3-phase standard meters, and high accuracy data loggers.

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