28 nm Analog-to-Digital Converters Enable Next-Generation Electronic Warfare Receiver Systems

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Introduction

The ever-present need for higher bandwidth and lower size, weight, and power (SWaP) in electronic warfare (EW) receivers, specifically those for signal intelligence (SIGINT) applications, has EW system designers continually looking for new developments and improvements in high speed analog-to-digital converter (ADC) technology. While 65 nm ADCs approach their inherent, process-related performance and bandwidth limitations, new 28 nm RF ADCs surpass these boundaries and form a new foundation for next-generation wideband receiver systems. A 28 nm process node's smaller transistor widths and lower parasitics enable faster sample rates, wider analog input bandwidth, integrated digital functionality, and new receiver architectures, all while reducing power consumption and overall size.

28 nm ADC Benefits

As wideband electronic warfare systems become increasingly prevalent in the modern battlefield, system designers are posed with many challenges with how to achieve higher performance and lower SWaP required by next-generation EW receivers. The high speed ADC is one of the primary design considerations in all wideband EW receivers and largely determines system architecture and overall detection and observation capability. Many performance characteristics of the high speed ADC, including sample rate, bandwidth, and resolution, are determining factors on how the rest of the receiver is designed—all the way from the analog RF domain to the DSP requirements. As EW system designers continue to develop the next-generation EW receivers, the need for higher ADC bandwidth and greater resolution remains the perpetual industry trend. Higher sample rates and bandwidth allow for more spectrum to be digitized at once, easing design challenges in the RF domain and reducing sweep times while greater bit depth leads to increased performance and fewer false alarms and detections. This insatiable need for higher sample rate and better resolution has led high speed ADC manufacturers to move to increasingly smaller transistor lithographic nodes (currently 28 nm and 16 nm) that enable these requirements to be achieved without increasing device power consumption.

The fundamental benefits of 28 nm ADCs are integral in enabling the next generation of wideband EW receivers and form a new foundation on which future systems will be built. 28 nm transistors have reduced parasitic gate capacitance, enabling faster switching due to the lower energy required to drive the switching. Because of this and the smaller physical transistor size of the 28 nm process, ADCs can not only achieve faster sample rates but also fit a greater number of transistors per square mm, leading to potentially greater digital processing capabilities. Taking the inherently lower power consumption into consideration makes ADCs on the 28 nm process key enablers in next-generation EW systems with performance and capability requirements previously considered impractical on the ≥65 nm process. The greater sample rates (several GSPS and above) achievable with 28 nm ADCs are one of the most attractive ADC features to most EW system designers, especially for SIGINT, electronic protect (EP), and electronic support (ES) applications. Just as important as ADC bandwidth is the resolution, which allows for greater SNR/SFDR and subsequent ability to detect, observe, and process a target signal. Undersampling beyond the 1st Nyquist is also possible as a result of higher analog input bandwidths.

Moving to a 28 nm process also allows mixed-signal semiconductor manufacturers to integrate increasing amounts of digital signal processing and functionality into their high speed ADCs with no increase in (or even a reduction of) system SWaP. Digital features like integrated NCOs (numerically controlled oscillators) and DDCs (digital downconverters) push converter performance boundaries and allow for easing of system design challenges related to the higher converter data rates and high digital interface power consumption. Taking advantage of the smaller 28 nm process and increasing the on-chip DSP capabilities of ADCs can also offload much of the processing load and power consumption from the processor, allowing EW system designers to drive down system SWaP.

While a faster 28 nm ADC enables a larger piece of the RF spectrum to be captured and observed, the signal of interest might still be of relatively small bandwidth compared to the ADC Nyquist bandwidth. Additionally, the vast amounts of data throughput from GSPS ADCs can lead to challenges finding a suitable processor and physically interfacing it to the ADC. Many 28 nm converters currently on the market use the JESD204B interface standard at lane rates above 10 Gbps, which can introduce board layout and signal integrity challenges associated with routing Gbps SERDES (serializer/deserializer) JESD lanes. Fortunately though, through integrated NCOs/DDCs and on-chip DSP, the ADC can convert the signal of interest down to a lower frequency or baseband, apply digital filtering, and decimate the digital data output rate so that more intensive processing can be performed on portions of the captured spectrum. Tunable NCOs allow the DDC to sweep across the digitized spectrum so that the entire spectrum can still be analyzed, but with the added benefits of processing

gain and lower digital data output rates. Adding multiple NCOs and DDCs in parallel allows the user to preconfigure and quickly switch and fast hop between the DDCs, further reducing sweep times since NCO tuning is removed from the equation. The integrated DDCs also offer significant power savings in the digital JESD204B interface. JESD SERDES running at such high rates can add a watt or more to system power consumption so decimating the data rate down to lower speeds is very beneficial in this aspect. As high speed ADCs continue to push to higher sample rates, bit depths, and bandwidth, integrating DDCs and ADCs becomes more attractive to wideband EW receiver system designers since the enormous amount of digital data from the ADC can become difficult to process with a low SWaP processor. For more information on DDCs and some practical examples, please see "What's Up with Digital Downconverters" Part 1 and Part 2 by Jonathan Harris.

Realizing New Receiver Architectures

Heterodyne receiver architectures are well understood and have been proven over many years. Historically, many microwave receivers have been implemented with dual downconversion architectures. With the ADCs available in previous generations, the large ratio of operating band frequencies to ADC input frequencies made image filtering impractical with a single downconversion receiver architecture. New ADCs increasing in both sample rate and analog input bandwidth now make high performance wideband single downconversion architectures practical and easily realizable.

An example single downconversion receiver architecture is shown in Figure 1. The front-end LNA is chosen for noise figure performance. If needed, a limiter is added in front of the LNA to increase the survive power capability of the front end. An operating band filter is next to attenuate out-of-band interference. Next, additional gain and/or gain control can be added as needed. Prior to the mixer, a low-pass filter can reduce RF harmonics that add to mixing spurious output. The mixer is a critical building block and chosen to optimize performance in the frequency translation bands of interest. Another low-pass filter following the mixer filters upper sidebands prior to amplification. Additional IF gain is added as needed. The antialiasing filter is typically the final component prior to the ADC and rejects any frequencies that can fold in band through the sampling process. The ADC is next and, although it is last in the chain, is typically the first component chosen while the rest of the receiver is built around the ADC.

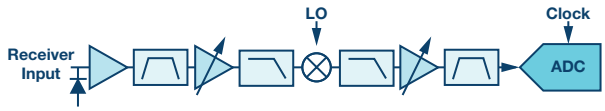


Figure 1. Example single downconversion receiver architecture.

Next, we review some considerations when selecting frequency plan options. Frequency planning is the process of selecting a frequency translation approach that, when implemented with the components available, yields the lowest spurious performance with reasonable filter designs. As RF engineers enter this decision for the first time, there are a number of options and repercussions of a suboptimal frequency plan that can make this a daunting task. Fortunately, modern advances in both CAD tools and the available components have made frequency planning a much more manageable task.

In general, a higher IF frequency in the 2nd or 3rd ADC Nyquist zone is preferred from a spurious perspective. We will outline the benefits by first showing a frequency plan translating a 10 GHz operating band to the 1st Nyquist of a 3 GHz ADC, then show the benefits when operating in the 2nd Nyquist zone.

Figure 2 shows the frequency translation of a 1 GHz operating band at 10 GHz to the 1st Nyquist zone of a 3 GSPS ADC. Two primary issues are illustrated. First, the RF image frequency is very closely spaced to the operating band requiring a very difficult filter for image suppression. Second, any IF created from the IF amplification stages are in-band and unable to be filtered by the antialiasing filter.

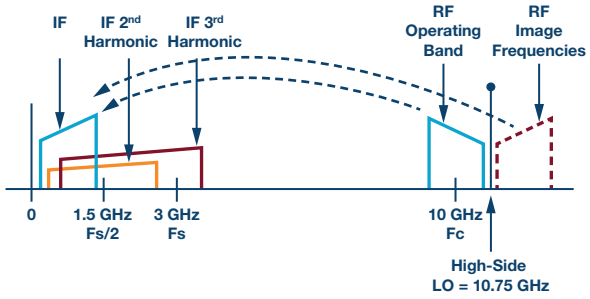


Figure 2. Problematic frequency plan. The IF harmonics are within the IF band—this makes the image filtering difficult.

Figure 3 shows a comparison when the same RF operating band is sampled in the 2nd Nyquist zone. The higher IF frequency results in the image frequency that is much further away from the operating band and the RF image filters are significantly easier to implement. In addition, any harmonics created in the IF amplifiers can be filtered by the antialiasing filter and the only IF harmonics that will be created are the ones inside the ADC itself.

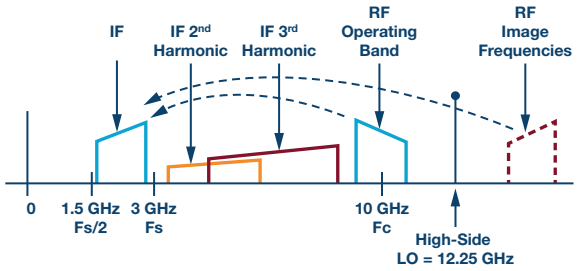


Figure 3. Improved frequency plan: The IF harmonics are outside the IF band, which means the image filtering is realizable.

A spur analysis using the Keysight Genesys tool can be used to quickly come to the same conclusion. Figure 4 is from the WhatIF frequency planning tool. Figure 4 shows the WhatIF frequency planning tool, where it is set to a 10 GHz operating band, 1 GHz instantaneous bandwidth, high-side LO selection, and a search for up to fifth-order spurious. Spur free zones are illustrated in green and, in this case, fall in the 2nd Nyquist zone of a 3 GSPS ADC.

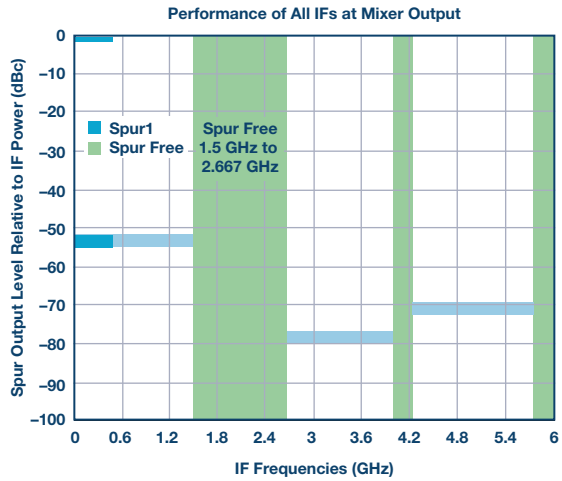


Figure 4. Spur analysis using the Keysight Genesys WhatIF frequency planning tool.

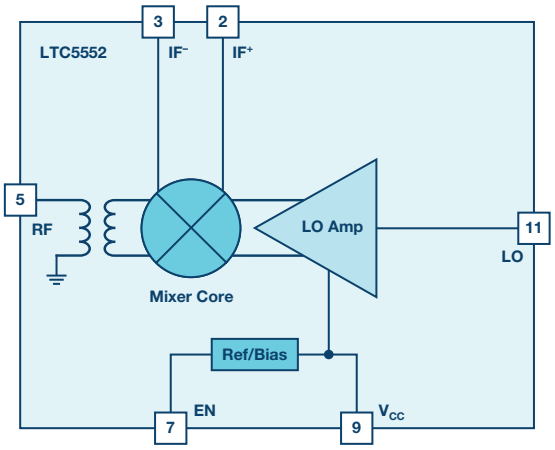
Component Enablers

As a follow up to any frequency plan analysis, mixers and ADCs should be evaluated under their intended operating conditions in the receiver to validate the spurious and noise performance.

Recently released high performance 3 GHz to 20 GHz mixers include the LTC5552 and LTC5553. Figure 5 shows key features to these devices. These are best-in-class, high linearity broadband mixers that fit directly into a wideband receiver architectures. The primary difference is the LTC5552 has a differential IF output, while the LTC5553 is single ended on all ports. The differential IF output allows the entire IF chain to remain differential, thus eliminating the balun that is normally added to the ADC input. Differential IF amplifiers are readily available by making a completely differential IF section realizable with the only design adjustment being the introduction of differential filters into the IF signal chains.

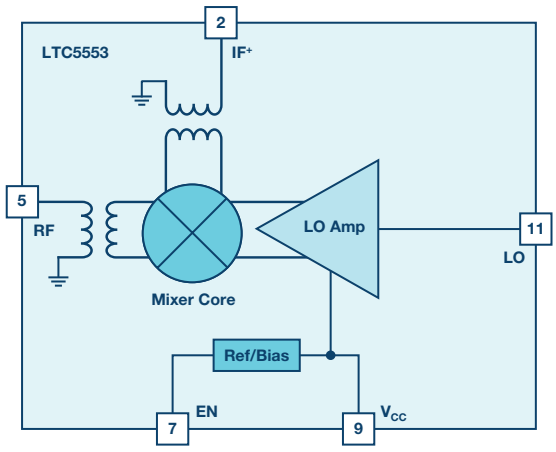
A recently released 28 nm ADC is the AD9208, a 14-bit, 3 GSPS dual ADC with many of the feature sets and characteristics mentioned previously in this article. The high input bandwidth and sampling resolution, along with digital features, like four integrated DDCs and NCOs, make the AD9208 well-suited for many EW receiver systems and applications. Additionally, a high analog input bandwidth of 9 GHz allows the AD9208 to directly sample up into the 2nd and 3rd Nyquist frequencies. Even 4th Nyquist sampling is possible with a clean, low jitter reference clock to minimize SNR degradation at higher input frequencies.

A continual challenge for the RF receiver designer is that every critical ADC metric degrades with input frequency. This is true for both noise and spurious-free dynamic range. In addition to silicon limitations, careful packaging design accommodating for the RF launch from the silicon to the packaging laminate and from the package to the PWB is required to maintain input bandwidths for GHz converters.



GND Pins are Not Shown

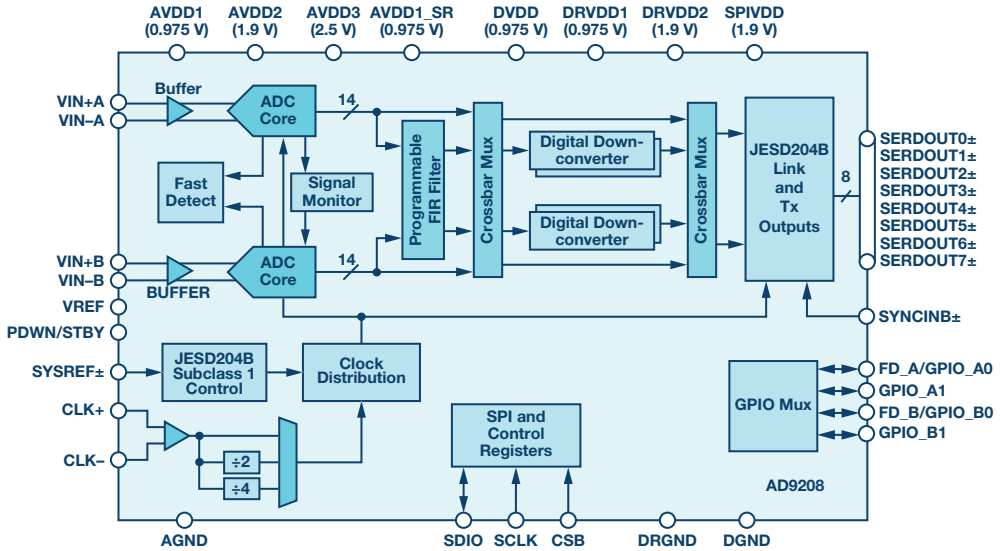
Features
- Integrated LO Buffer: 0 dBm LO Drive
- 50 Ω Wideband Matched RF and LO Ports
- Wide IF Bandwidth: DC to 6 GHz
- Upconversion or Downconversion
- High IIP3:
  - 22.5 dBm at 10 GHz
  - 18.3 dBm at 17 GHz
- 14.6 dBm Input P1 dB at 10 GHz
- 8 dB Conversion Loss at 10 GHz
- 3.3 V/132 mA Supply
- Fast Turn ON/OFF for TDD Operation
- 3 mm × 2 mm, 12-Lead QFN Package



GND Pins are Not Shown

Features
- Upconversion or Downconversion
- High IIP3:
  - 24.3 dBm at 10 GHz
  - 21.5 dBm at 17 GHz
- 9 dB Conversion Loss at 10 GHz
- 16 dBm Input P1 dB at 10 GHz
- Integrated LO Buffer: 0 dBm LO Drive
- Low LO-RF Leakage; < –25 dBm
- 50 Ω Wideband Matched RF, LO, and IF Ports
- 3.3 V/132 mA Supply
- Fast Turn ON/OFF for TDD Operation
- 3 mm × 2 mm, 12-Lead QFN Package

Figure 5. Wideband, high performance, high linearity mixers.



Features
- JESD204B (Subclass 1) Coded Serial Digital Outputs Support for Lane Rates Up to 16 Gbps Per Lane
- 1.65 W Total Power Per Channel at 3 GSPS (Default Settings)
- Performance at –2 dBFS Amplitude, 2.6 GHz Input
  - SFDR = 70 dBFS
  - SNR = 57.2 dBFS
- Performance at –9 dBFS Amplitude, 2.6 GHz Input
  - SFDR = 78 dBFS
  - SNR = 59.5 dBFS
- Integrated Input Buffer
- Noise Density = –152 dBFS/Hz
- 0.975 V, 1.9 V, and 2.5 V DC Supply Operation
- 9 GHz Analog Input Full Power Bandwidth (–3 dB)
- Amplitude Detect Bits for Efficient AGC Implementation

Figure 6. AD9208: 28 nm 3 GSPS, high performance, wide input bandwidth ADC.

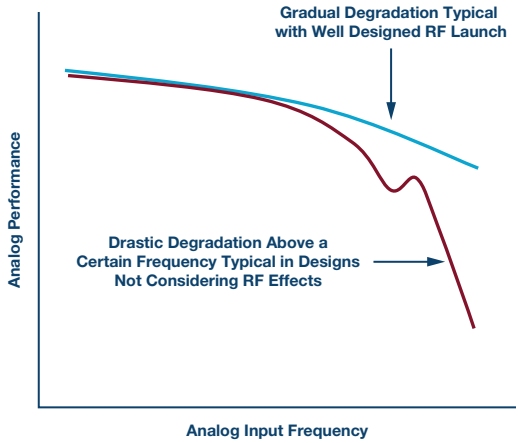


Figure 7. Analog performance: SNR, SFDR, and signal power all degrade with input frequency. Design for high IF sampling requires validating that the ADC selected does not significantly degrade with the input frequencies required. In addition, careful RF layout techniques are required with the implementation in a PWB design.

A well designed RF I/O structure will have gradual degradation vs. input frequency. Without these considerations in the design, there is typically an input frequency where the performance drastically degrades. This is illustrated conceptually in Figure 7. When screening converters for an application, much effort is spent validating performance prior to committing a design. For RF sampling ADCs operating well into the GHz frequencies, this becomes ever more important and the performance response vs. frequency should be well understood prior to ADC selection for an application.

Conclusion

A review of several wideband application and receiver design considerations has been discussed. The EW application is particularly challenging as a receiver with a wide operating band and as much instantaneous bandwidth as possible is desired. These challenges indicate that for single downconversion receiver architectures, operation in the higher ADC Nyquist zones will produce improved spurious performance. This objective challenges the input bandwidth of ADCs and performance parameters of mixing stages. Fortunately, enabling components, both high speed, 28 nm ADCs with extended input frequency ranges and broadband high linearity mixers, is now available to form the foundation for the next generation of receivers. Figure 6 shows a complete protection solution.

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