VT1697SBFQ Qualification Report

Report approved:
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Silicon Foundry: TSMC **Process Technology: 0.18 μM, 1 Poly, 3 Metal, 1.8/12V**
Assembly Sub-Contractor: UTL ` **Package Type: fcQFN-16, SAC105 (MSL Level = 1)**

Summary of Results (Product Related Stress Test)

Test(s)	Spec. Ref.	Conditions	Read points	Pass Criteria	Lot 1	Lot 2	Lot 3	Comments
High Temperature Operational Life (HTOL) #	JESD22-A108	T_A = 125°C V_{DDH} = 14.0V V_{DD}/V_{CC} = 2.1 V	168 Hours 500 Hours 1000 Hours	0/77 0/77 0/77	0/77 0/77 0/77	0/77 0/77 0/77	0/77 0/77 0/77	Pass
Electro Static Discharge Human Body Model (HBM) #	JS-001-2012 Formerly JESD22-A114	HBM	Post-ESD 500 Volts 1000 Volts 1500 Volts 2000 Volts	 0/21 0/21 0/21 0/21	 0/21 0/21 0/21 7/21	 0/21 0/21 0/21 9/21	 0/21 0/21 0/21 6/21	Pass HBM ESD Rating > 1500 Volts
ESD Characterization Charge Device Model #	JESD22-C101	CDM	Post-ESD 100 Volts 200 Volts 500 Volts 1000 Volts 2000 Volts	 0/3 0/3 0/3 0/3 0/3	 0/3 0/3 0/3 0/3 3/3	 0/3 0/3 0/3 0/3 1/3	 0/3 0/3 0/3 0/3 0/3	Pass CDM ESD Rating > 1000 Volts
Latch-Up (LU) #	JESD78	T_A=125°C at V_{DD} = Max. Max clamp = ±100mA Except Vx = ±1A	Post-LU Pass ATE	0/30	0/30	0/30	0/30	Pass Class 2

- # HTOL, ESD and Latch-Up tests are done using coupons (QFN Package soldered on to small PC boards)

Summary of Results (Package Related Stress Test)

Test(s)	Spec. Ref.	Conditions	Read points	Pass Criteria	Lot 1	Lot 2	Lot 3	Comments fcQFN-16 UTL Assembly
Temperature Cycling (TC) *	JESD22-A104 Condition B	-55^0C to 125^0C	500 Cycles 1000 Cycles	0/76 0/76	0/76 0/76	0/76 0/76	0/76 0/76	Pass
High Temperature Storage (HTS) *	JESD22-A103 Condition B	150^0C	500 Hours 1000 Hours	0/76 0/76	0/76 0/76	0/76 0/76	0/76 0/76	Pass
Highly Accelerated Stress Test (HAST) *	JESD22-A110	130°C, 2 ATM, 85% RH, V_{DDH} = 10.0 V	96 Hours	0/76	0/76	0/76	0/76	Pass

* Pre-conditioning prior to TC, HTS and HAST stress tests (per JESD22-A113 and J-STD-020) Level 1 at 260°C.