RELIABILITY REPORT

FOR

MAX574AxxI

PLASTIC ENCAPSULATED DEVICES

January 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MX574A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MX574 is a complete 12-bit analog-to-digital converter (ADC) that combines high speed, low-power consumption, and on-chip clock and voltage reference. The maximum conversion time is 25µs. Maxim's BiCMOS construction reduces power dissipation 3 times (150mW) over comparable devices. The internal buried zener reference provides low-drift and low-noise performance. External component requirements are limited to only decoupling capacitors and fixed resistors. The versatile analog input structure allows for 0V to +10V or 0V to +20V unipolar or ±5V or ±10V bipolar input ranges with pin strapping.

The MX574 uses standard microprocessor interface architectures and can be interfaced to 8-, 12- and 16-bit wide buses. Three-state data outputs are controlled by /CS, CE and R//C logic inputs.

B. Absolute Maximum Ratings

Item	Rating
V_{CC} to DGND	0V to +16.5V
V_{EE} to DGND	0V to -16.5V
V_L to DGND	0V to +7V
DGND to AGND	±1V
Control Inputs to DGND (CE, CS, A0, 12/8, R/C)	-0.3V to V_{CC} +0.3V
Digital Output Voltage to DGND (DB11-DB0, STS)	-0.3V, V_L +0.3V
Analog Inputs to AGND (REFIN, BIPOFF, $10V_{IN}$)	±16.5V
$20V_{IN}$ to AGND	±24V
REFOUT	Indefinite short to V_{CC} or AGND
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation (TA=+75°C)	1000mW
Derates above +75°C	10mW/°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin WSO	1000mW
28-Pin PDIP	1142.9mW
Derates above +70°C	
28-Pin WSO	12.5mW/°C
28-Pin PDIP	14.3mW/°C

II. Manufacturing Information

A. Description/Function:	Industry Standard Complete 12-Bit A/D Converter
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	974
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	March, 1993

III. Packaging Information

	28-Lead PDIP	**28-Lead WSO**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0101-0216	# 05-0101-0215
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	144 x 163 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contact: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 611 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.78 \times 10^{-9}$ $\lambda = 1.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0243) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AD55 die type has been found to have all pins able to withstand a transient pulse of 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1

Reliability Evaluation Test Results

MAX594AxxI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		611	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	WSO PDIP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

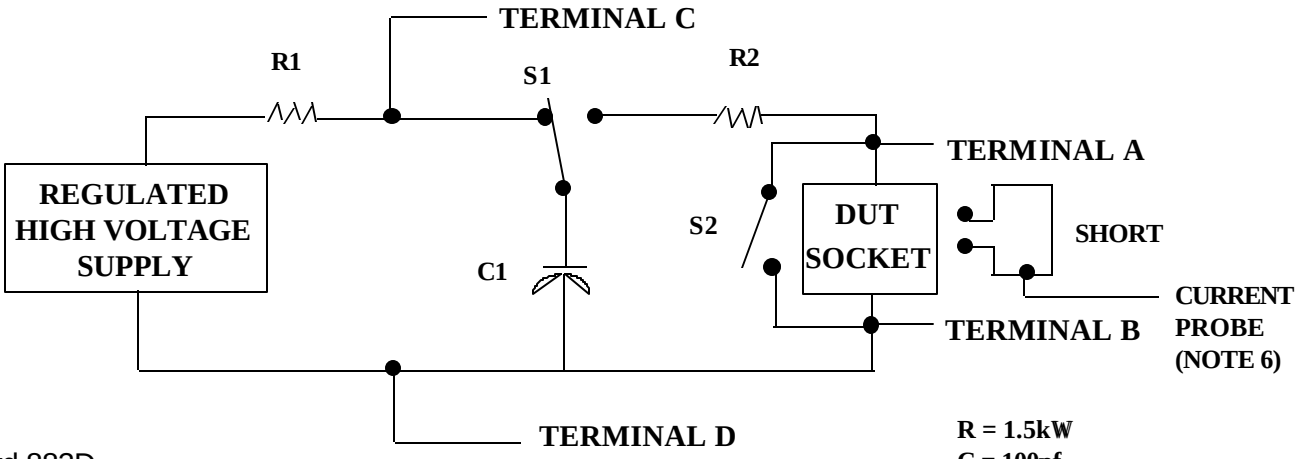
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

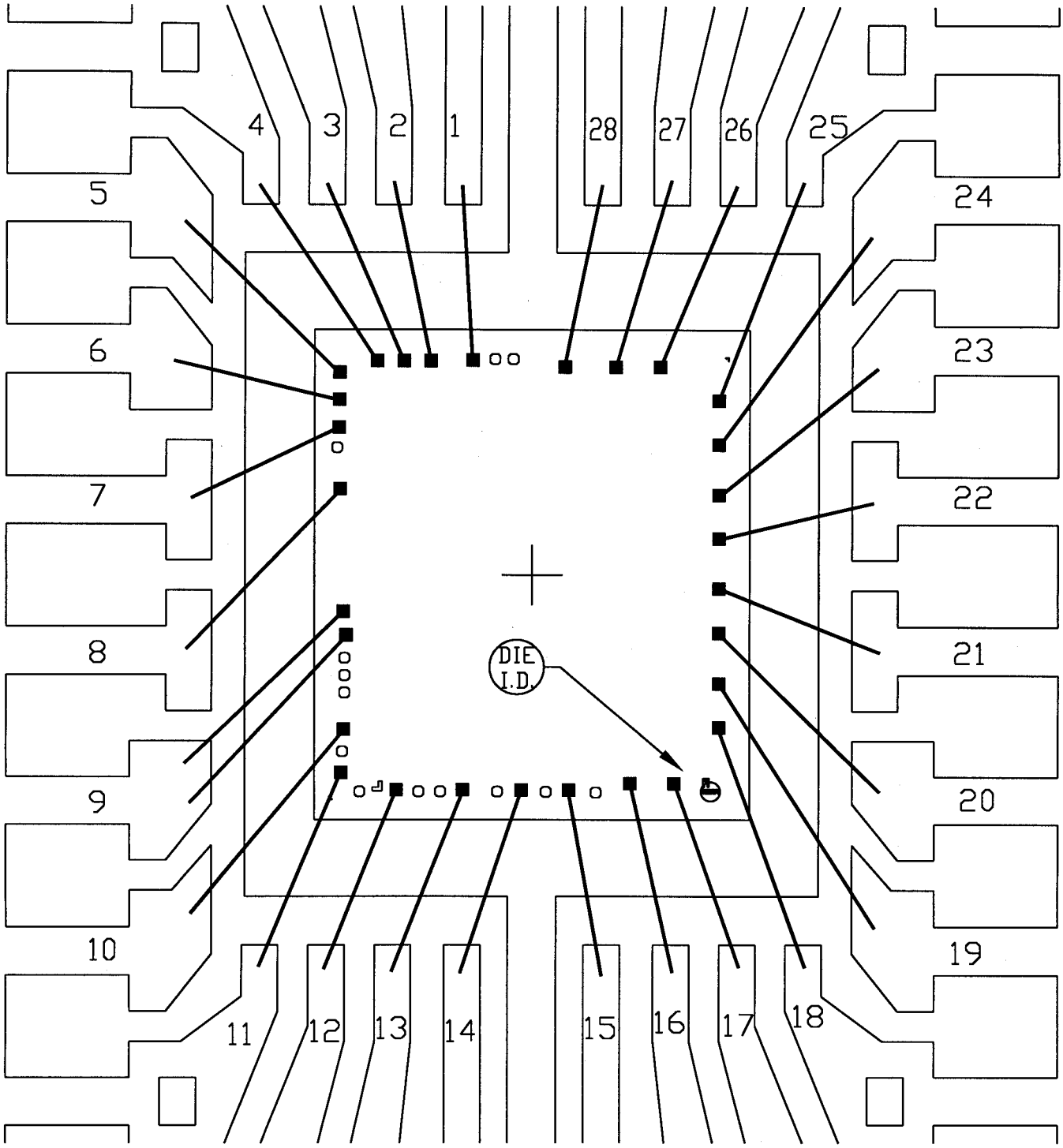
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

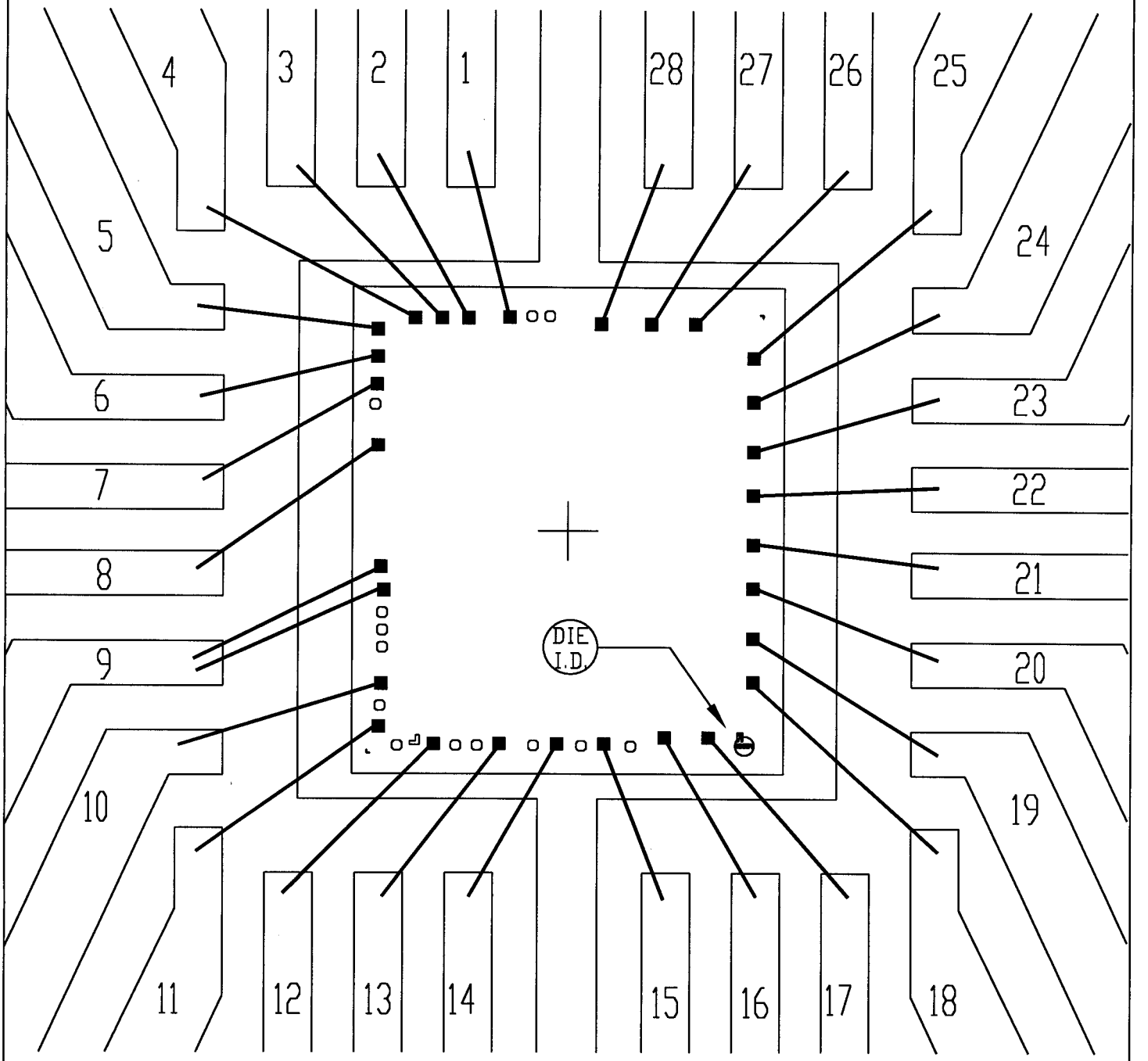


Mil Std 883D
Method 3015.7
Notice 8

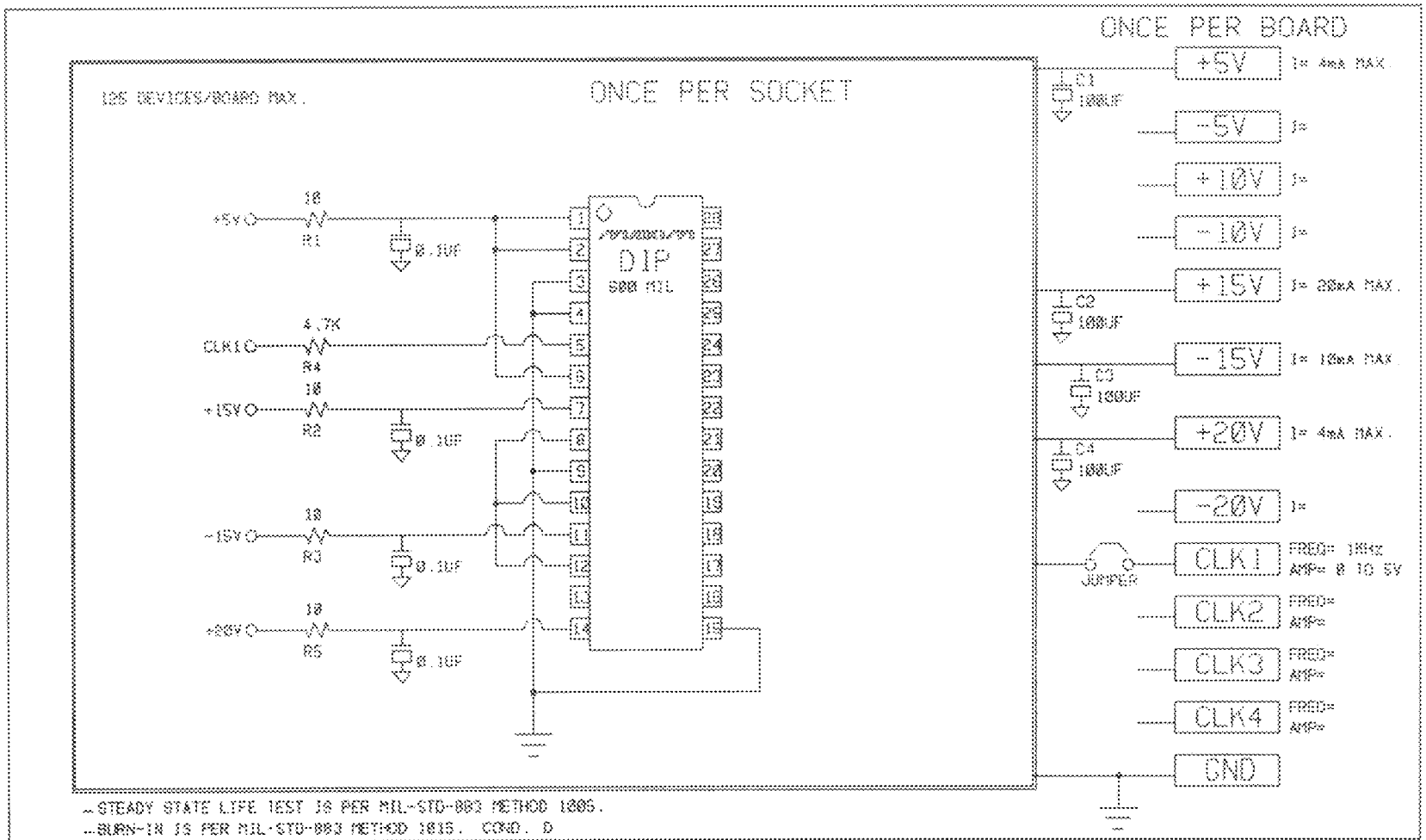


PKG. CODE: W28-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 190 X 214	PKG. DESIGN			BOND DIAGRAM #: 05-0101-0215 REV: F

45-0081 REV.A



PKG. CODE: P28-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 180 X 180	PKG. DESIGN			BOND DIAGRAM #: 05-0101-0216 REV: E



--STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
--BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. D

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL
   ( ) MR/883

SPEC. NO. 06-243 REV. B

DATE: 4/30/92

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX174, MX574/674/774