RELIABILITY REPORT

FOR

**MAX998Exx**

PLASTIC ENCAPSULATED DEVICES

June 22, 2003

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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**Conclusion**

The MAX976 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX998 single, high-speed, low-power comparator is optimized for +3V/+5V single-supply applications. It achieves a 20ns propagation delay while consuming only 225µA supply current per comparator. The MAX998 featuress a low-power shutdown mode that places the output in a high-impedance state and reduces supply current to 1nA.

The MAX998 inputs have a common-mode voltage range that extends 200mV below ground. The outputs are capable of Rail-to-Rail® operation without external pull-up circuitry, making this device ideal for interface with CMOS/TTL logic. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail. The comparators' internal hysteresis ensures clean output switching, even with slow-moving input signals.

For space-critical applications, the single MAX998 is available in a 6-pin SOT23 package.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Supply Voltage (VCC) | +6V |
| SHDN | -0.3V to 6V |
| All Other Pins | -0.3V to (VCC + 0.3V) |
| Duration of Output Short Circuit to GND or VCC | Continuous |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | -65°C to +160°C |
| Lead Temperature (soldering, 10sec) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 6-Pin SOT23 | 571mW |
| 8-Pin SO | 471mW |
| Derates above +70°C | |
| 6-Pin SOT23 | 7.1mW/°C |
| 8-Pin SO | 5.88mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Single, SOT23, Single-Supply, High-Speed, Low-Power Comparators |
| B. Process: | S12 (SG1.2) - Standard 1.2 micron silicon gate CMOS |
| C. Number of Device Transistors: | 300 |
| D. Fabrication Location: | California or Oregon, USA |
| E. Assembly Location: | Philippines, Malaysia or Thailand |
| F. Date of Initial Production: | January, 1998 |

## III. Packaging Information

| | **8-Lead SO** | **6-Lead SOT23** |
|---|---|---|
| A. Package Type: | | |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.0 mil dia.) | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-1501-0149 | # 05-1501-0150 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 27 x 50 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Copper/Si |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 1.2 microns (as drawn) |
| F. Minimum Metal Spacing: | 1.2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts:

| | |
|---|---|
| Jim Pedicord | (Manager, Reliability Operations) |
| Bryan Preeshl | (Executive Director of QA) |
| Kenneth Huening | (Vice President) |

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5306) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM41 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

## Table 1
Reliability Evaluation Test Results

### MAX998Exx

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 150°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | SO<br>SOT | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters<br>& functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

**Attachment #1**

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

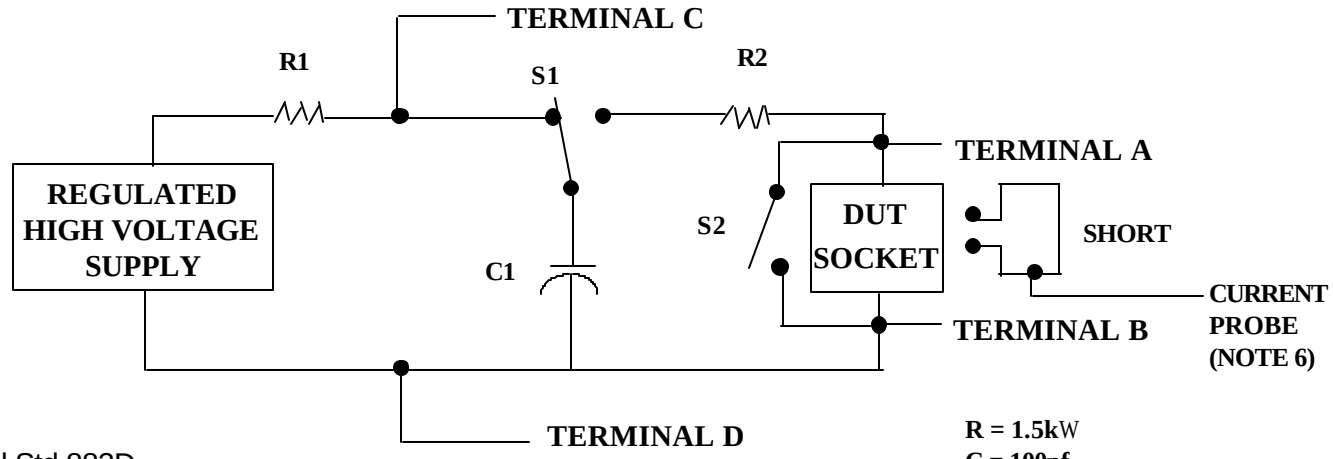
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

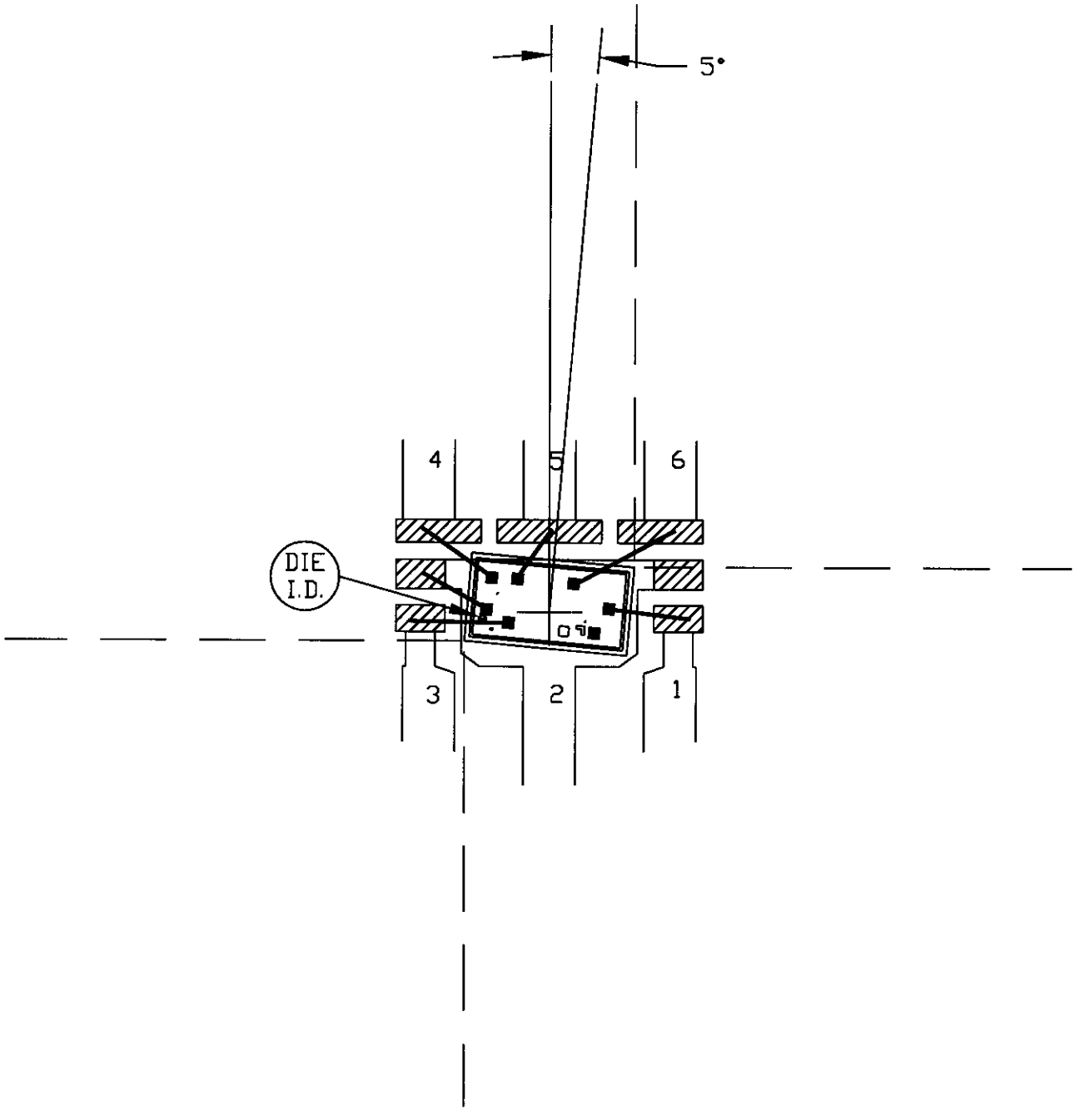
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



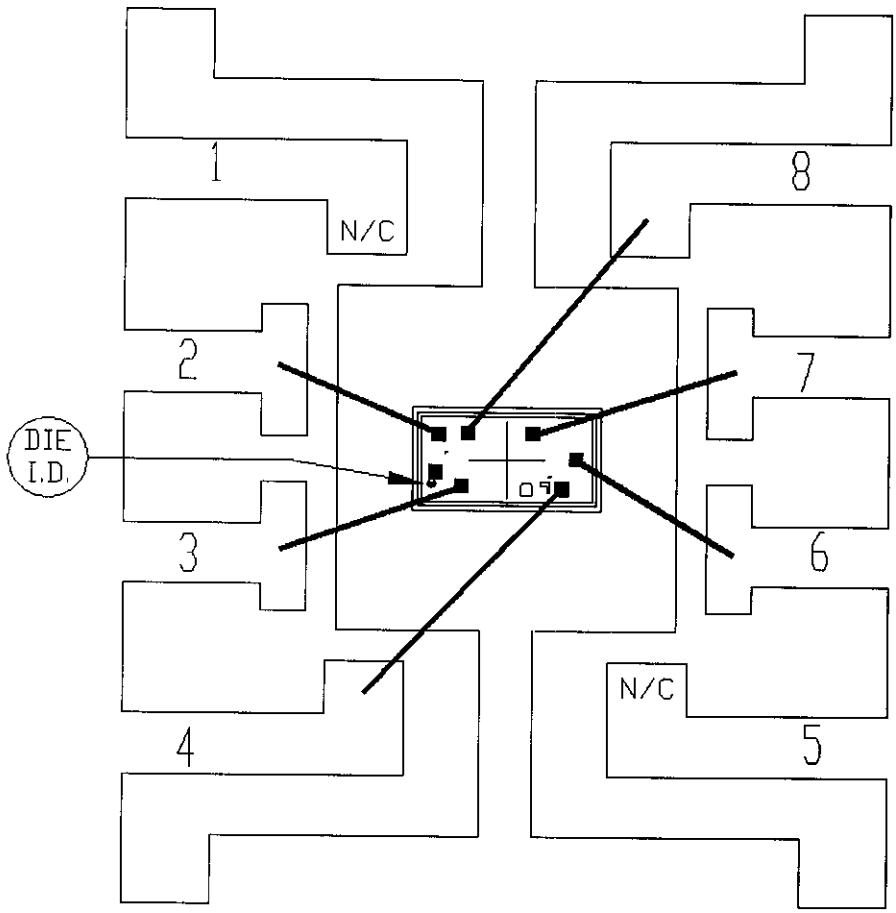

Mil Std 883D
Method 3015.7
Notice 8




Ø- BONDING AREA

NOTE: CAVITY DOWN

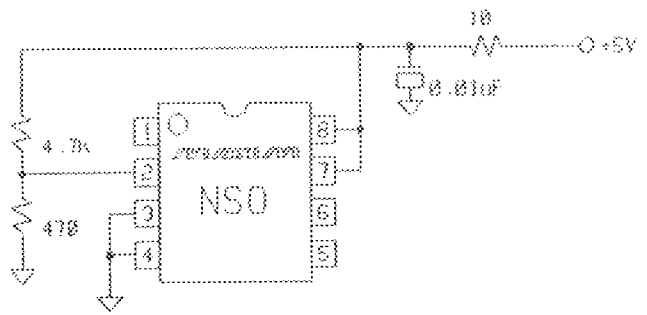
| | | | | |
|---|---|---|---|---|
| PKG.CODE: U6-2 | | APPROVALS | DATE: | MAXIM |
| CAV./PAD SIZE: 53X33 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1501-0150 / REV.: A |




| | | | | |
|---|---|---|---|---|
| PKG.CODE: S8-2 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 90 X 90 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1501-0149 / REV.: A |

ONCE PER BOARD

ONCE PER DEVICE




+5V I = 10mA

100uF

PS2 I=

PS3 I =

PS4 I=

PS5 I =

PS6 I =

CLK0 FREQ=
AMP=

CLK1 FREQ=
AMP=

CLK2 FREQ=
AMP=

CLK3 FREQ=
AMP=

CLK4 FREQ=
AMP=

GND

-STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
-BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-5306 REV: B

DATE: 8/31/99

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S): ALSO REFERENCE 06-5999

MAX938