RELIABILITY REPORT

FOR

MAX9961xxCCQ

PLASTIC ENCAPSULATED DEVICES

December 28, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX9961 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX9961 dual, low-power, high-speed, pin electronics driver/comparator/load (DCL) IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. The driver features a wide voltage range and highspeed operation, includes high-impedance and active termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 2mA of source and sink current. The load facilitates contact/continuity testing and pullup of high-output-impedance devices.

The MAX9961A provides tight matching of offset for the drivers and the comparators, allowing reference levels to be shared across multiple channels in cost-sensitive systems. Use the MAX9961B for system designs that incorporate independent reference levels for each channel.

The MAX9961provides high-speed, differential control inputs compatible with LVPECL, LVDS, and GTL. The MAX9961 is available with optional internal termination resistors. The open-collector comparator outputs are available with or without internal pullup resistors. The optional internal resistors significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage, slew-rate limit, and tri-state/terminate operational configurations of the MAX9961.

The MAX9961's operating range is -1.5V to +6.5V with power dissipation of only 900mW per channel. The device is available in a 100-pin, 14mm x 14mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +70°C to +100°C, and features a die temperature monitor output.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +11.5V
VEE to GND	-7.0V to +0.3V
VCC – VEE	-0.3V to +18V
GS to GND	±1V
DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_ to GND	-2.5V to +5.0V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_	±1.5V
VCCO_ to GND	-0.3V to +5V
SCLK, DIN, CS, RST, TDATA_, TRCV_, TLDEN_ to GND	-1.0V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_, FORCE_, SENSE_ to GND	-2.5V to +7.5V
DUT_, LDH_, LDL_ to GND	-2.5V to +7.5V
CPHV_ to GND	-2.5V to +8.5V
CPLV_ to GND	-3.5V to +7.5V
DHV_ to DLV_	±10V
DHV_ to DTV_	±10V
DLV_ to DTV_	±10V
CHV_ or CLV_ to DUT_	±10V
CH_, NCH_, CL_, NCL_ to GND	-2.5V to +5V
All Other Pins to GND	(VEE - 0.3V) to (VCC + 0.3V)
DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_ Current	±10mA
TEMP Current	-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V	Continuous
Continuous Power Dissipation (TA = +70°C)	
MAX9961_ _CCQ (derate 167mW/°C above +70°C)	13.3W*
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+125°C
Lead Temperature (soldering, 10s)	+300°C

**Dissipation wattage values are based on still air with no heat sink for the MAX9961. Actual maximum allowable power dissipation is a function of heat extraction technique and may be substantially higher.*

II. Manufacturing Information

A. Description/Function: Dual, Low-Power, 500Mbps ATE Drivers/Comparators with 2mA Load

B. Process: CB20

C. Number of Device Transistors: 5130

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: October, 2004

III. Packaging Information

A. Package Type: **100-Lead TQFP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.2 mil dia).

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-9000-1083 & 05-9000-0112

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C: Level 3

IV. Die Information

A. Dimensions: 236 x 236 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Reliability Operations)
Bryan Preeshl	(Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 44 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 11.17 \times 10^{-9}$ λ= 11.17 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B3A**). Current monitor data for the CB20 Process results in a FIT Rate of 0.17 @ 25C and 2.86 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AT03 die type has been found to have all pins able to withstand a transient pulse of +/-800V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX9961xxCCQ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Tj = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	44	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

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Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

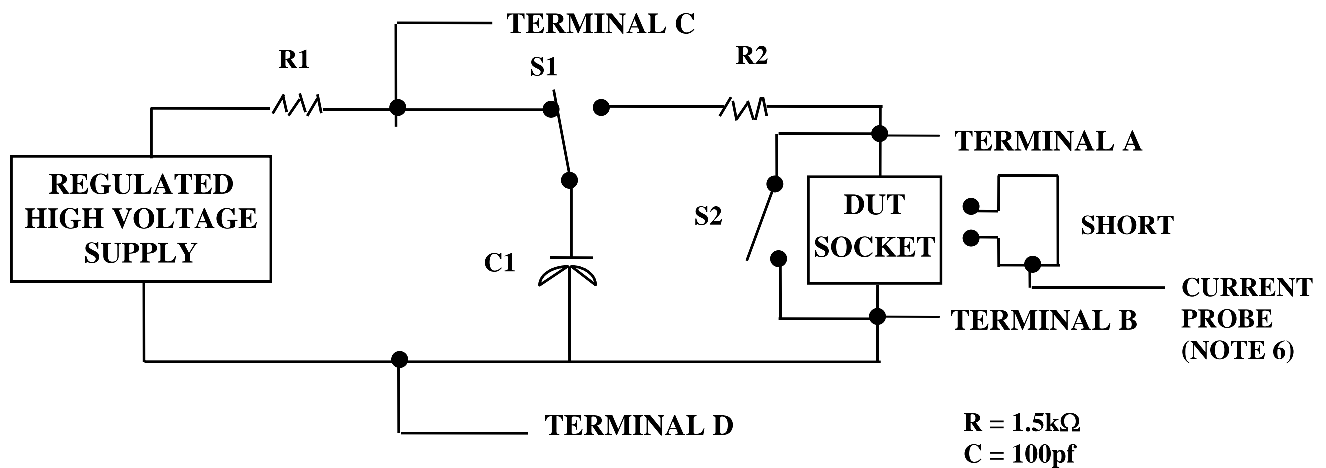
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S}$, $-V_{S}$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



76 80 85 90 95 100

75 1

70 5

65 10

60 15

55 20

51 25

50 45 40 35 30 26

DIE I.D.

EXPOSED PAD PKG.

CAVITY DOWN

SCALE: 15x

76 80 85 90 95 100

75 1

70 5

65 10

DIE I.D.

60 15

55 20

51 25

50 45 40 35 30 26

EXPOSED PAD PKG.

CAVITY DOWN

SCALE: 15x