

RELIABILITY REPORT

FOR

MAX9914EXK+T

PLASTIC ENCAPSULATED DEVICES

April 29, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by				
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Quality Assurance				
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Conclusion

The MAX9914EXK+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The single MAX9914/MAX9915 and dual MAX9916/MAX9917 operational amplifiers feature maximized ratio of gain bandwidth to supply current and are ideal for battery-powered applications such as portable instrumentation, portable medical equipment, and wireless handsets. These CMOS op amps feature an ultra-low 1pA input bias current, rail-to-rail inputs and outputs, low 20µA supply current, and operate from a single 1.8V to 5.5V supply. For additional power conservation, the MAX9915/MAX9917 feature a low-power shutdown mode that reduces supply current to 1nA, and puts the amplifier outputs in a high-impedance state. These devices are unity-gain stable with a 1MHz gain-bandwidth product. The MAX9914 and MAX9915 are available in 5-pin and 6-pin SC70 packages, respectively. The MAX9916 is available in an 8-pin SOT23 package, and the MAX9917 in a 10-pin µMAX® package. All devices are specified over the -40°C to +85°C extended operating temperature range.



II. Manufacturing Information

A. Description/Function: 1MHz, 20µA, Rail-to-Rail I/O Op Amps with Shutdown

B. Process: C6C. Number of Device Transistors: 201

D. Fabrication Location: USA or Japan

E. Assembly Location: Malaysia and Thailand

F. Date of Initial Production: July 23, 2005

III. Packaging Information

A. Package Type: 5-pin SC70

B. Lead Frame: Copper or Alloy42

C. Lead Finish: 100% matte Tin

D. Die Attach: Conductive

E. Bondwire: Au (1 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #05-9000-0883

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 324°C/W
K. Single Layer Theta Jc: 115°C/W
L. Multi Layer Theta Ja: 324°C/W
M. Multi Layer Theta Jc: 115°C/W

IV. Die Information

A. Dimensions: 30 X 30 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: Metal1-3 = 0.9 microns (as drawn)
 F. Minimum Metal Spacing: Metal1-3 = 0.9 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO₂I. Die Separation Method: Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppmD. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{\text{max}} = \underbrace{\frac{1.83}{192 \times 4340 \times 130 \times 2}}_{\text{(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)}$$

$$\lambda = 8.5 \times 10^{-9}$$

 λ = 8.5 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the C6 Process results in a FIT Rate of 0.2 @ 25C and 3.4 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot EOK3EQ002F, D/C 1140)

The OY16-3 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



Table 1Reliability Evaluation Test Results

MAX9914EXK+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (N	ote 1)				
	Ta = 135C	DC Parameters	50	0	SOK2CQ002B, D/C 0523
	Biased	& functionality	80	0	EOK3EQ002F, D/C 1140
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.