RELIABILITY REPORT

FOR

MAX987Exx

PLASTIC ENCAPSULATED DEVICES

August 5, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX987 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX987 single micropower comparator features low-voltage operation and Rail-to-Rail® input and output. The operating voltage ranges from +2.5V to +5.5V, making it ideal for both 3V and 5V systems. This comparator also operates with ±1.25V to ±2.75V dual supplies. It only consumes only 48µA per comparator while achieving a 120ns propagation delay.

The common-mode input voltage range extends 250mV beyond the supply rails. Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The output stage's unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX987 has a push/pull output stage that sinks as well as sources current. Large internal output drivers allow rail-to-rail output swing with loads up to 8mA.

B. Absolute Maximum Ratings

Item	Rating
VCC to VEE	6V
IN_-, IN_+ to VEE	-0.3V to (VCC + 0.3V)
OUT_ to VEE	-0.3V to (VCC + 0.3V)
OUT_ Short-Circuit Duration to VEE or VCC	10ns
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SC70	247mW
5-Pin SOT23	571mW
8-Pin NSO	471mW
Derates above +70°C	
5-Pin SC70	3.1mW/°C
5-Pin SOT23	7.1mW/°C
8-Pin NSO	5.88mW/°C

II. Manufacturing Information

A. Description:	High-Speed, Micropower, Low-Voltage Rail-to-Rail I/O Comparator
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	223
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Korea, Thailand, Philippines or Malaysia
F. Date of Initial Production:	July, 1997

III. Packaging Information

A. Package Type:	**5-Lead SC70**	**5-Lead SOT23**	**8-Lead NSO**
B. Lead Frame:	Alloy 42	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive	Non-Conductive	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1501-0200	# 05-1501-0136	# 05-1501-0135
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	31 x 30 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 480 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 2.26 \times 10^{-9}$ $\lambda = 2.26$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5255) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM61-2 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX987Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		480	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT23 SC70 NSO	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test may represent DIP qualification packages.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

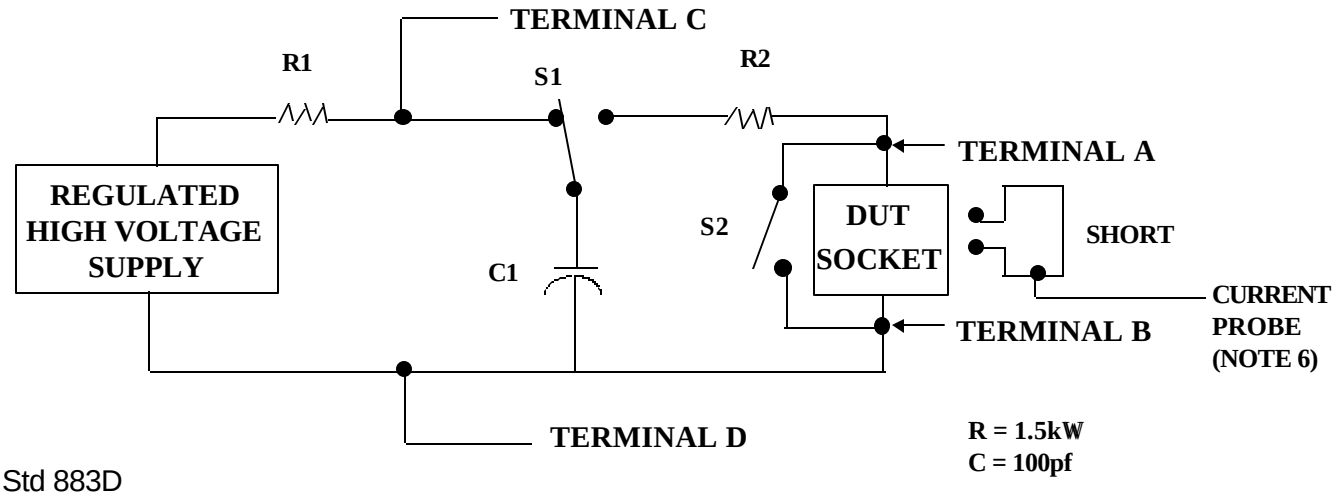
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

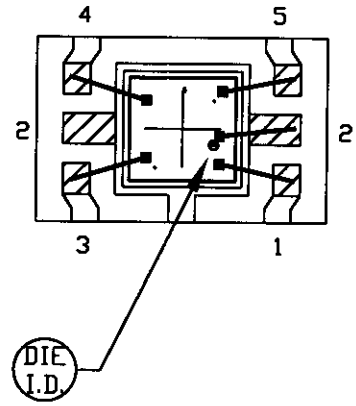
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

NOTES:
1. MAX DIE SIZE: 31x30
2. MIN. WIRE LENGTH: 21 MILS.

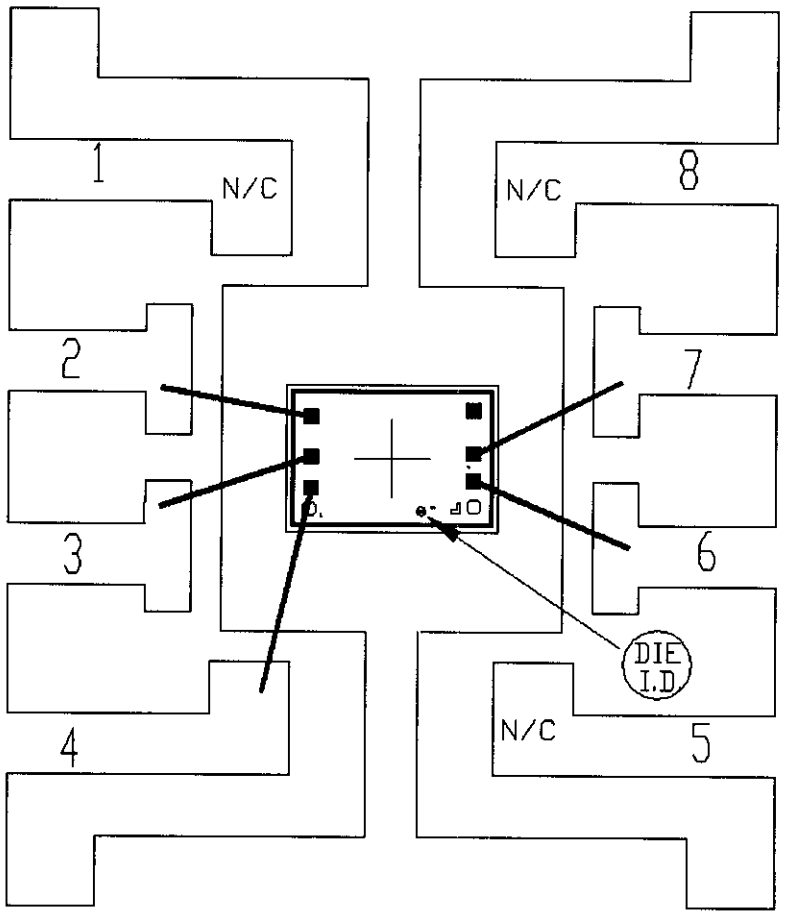


USE NON-CONDUCTIVE EPOXY

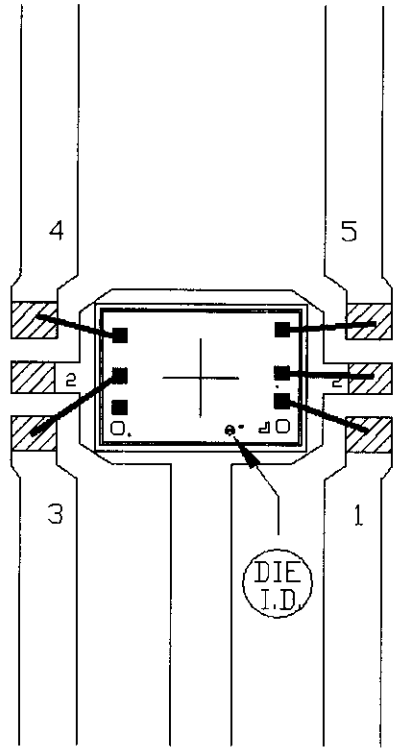
▨ BONDABLE AREA

NOTE: CAVITY DOWN

PKG. CODE: X5-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 35x34	PKG. DESIGN			BOND DIAGRAM #: 05-1501-0200	REV: B



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BUILDSHEET NUMBER: 05-1501-0135 REV.: A

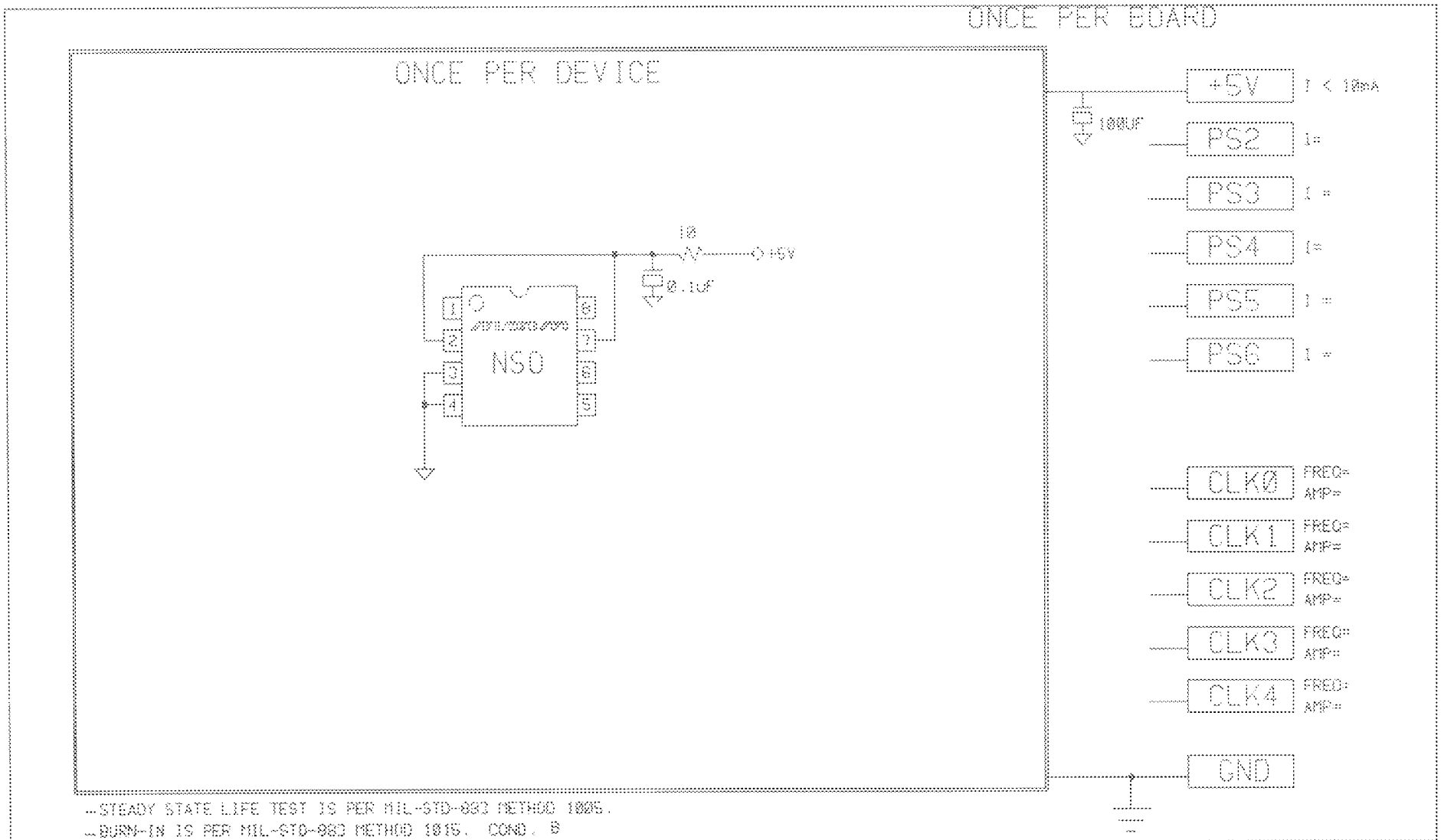


NOTE: MUST USE NON-CONDUCTIVE EPOXY

▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64X45	PKG. DESIGN			BUILDSHEET NUMBER: 05-1501-0136 / REV.: A



—STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
—BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-5255 REV: A

DATE: 12/18/96

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX985/6/7/8